EiceDRIVER™

2ED300C17-S 2ED300C17-ST

Dual IGBT Driver Board for Infineon Medium and High Power IGBT Modules

Power Management & Drives

2ED300C17-S 2ED300C17-ST

Revision History: 2013-08 V4.03

Previous Version:	V4.02	
Version	Page	Subjects (major changes since last revision)
4.03	2	Revision history modified. All changes included.
4.03	8; 18	Figure 4 and figure7 size changed.
4.02	19	Partial discharge test voltage added
4.02		Chapter 4.5 and 4.6 added
4.01		Update figure 2 and figure 6
4.00	all	General review, new hardware version V6

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Dual channel high voltage IGBT driver board

Product Highlights

- Galvanically isolated dual channel IGBT driver
- Reinforced isolation according to EN 50178
- Integrated protection features
- 5kV isolation test performed as 100% test
- High Electromagnetic Compatibility

Features

- Designed for Infineon IGBT modules up to 1700V
- High peak output current of 30A
- Integrated DC-DC SMPS
- Soft Shut Down in fault conditions
- Dynamic Over Current Detection
- IGBT desaturation monitoring
- Interlocking in half-bridge mode
- Open drain fault output
- Low impedance 15V inputs for high noise immunity
- ±15 V secondary drive voltage
- Short propagation delay time
- Optional sense function
- RoHS compliant
- UL94V-2 compliant materials

Typical Applications

- Renewable energies
- Drives and automation
- Transportation
- Power supplies
- Medical
- UPS systems

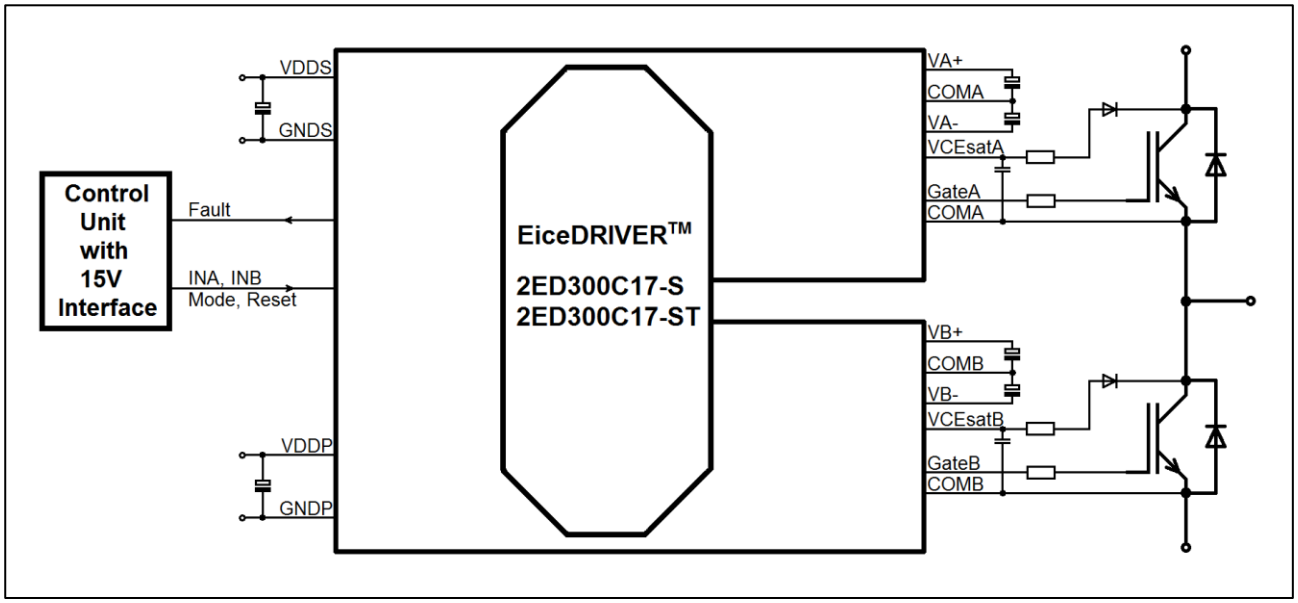

Figure 1: Basic schematic for driver setup

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1 Block Diagram and Schematic

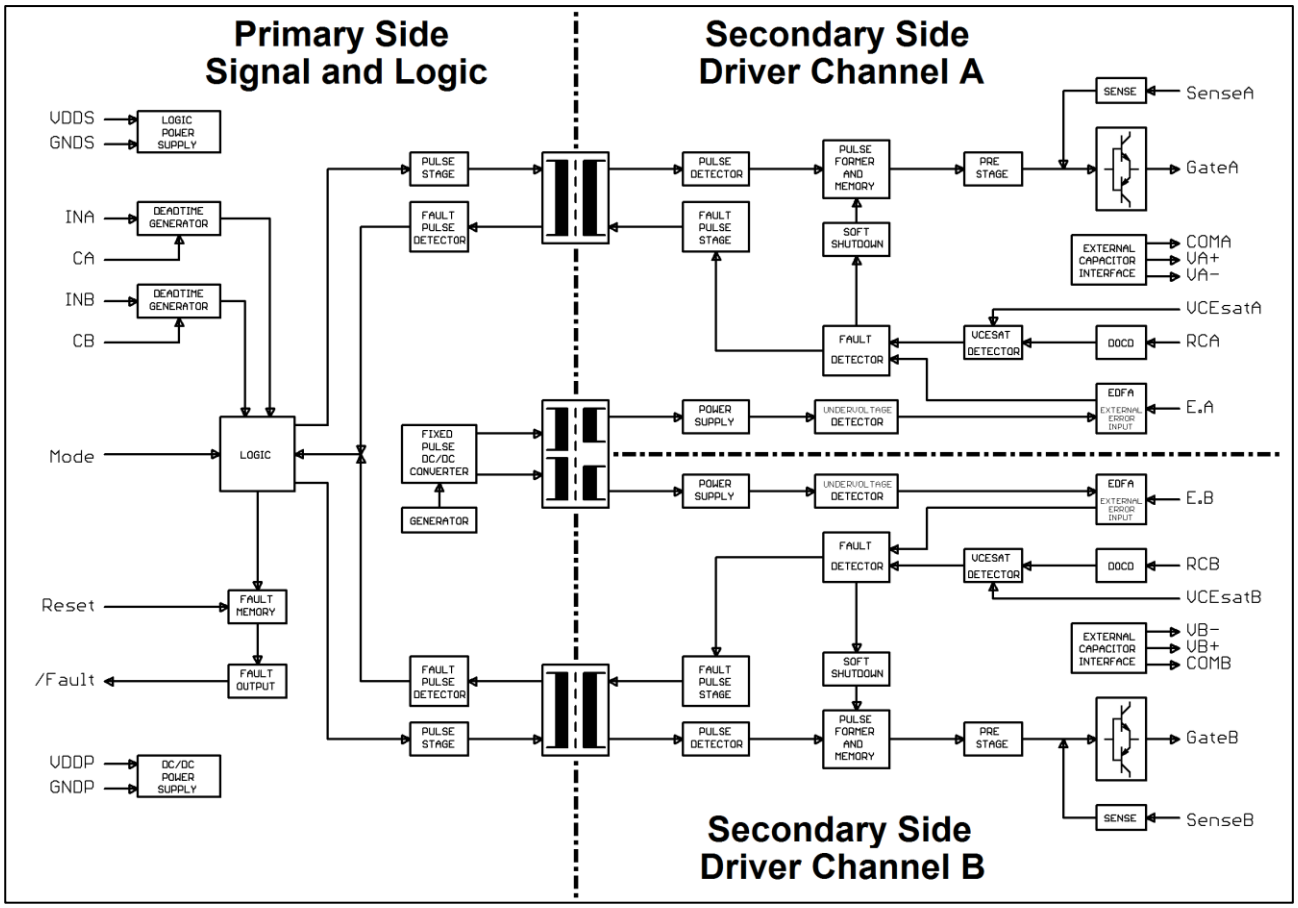

Figure 2: Block Diagram 2ED300C17-S/-ST

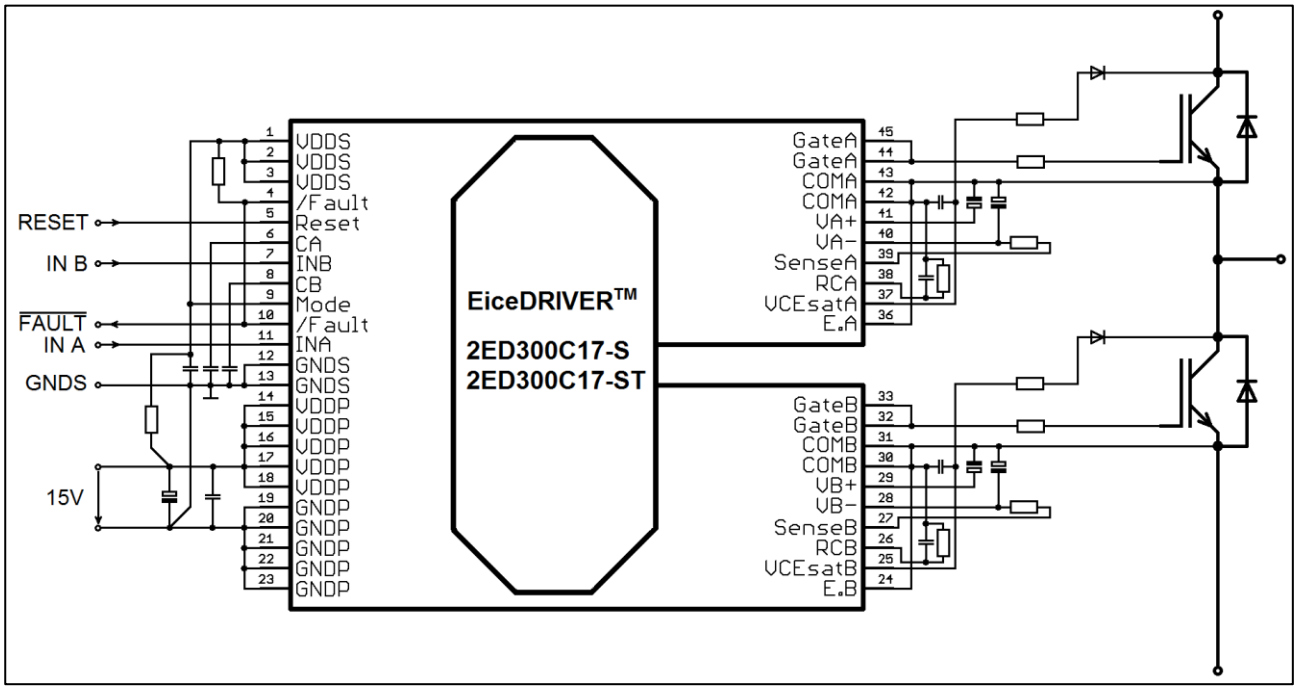

Figure 3: Peripheric components for half-bridge mode

2 Functional Description

EiceDRIVER™ (eupec IGBT controlled efficiency DRIVER) is the name of a family of IGBT-Drivers consisting of IGBT driver boards and IGBT driver ICs.

The 2ED300C17-S/-ST is a dual channel high voltage gate driver board featuring reinforced isolation between logic side and high voltage output.
Control and protection functions are included to ease the design of highly reliable systems.

The 2ED300C17-S is designed for use in industrial applications and the 2ED300C17-ST, with special coating, for the use in more demanding applications like railway traction or windmills.

The device consists of two galvanically separated driver channels and features two operating functions, the direct mode and the half-bridge mode, to drive IGBT modules.

The 2ED300C17-S/-ST is designed for use with Infineon IGBT modules up to 1700V in applications with high safety and reliability requirements and aims for power ratings of 75kW to 1MW.

The driver also includes IGBT desaturation protection, external failure input and Undervoltage Lockout (UVLO) detection. All fault states set the fault memory and activate the open drain fault output.

2.1 Reinforced Isolation

The most important safety feature of the 2ED300C17-S/-ST high voltage driver board is the reinforced isolation between primary and secondary side. This is achieved by using a specially designed transformer characterized by lowest coupling capacitances, , high isolation stability and by appropriate creepage and clearance distances on the printed circuit board. Figure 4 shows the specially transformer design for high isolation solution.

The clearance and creepage distances comply with VDE0110 and VDE0160 / EN50178 and are designed for pollution degree 3, over voltage class III. All materials used within the transformer at least meet the requirements of UL94V-2.

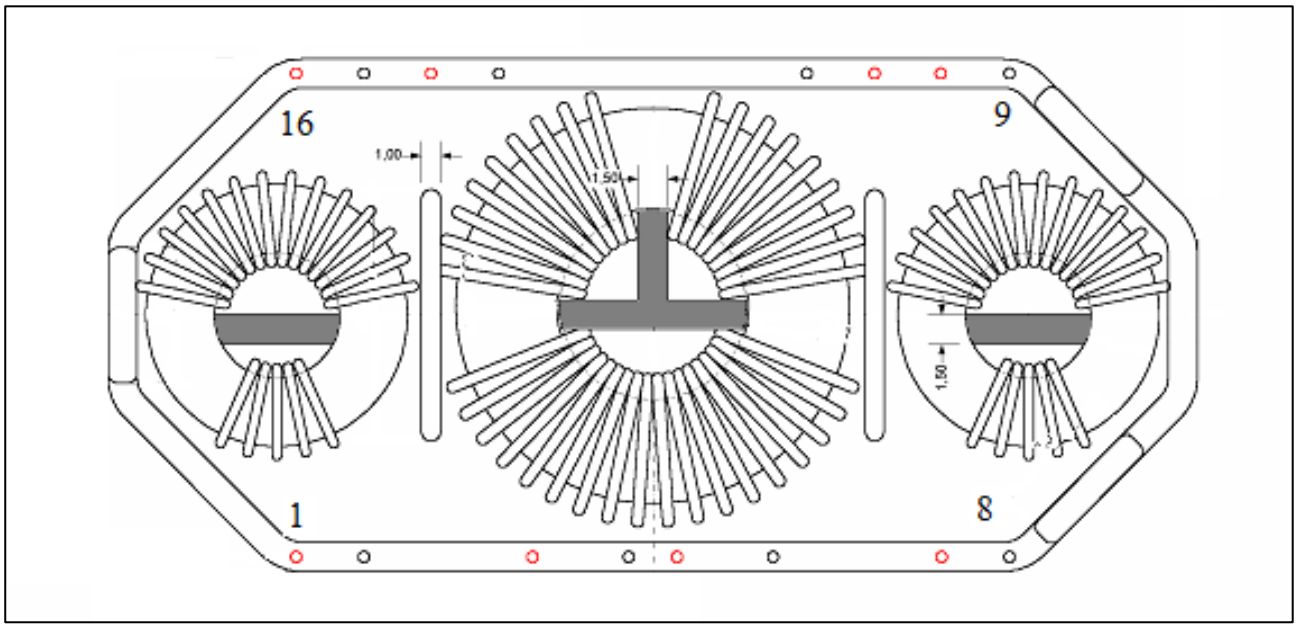

Figure 4: Additionally mechanical barriers for high isolation solution

2.2 Integrated SMPS

A switch mode power supply with galvanically separated outputs is integrated on the 2ED300C17-S/-ST. It generates the required voltages for both driver channels. The secondary supplies are not protected against external short circuit.

2.3 Undervoltage Lockout (UVLO)

Undervoltage monitoring is implemented for both secondary sides, positive and negative driver supply voltages are monitored. The Signal and Logic side is not monitored. Undervoltage lockout functionality in both driver channels ensures correct IGBT switching operation.

If the absolute value of one of the driver channel's power supplies drops below the UVLO detection level, the IGBT is shut down using the soft shut down functionality; gate-signals are ignored and the fault output is activated.

2.4 Dynamic Overcurrent Detection (DOCD)

The dynamic over current detection protects the IGBT in case of a short circuit. The saturation voltage during IGBT on-state is measured and continuously compared with a defined reference signal.

The shut down reference curve has to be adapted to each individual IGBT connecting an external RC network. If no measures are taken, the reference level for desaturation detection is approx. at 10 V. Adding an RC network allows to tune the characteristics of the detection circuit.

2.5 Soft Shut Down (SSD)

Soft shut down is a technique to limit the current slope di/dt during turn-off. It is activated if the fault memory is set as a consequence of a detected fault condition. A sense terminal can optionally be used to connect an additional external resistor. This is done to adjusting the IGBT turn-off characteristics. This terminal can optionally be used as an input for the active clamping or di/dt and dv/dt control.

2.6 External Detected Failure Analysis (EDFA)

Additional function, customizable according to individual applications such as thermo switches on heat sinks. Digital high level on these terminals set the fault memory. Soft shut down is initiated and further operation inhibited.

2.7 Reset

Resetting the driver can be done by applying a digital high level to the Reset-pin or by applying a digital low level to both gate-signal inputs for at least 60ms.On Reset, the fault memory is deleted and restarting driver operation is possible.

2.8 Control Inputs and Outputs 2ED300C17-S /-ST

Inputs of the Signal and Logic side require 15V CMOS levels according to 40xx CMOS technology. This offers a high signal to noise ratio. In very harsh environments, negative low level input signals can be used with the limits given for the maximum ratings.

The open drain fault output is a very low impedance output. Voltage levels similar to Signal and Logic ground are achieved.

3 Pin Configuration and Functionality

Pin	Label	Function
1	VDDS	Signal and logic supply voltage primary side
2		
3		
4	/Fault	Open drain fault output
5	Reset	Active high signal and logic reset input
6	CA	External capacitor terminal for half-bridge mode dead time adjustment channel A
7	INB	Active high PWM input channel B
8	CB	External capacitor terminal for half-bridge mode dead time adjustment channel B
9	Mode	Operating mode selection input
10	/Fault	Open drain fault output
11	INA	Active high PWM input channel A
12	GNDS	Signal and logic common ground primary side
13		
14	VDDP	DC/DC-SMPS supply voltage primary side
15		
16		
17		
18		
19	GNDP	DC/DC-SMPS ground primary side
20		
21		
22		
23		
24	E.B	Active high external digital fault input driver channel B
25	VCEsatB	IGBT desaturation sensing input driver channel B
26	RCB	Desaturation reference curve RC network terminal driver channel B
27	SenseB	Active clamping input or soft shut down resistor terminal driver channel B
28	VB-	External capacitor terminal for negative power supply driver channel B
29	VB+	External capacitor terminal for positive power supply driver channel B
30	COMB	Common ground terminal driver channel B
31		
32	GateB	IGBT gate output driver channel B
33		
34		Pin not existing; cut out
35		Pin not existing; cut out
36	E.A	Active high external digital fault input driver channel A
37	VCEsatA	IGBT desaturation sensing input driver channel A
38	RCA	Desaturation reference curve RC network terminal driver channel A
39	SenseA	Active clamping input or soft shut down resistor terminal driver channel A
40	VA-	External capacitor terminal for negative power supply driver channel A
41	VA+	External capacitor terminal for positive power supply driver channel A
42	COMA	Common ground terminal driver channel A
43		
44	GateA	IGBT gate output driver channel A
45		

Table 1 : Pin Configuration of 2ED300C17-S/-ST

In addition to Table 1, Figure 5 gives an overview on the pin positions.

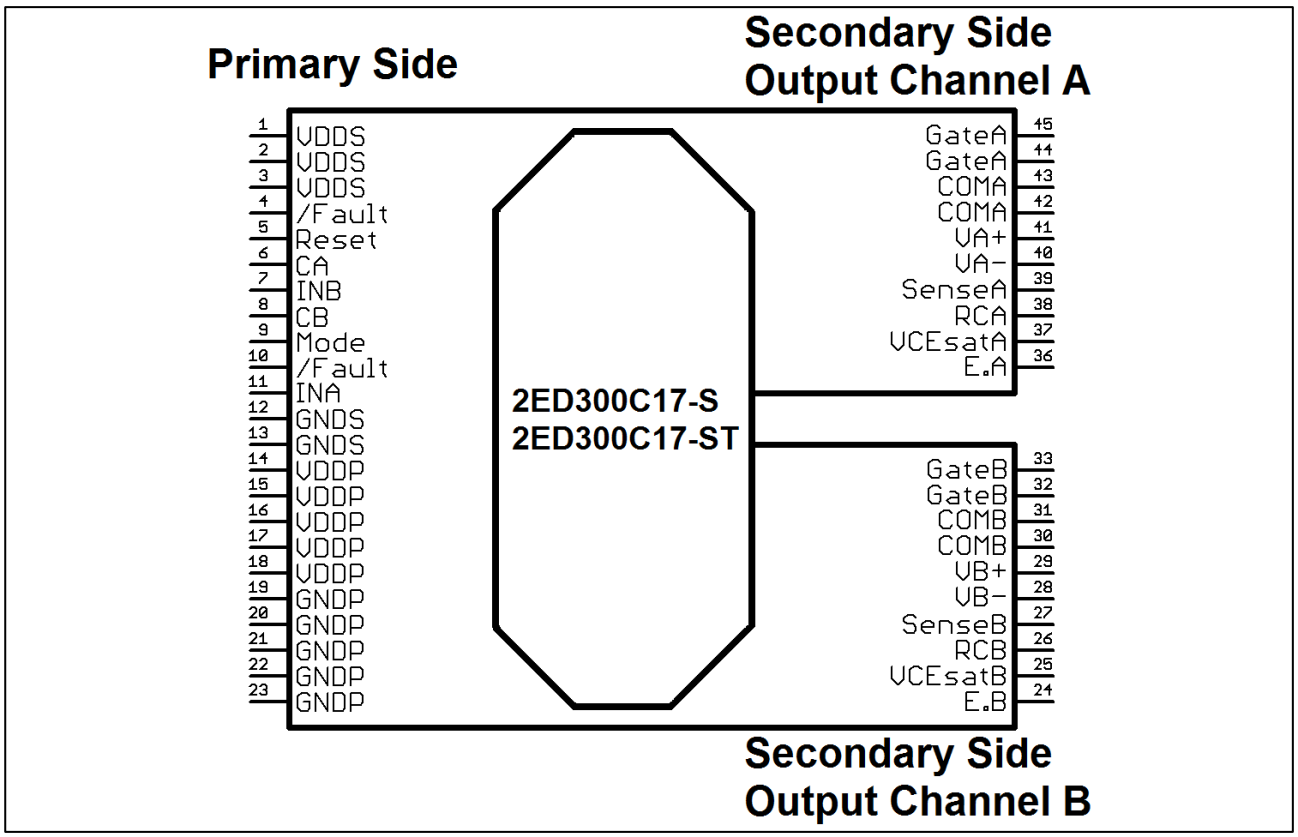

Figure 5 : EiceDRIVER™ pinning top view

3.1 Pin functionalities, Primary side

All input pins are compatible to 15V CMOS logic according to 40xx technology.

VDDS

15V supply voltage for signal and logic part on the primary side. All pins have to be connected.

/Fault

Open drain fault output for signalization of internal and external faults. Reset signal required to delete the fault memory and for restarting operation after fault state.

External pull-up resistor needed.

Reset

Active high signal to delete the fault memory.

INA

Active high signal for PWM, channel A. Negative input voltage for low level is allowed within the limits given for maximum values.

INB

Active high signal for PWM, channel B. Negative input voltage for low level is allowed within the limits given for maximum values.

CA

Terminal to connect external capacitor for dead time adjustment of channel A in half-bridge mode.

CB

Terminal to connect external capacitor for dead time adjustment of channel B in half-bridge mode.

Mode

Terminal for mode selection, choosing direct mode or half-bridge mode. High level or connection to VDDS activates half-bridge mode. Low level or connection to ground GNDS activates direct mode.

GNDS

Common ground connection for signals and supply voltage of Signal and Logic part.
All pins have to be connected.

Connection between GNDS and GNDP is permissible.

VDDP

15V supply voltage for DC/DC switch mode power supply. An external capacitor to GNDP is mandatory at this terminal.
All pins have to be connected.

GNDP

Ground connection for DC/DC switch mode power supply.
All pins have to be connected.

Connection between GNDS and GNDP is permissible.

3.2 Pin functionalities, Secondary side

GateA

Output to IGBT gate, driver channel A. Both pins have to be connected.

COMA

Common ground connection for IGBT auxiliary emitter and all signals of driver channel A. Both pins have to be connected.

VA+

Positive power supply, driver channel A. An external capacitor to ground COMA is mandatory at this terminal.

VA-

Negative power supply driver channel A. An external capacitor to ground COMA is mandatory at this terminal.

SenseA

Terminal for additional external soft shut down resistor or input for active clamping, di/dt or dv/dt control, driver channel A

RCA

Desaturation reference curve RC network terminal, driver channel A

VCEsatA

IGBT desaturation sensing input, driver channel A.

E.A

Active high external digital fault input driver channel A for set fault memory.

GateB

Output to IGBT gate, driver channel B. Both pins have to be connected.

COMB

Common ground connection for IGBT auxiliary emitter and all signals of driver channel B. Both pins have to be connected.

VB+

Positive power supply, driver channel B. An external capacitor to ground COMB is mandatory at this terminal.

VB-

Negative power supply, driver channel B. An external capacitor to ground COMB is mandatory at this terminal.

SenseB

Terminal for additional external soft shut down resistor or input for active clamping, di/dt or dv/dt control, driver channel B

RCB

Desaturation reference curve RC network terminal, driver channel B.

VCEsatB

IGBT desaturation sensing input, driver channel B.

E.B

Active high external digital fault input driver channel B for set fault memory.

4 Electrical Parameters

Electrical parameters are differentiated into maximum values that in no case are to be exceeded and operational conditions typical to the application. All parameters are listed in the following sections.

4.1 Absolute Maximum Ratings

Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the driver board. Unless otherwise noted all primary side parameters refer to GNDS. The secondary side signals from driver channel A and driver channel B are measured with respect to their individual COMA or COMB.

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Positive power supply voltage Logic and Signal	V_{VDDS}		16,5	V	[1]
Positive power supply voltage DC/DC SMPS	V_{VDDP}		16,5	V	[2]
Total input current V_{VDDS} and V_{VDDP}	$I_{VDD,sum}$		670	mA	[3]
PWM signal input voltage INA, INB	V_{INA}, V_{INB}	-20	20	V	
Logic signal input voltage Mode, Reset	V_{Mode}, V_{Reset}	-20	20	V	
Voltage on open drain fault output	V_{Fault}		20	V	
Total fault output current on one or both terminals	I_{Fault}		40	mA	
Peak turn on output current	I_{GateA}, I_{GateB}		30	A	[4]
Peak turn off output current	I_{GateA}, I_{GateB}		-30	A	[4]
DC/DC SMPS average current per output	I_{VX}		133	mA	[5]
Total DC/DC SMPS output power	P_{SMPS}		8	W	
Collector emitter voltage of IGBT	V_{CES}		1700	V	
Minimum total gate resistor	R_{Gmin}	1		Ω	
Maximum IGBT gate charge	Q_{Gmax}		52	µC	
Maximum slew rate	dvce/dt		50	kV/µs	[6]
Maximum switching frequency	f_{smax}		60	kHz	[7]
Maximum duty cycle	d_{max}		100	%	
Operating temperature 2ED300C17-S	T_{op}	-25	85	°C	[7]
Operating temperature 2ED300C17-ST	T_{op}	-40	85	°C	[7]
Storage temperature	T_{sto}	-40	85	°C	

Table 2: Absolute maximum ratings

[1] With respect to GNDS
[2] With respect to GNDP
[3] Calculated value for equivalent average DC input current @ maximum SMPS output power of 8W
[4] Maximum output current of the transistor power stage
[5] Maximum DC output current per DC/DC output voltage calculated for total SMPS power of 8W
[6] The parameter is not subject to production test – verified by design/characterization
[7] Operating temperature depends on load and environmental conditions.

4.2 Operating Parameters

Within the operating range the driver board operates as described in the functional description. Unless noted otherwise, all primary side parameters refer to GNDS. The secondary side signals from driver channel A and driver channel B are measured with respect to their individual COMA or COMB.

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Positive power supply voltage Logic and Signal	V_{VDDS}	14	16	V	
Positive power supply voltage DC/DC SMPS	V_{VDDP}	14	16	V	[8]
PWM signal input voltage INA, INB	V_{INA}, V_{INB}	-15	15	V	
Logic signal input voltage Mode, Reset	V_{Mode}, V_{Reset}	-15	15	V	
Voltage on open drain fault output in non-fault condition	V_{Fault}		16	V	
Switching frequency	f_{smax}	0	60	kHz	[9]
Duty cycle	d_{max}	0	100	%	

Table 3: Operating parameters

4.3 Recommended Operating Parameters

Unless noted otherwise, all primary side signals refer to GNDS. The secondary side signals from driver channel A and driver channel B are measured with respect to their individual COMA or COMB.

Parameter	Symbol	Value	Unit	Remarks
Positive power supply voltage logic and signal	V_{VDDS}	15	V	
Positive power supply voltage DC/DC SMPS	V_{VDDP}	15	V	[10]
PWM signal input voltage INA, INB	V_{INA}, V_{INB}	15	V	
Logic signal input voltage Mode, Reset	V_{Mode}, V_{Reset}	15	V	
Voltage on open drain fault output in non-fault condition	V_{Fault}	15	V	
Switching frequency @ 65°C operating temperature	f_{smax}	60	kHz	[11]

Table 4: Recommended operating parameters

[8] With respect to GNDP
[9] Operating temperature depends on load and environmental conditions.
[10] With respect to GNDP
[11] Operating temperature depends on load and environmental conditions.

4.4 Electrical Characteristics

The electrical characteristics involve the spread of values for the supply voltages, load and junction temperatures given below. Typical values represent the median values, which are related to production processes at T = 25°C. V_{VDDS} and V_{VDDP} are 15V. Unless otherwise noted all voltages are given with respect to GNDS. The specification for all output driver signals is valid for driver channel A and driver channel B without special notice. The secondary signals are measured with respect to their individual COMA or COMB.

Parameter	Symbol	Limit Values			Unit	Remarks
		min	typ	max		
No load SMPS average DC input current	I_{VDDS}		80		mA	
Signal and Logic DC input current	I_{VDDP}		10		mA	
Turn on propagation delay time	$t_{pd,on}$		670		ns	
Turn off propagation delay time	$t_{pd,off}$		580		ns	
Transition time differences	t_{dif}		50		ns	
Minimal pulse suppression	t_{md}		400		ns	
DC input impedance of INA, INB, Mode, Reset			3300		Ω	
Input threshold level	V_{INA}, V_{INB}		8		V	
Input threshold for external failure input E.A or E.B	$V_{E.A}$, $V_{E.B}$		5		V	[12]
Interlock delay time half-bridge mode	t_{TD}	1,6			µs	
Reactivation after fault condition @ INA and INB with low input signal	t_{react}	50	60		ms	
Reference voltage for IGBT desaturation sensing			10		V	
Coupling capacitance primary/secondary	C_{cps}		18		pF	
Coupling capacitance between secondary sides	C_{css}		15		pF	
External capacitor for Logic and Signal power supply. Connected between VDDS and GNDS.	C_{VDDP}	10			µF	
External capacitor for SMPS power supply. Connected between VDDP and GNDP.	C_{VDDS}	470			µF	
Positive supply voltage driver channel A and B @ no switching operation	V_{VA+}, V_{VB+}		16		V	
Negative supply voltage driver channel A and B @ no switching operation	V_{VA-}, V_{VB-}		-16		V	
Internal capacitor on positive supply voltage driver channel VA+ and VB+	$C_{VA+,int}$, $C_{VB+,int}$		28		µF	
Internal capacitor on negative supply voltage driver channel VA- and VB-	$C_{VA-,int}$, $C_{VB-,int}$		23		µF	
Internal UVLO level for positive supply voltage driver channel	$V_{UVLO,pos}$		10,9		V	
Internal UVLO level for negative supply voltage driver channel	$V_{UVLO,neg}$		-9,3		V	
External capacitor for interlocking generation	C_{CA}, C_{CB}	0		1	nF	[13]

Table 5: Electrical characteristics

[12] If not use E.A and E.B should be connected to COMA or COMB

[13] Capacitor terminal only. Connection to another terminals or voltages not allowed.

4.5 Driver performance

The 2ED300C17-S can transmit a maximum power of 4 W per channel from primary to secondary side. The power required to drive an IGBT is dependent of gate charge of the IGBT (datasheet value Q_G), switching frequency f_s and gate voltage difference ΔV. The safety factor 1.2 included 20% over all tolerances. The power for IGBT drive may be calculated by the following equation:

$$P_{driver} = 1.2 * Q_G * f_s * \Delta V$$

This power is dissipated in the driver itself, in the external gate resistor and in the internal IGBT gate resistor.

The share of the total power each part has to dissipate varies with load conditions. There is a limit for the power dissipation of each channel of the driver which significantly varies with temperature inside the cabinet and with airflow conditions. Figure 6 shows the usable driver output power for a typical mounting condition with natural connection and several load conditions. Required gate power is considered to be constant.
The highest share of power dissipation inside the driver is to be expected when operating a small IGBT with low total R_G at high switching frequency. Whereas driving a larger IGBT with higher R_G at low switching frequency is less demanding regarding thermal considerations.

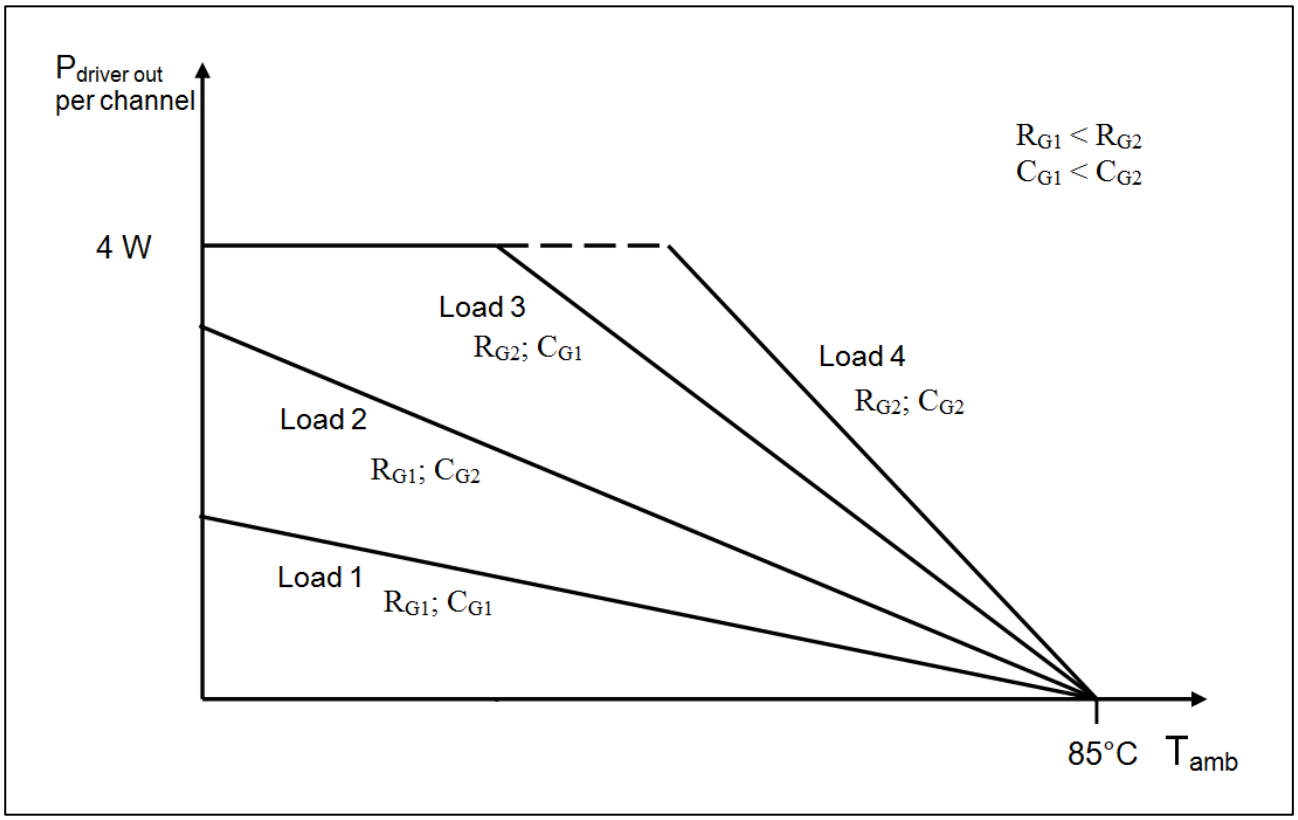

Figure 6: Power dissipation of the driver for different load conditions

Load 1 > load 2 > load 3 > load 4

Load 1 – small R_G and small C_G
Load 2 – small R_G and high C_G
Load 3 – high R_G and small C_G
Load 4 – high R_G and high C_G

The load is a combination of the gate resistors and the gate capacitance.

4.6 VCESAT reference

The short circuit detection measurement is integrated in the 2ED300C17-S. The 2ED300C17-S measures the V_{CE} voltage while the IGBT is turned on. If the V_{CE} voltage rises above the preset reference voltage during this period, a fault is triggered and the IGBT is turned off via the internal soft shut-down.

The reference curve is only adjustable via an external R_{SX} and C_{SX}. R_{SX} sets the reference voltage and C_{SX} sets the time constant for the decay to the stationary reference value.

The resistor and the capacitor are connected parallel between RC A and COM A or RC B and COM B.

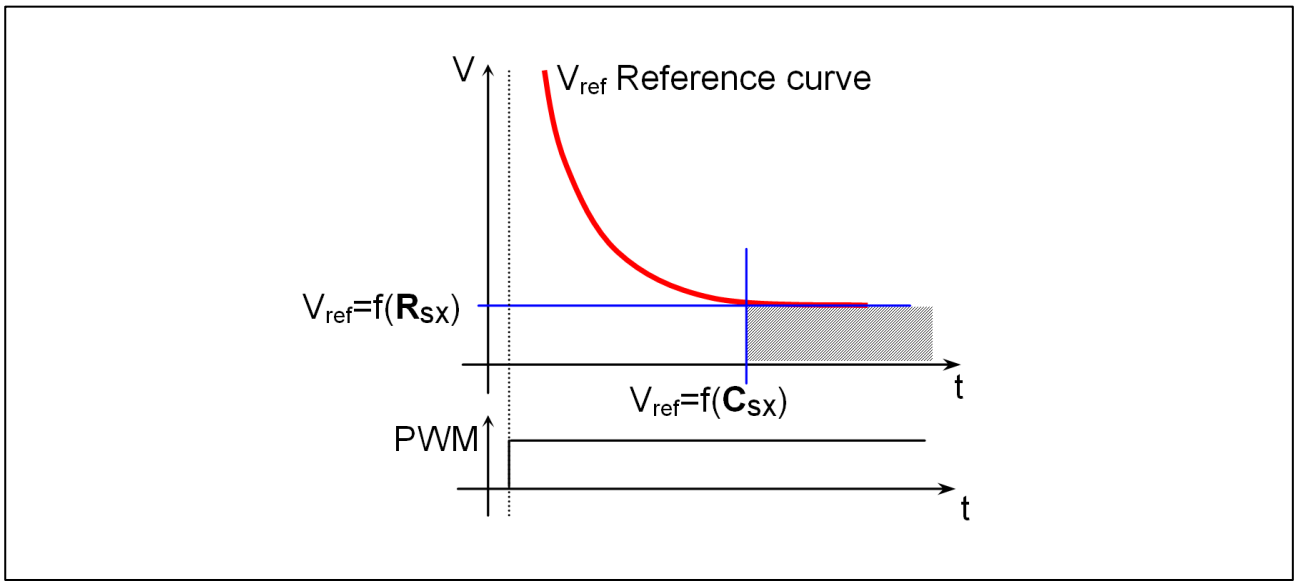

Figure 7: Vce,sat reference curve

5 Isolation characteristics

Electrical characteristics, at Ta = 25 °C, unless otherwise specified.

Parameter	Value	Unit	Remarks
Isolation test voltage	5000	V	Signal and Logic Side - Driver Channel A and Driver Channel B (RMS, 50Hz, 1s)
Isolation test voltage	2250	V	Driver Channel A - Driver Channel B (RMS, 50Hz, 1s)
Surge voltage test	9600	V	Surge test according to EN50178 Signal and Logic Side to Driver Channels A and B
Partial discharge test voltage	>1920	V	RMS; transformer series test According to EN 61800-5-1
Clearance and creepage distance primary to secondary	>15	mm	Distance Signal and Logic Side to Driver Channels A and B
Clearance distance secondary to secondary	>4,59	mm	Distance Driver Channel A to Driver Channel B. 4mm air gap included.
Creepage distance secondary to secondary	>14	mm	Distance Driver Channel A to Driver Channel B

Table 6: Isolation characteristics

6 Timing diagrams

Diagram in Figure 8 shows typical input and output signals. Figure 9 shows propagation delay times.

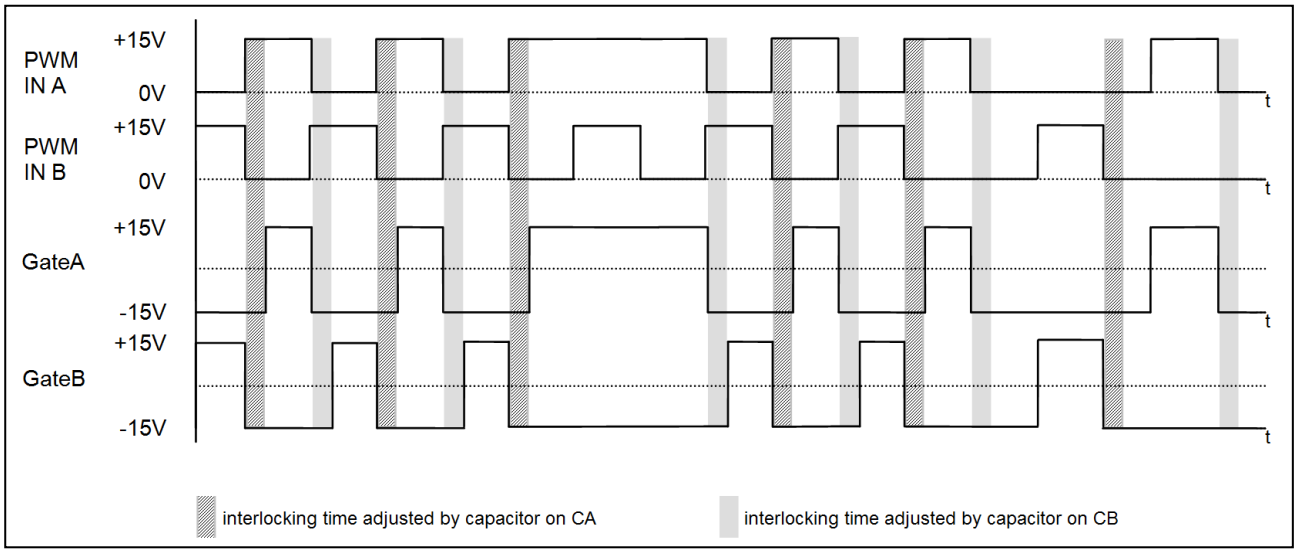

Figure 8: PWM timing diagram with interlocking time functionality

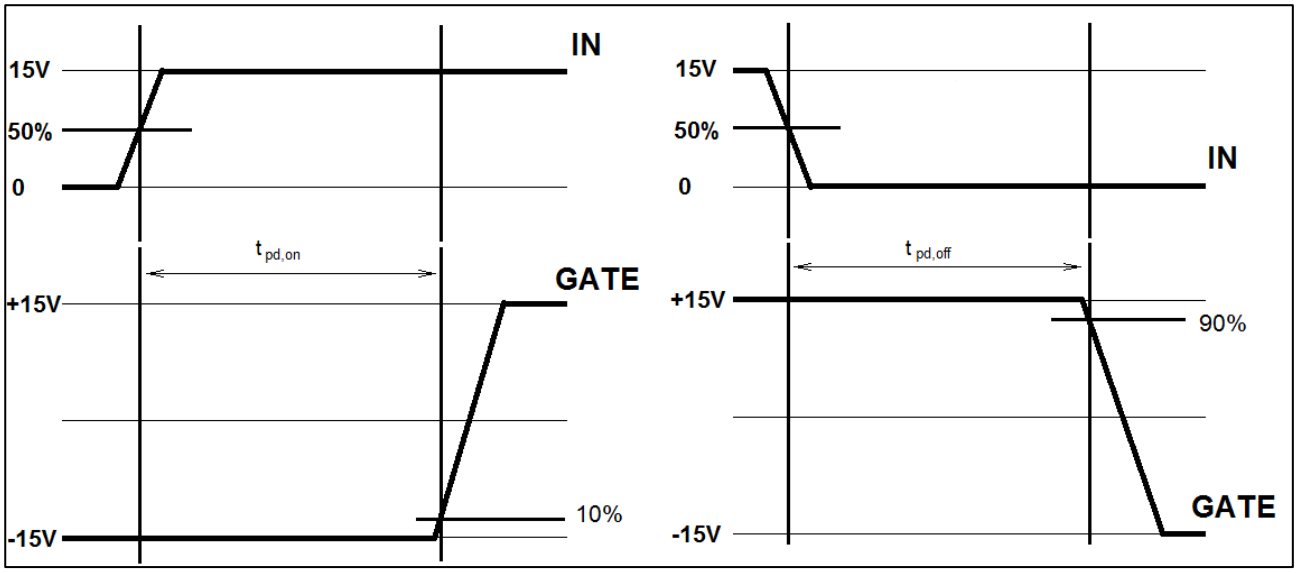

Figure 9: Propagation delay times

7 Mechanical dimensions

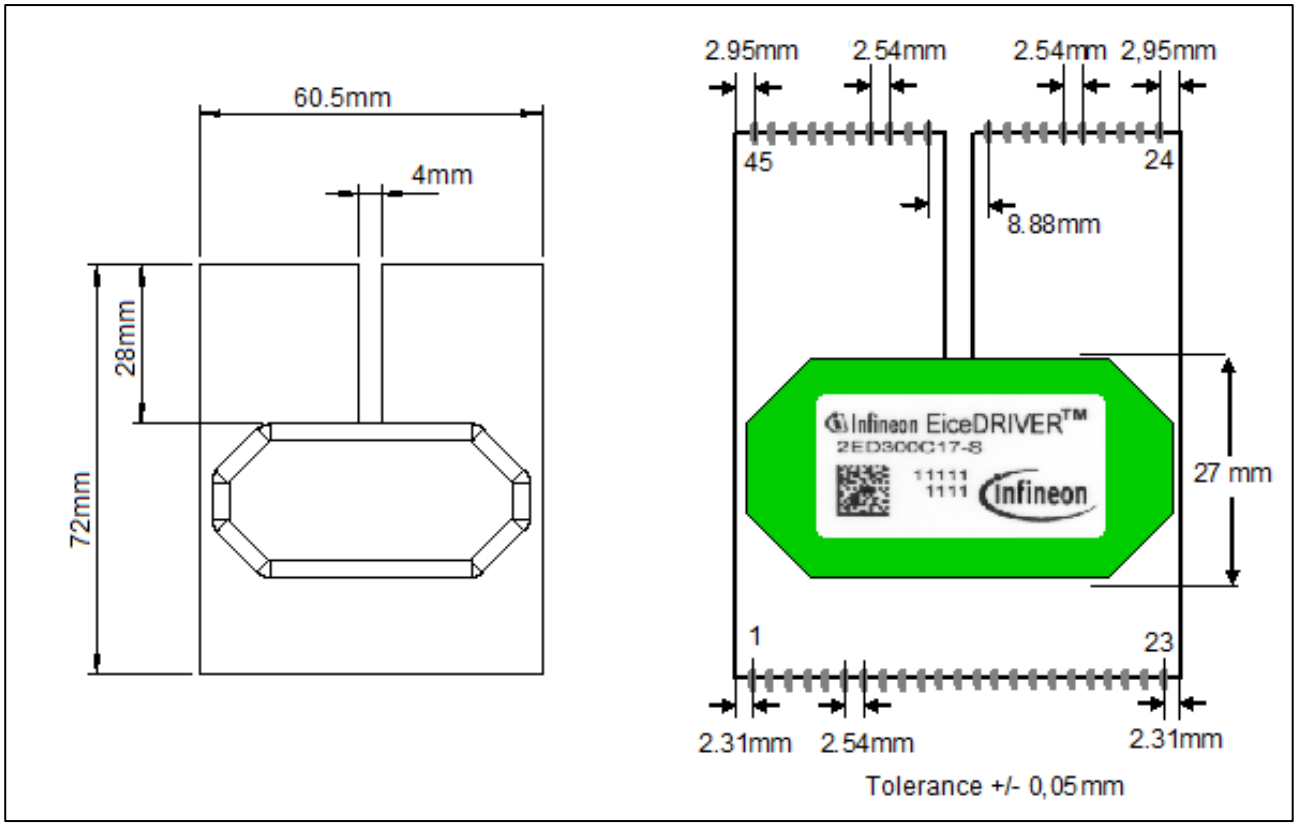

Figure 10: Package outlines top view

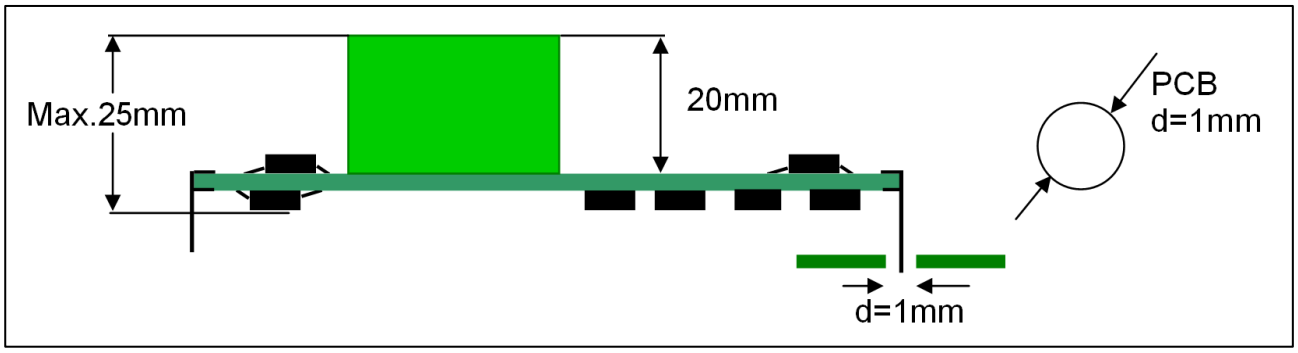

Figure 11: Package outlines side view

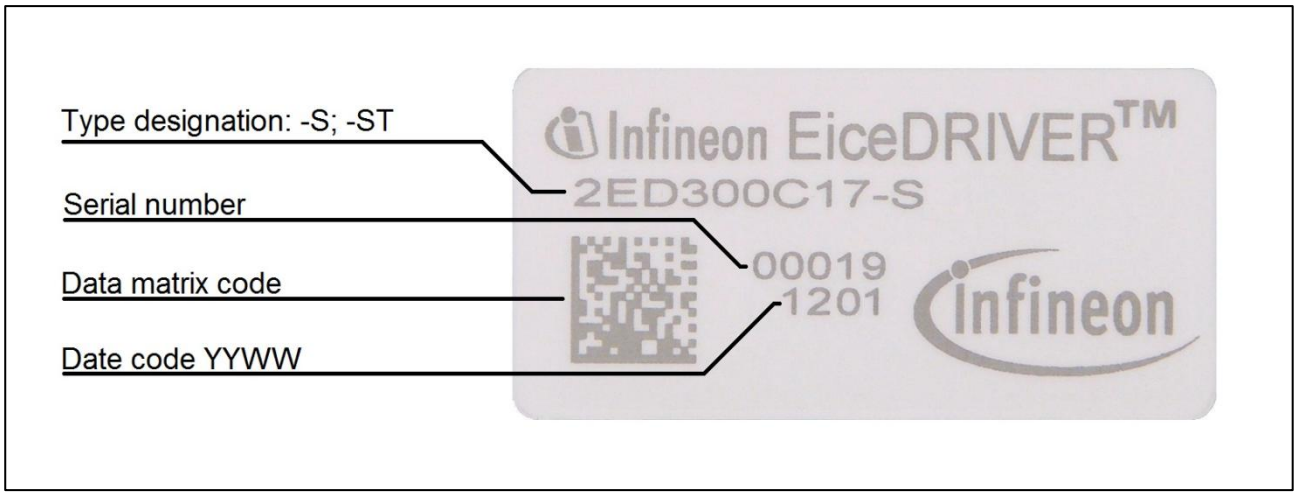

Figure 12: Label

Intent of DMX Code	DMX Code	DMX Code
	digit	digit quantity
Serial Number	1-5	5
SAP Material Number	6-11	6
Internal Production Order Number	12-19	8
Datecode (Production Year)	20-21	2
Datecode (Production Week)	22-23	2

Table 7: Intent of DMX code

8 Handling and mounting

The device has been designed to be soldered onto a carrier board as a through-hole component. Dual wave soldering process or selective soldering can be done. For more information see IFX Additional Information, DS1, March 2008

The -ST version differentiates from the -S as it features an additional coating. The coating used is type 1306N made by the company Peters. The soldering pins are not coated. When further coating processes are done on the customer assembly, the compatibility of the coated type has to be established first.

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