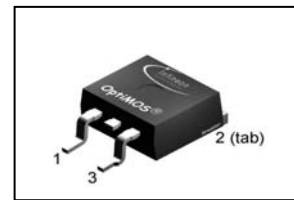


**OptiMOS® Power-Transistor**
**Features**

- N-channel Logic Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green package (lead free)
- Ultra low Rds(on)
- 100% Avalanche tested

**Product Summary**

$V_{DS}$	75	V
$R_{DS(on),max}$	20.5	mΩ
$I_D$	30	A

**PG-TO252-3-11**


Type	Package	Marking
IPD30N08S2L-21	PG-TO252-3-11	2N08L21


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	$I_D$	$T_C=25\text{ °C}, V_{GS}=10\text{ V}^{1)}$	30	A
		$T_C=100\text{ °C}, V_{GS}=10\text{ V}^{2)}$	30	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	120	
Avalanche energy, single pulse	$E_{AS}$	$I_D=30\text{ A}$	240	mJ
Gate source voltage	$V_{GS}$		±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	136	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
<b>Thermal characteristics<sup>2)</sup></b>						
Thermal resistance, junction - case	$R_{thJC}$		-	-	1.1	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$		-	-	100	
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	75	
		6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	-	50	

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	75	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=80\text{ }\mu\text{A}$	1.2	1.6	2.0	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	0.01	1	$\mu\text{A}$
		$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ }^\circ\text{C}^{2)}$	-	1	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=25\text{ A}$	-	20.6	26	m $\Omega$
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=25\text{ A}$	-	15.9	20.5	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	1650	-	pF
Output capacitance	$C_{oss}$		-	400	-	
Reverse transfer capacitance	$C_{rss}$		-	190	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=30\text{ A}, R_G=3.9\ \Omega$	-	9	-	ns
Rise time	$t_r$		-	30	-	
Turn-off delay time	$t_{d(off)}$		-	44	-	
Fall time	$t_f$		-	11	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=60\text{ V}, I_D=30\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	6	6.8	nC
Gate to drain charge	$Q_{gd}$		-	22	32	
Gate charge total	$Q_g$		-	56	72	
Gate plateau voltage	$V_{plateau}$		-	3.5	-	V

**Reverse Diode**

Diode continuous forward current <sup>2)</sup>	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	30	A
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$		-	-	120	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=30\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time <sup>2)</sup>	$t_{rr}$	$V_R=40\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	50	-	ns
Reverse recovery charge <sup>2)</sup>	$Q_{rr}$	$V_R=40\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	120	-	nC

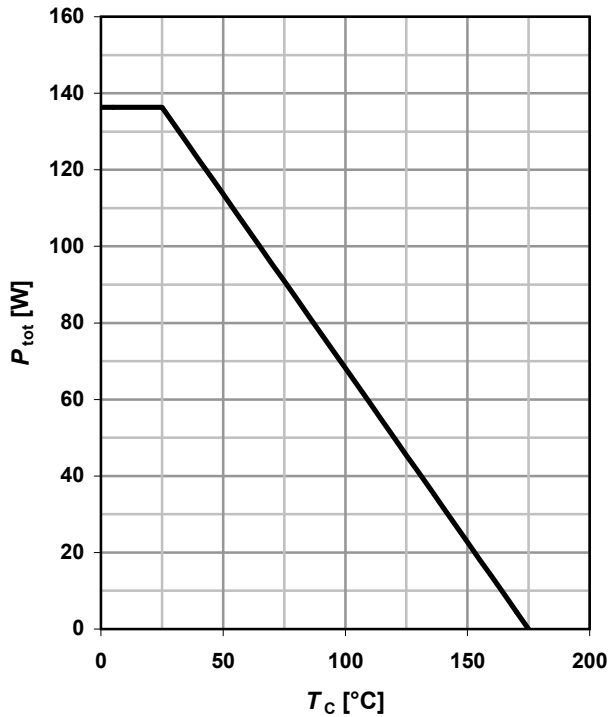
<sup>1)</sup> Current limited by bondwire; with an  $R_{thJC} = 1.1\text{ K/W}$  the chip is able to carry  $I_D = 54\text{ A}$  at  $25^\circ\text{C}$ , for detailed information see app.-note ANPS071E available at [www.infineon.com/optimos](http://www.infineon.com/optimos)

<sup>2)</sup> Defined by design. Not subject to production test.

<sup>3)</sup> Device on  $40\text{ mm} \times 40\text{ mm} \times 1.5\text{ mm}$  epoxy PCB FR4 with  $6\text{ cm}^2$  (one layer,  $70\ \mu\text{m}$  thick) copper area for drain connection. PCB is vertical in still air.

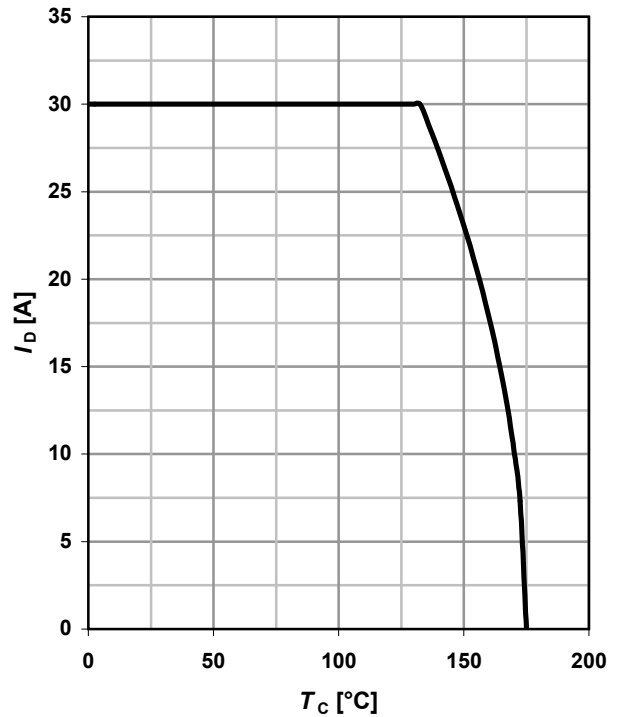
### 1 Power dissipation

$$P_{\text{tot}} = f(T_C); V_{\text{GS}} \geq 6 \text{ V}$$



### 2 Drain current

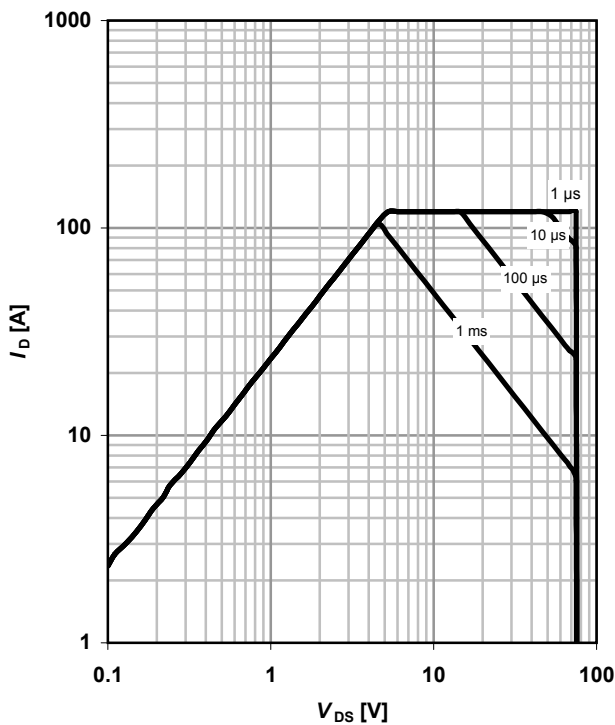
$$I_D = f(T_C); V_{\text{GS}} \geq 10 \text{ V}$$



### 3 Safe operating area

$$I_D = f(V_{\text{DS}}); T_C = 25 \text{ °C}; D = 0$$

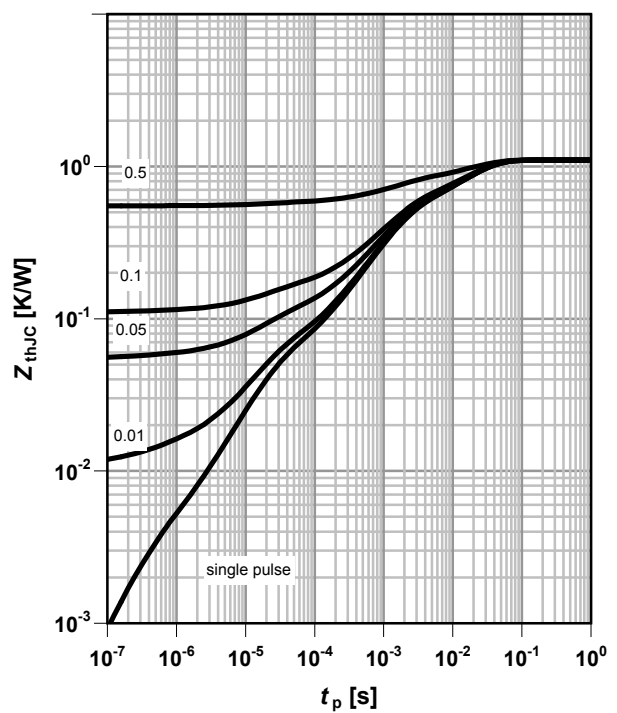
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{\text{thJC}} = f(t_p)$$

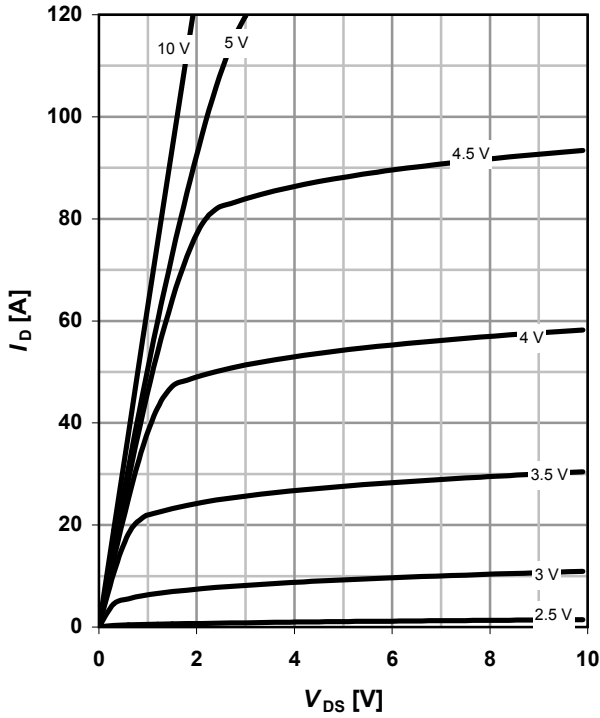
parameter:  $D = t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

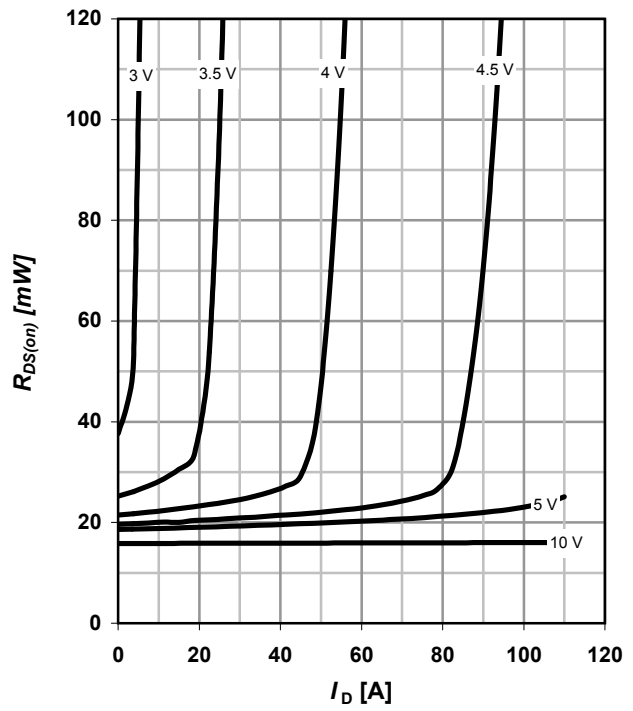
parameter:  $V_{GS}$



**6 Typ. drain-source on-state resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

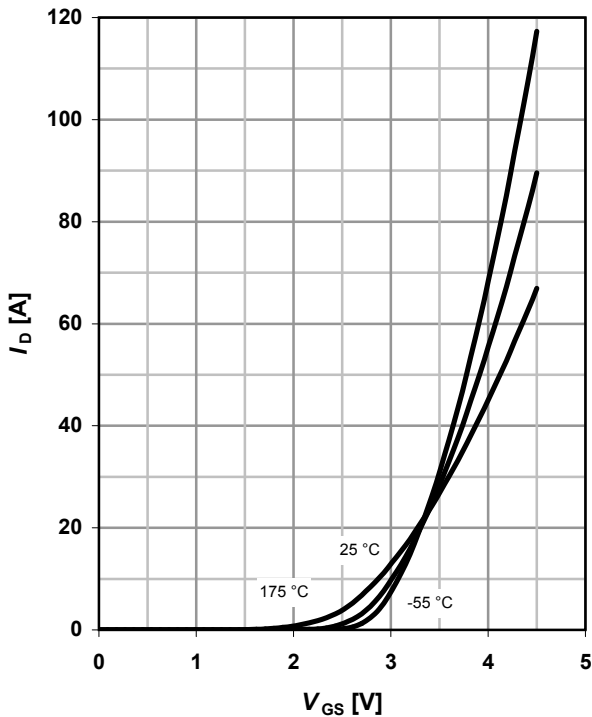
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} = 6\text{V}$

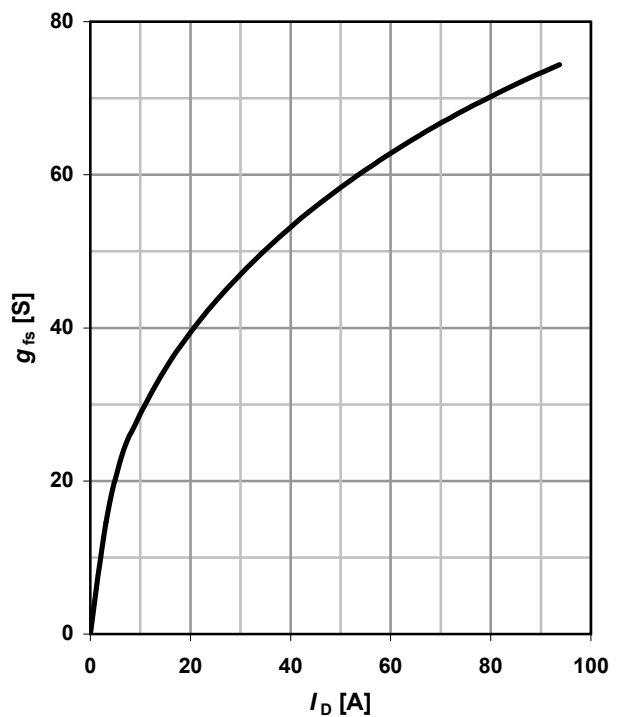
parameter:  $T_j$



**8 Typ. Forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

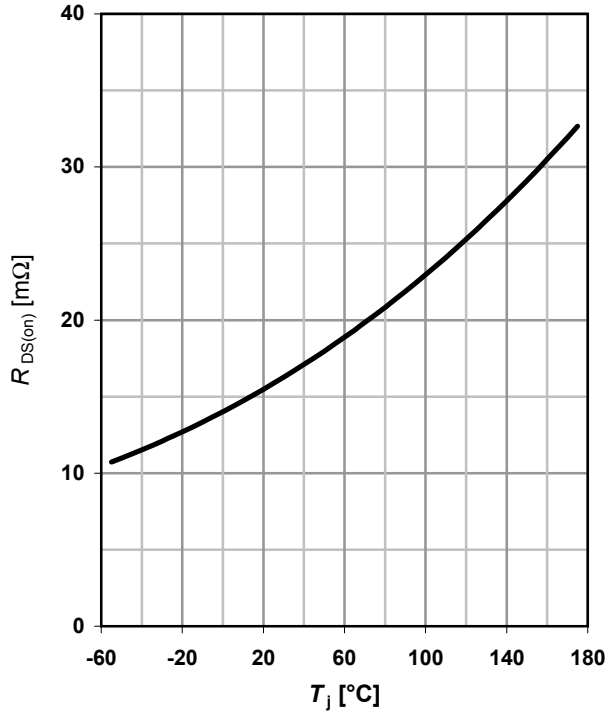
parameter:  $g_{fs}$



**9 Typ. Drain-source on-state resistance**

$R_{DS(on)} = f(T_j)$

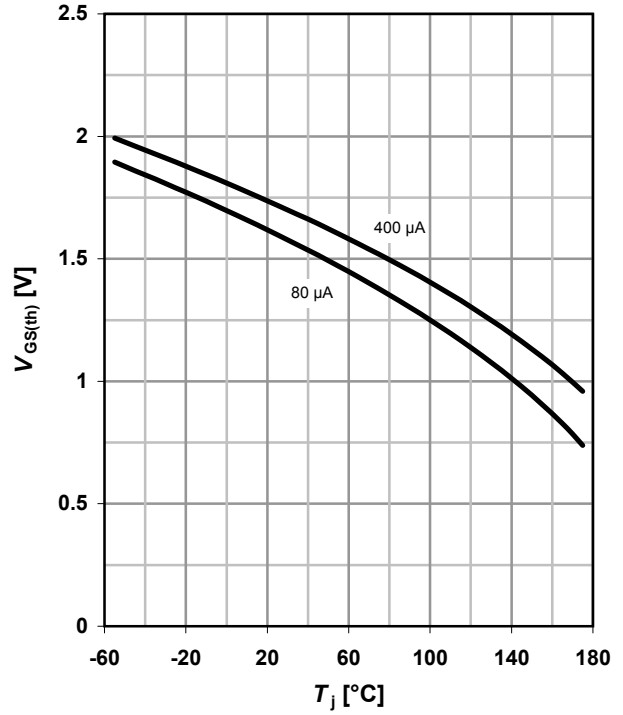
parameter:  $I_D = 25\text{ A}$ ;  $V_{GS} = 10\text{ V}$



**10 Typ. gate threshold voltage**

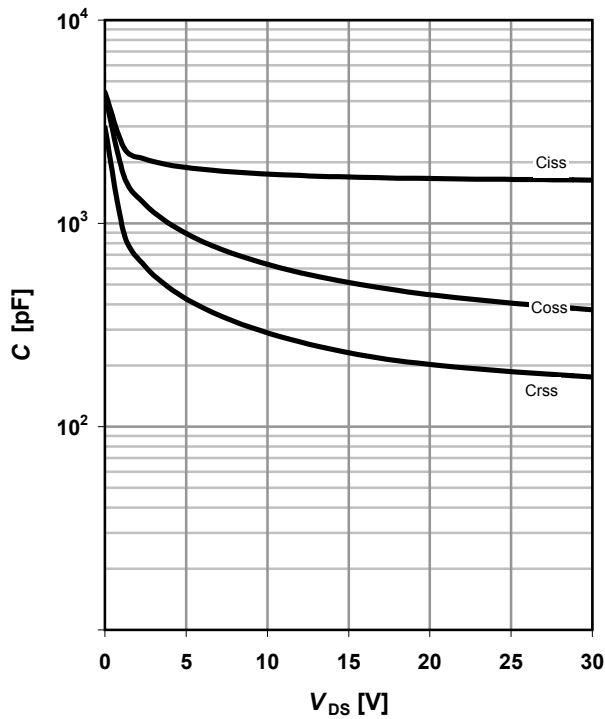
$V_{GS(th)} = f(T_j)$ ;  $V_{GS} = V_{DS}$

parameter:  $I_D$



**11 Typ. capacitances**

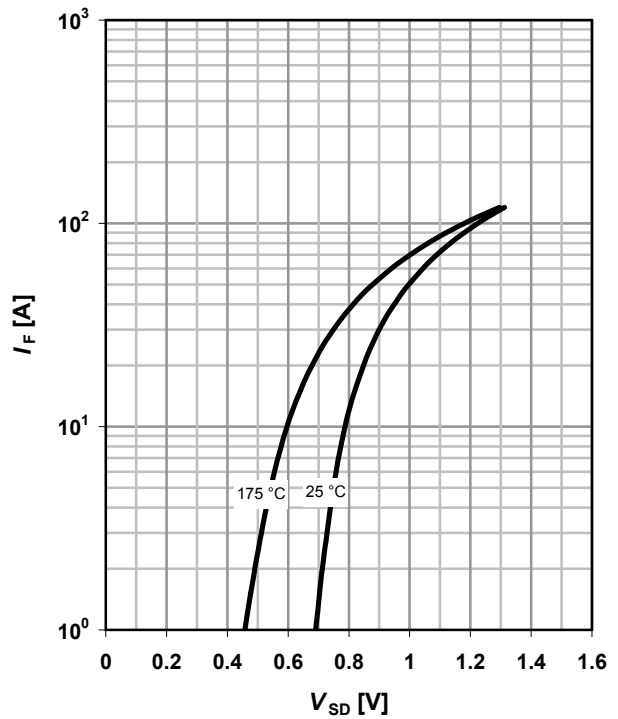
$C = f(V_{DS})$ ;  $V_{GS} = 0\text{ V}$ ;  $f = 1\text{ MHz}$



**12 Typical forward diode characteristics**

$I_F = f(V_{SD})$

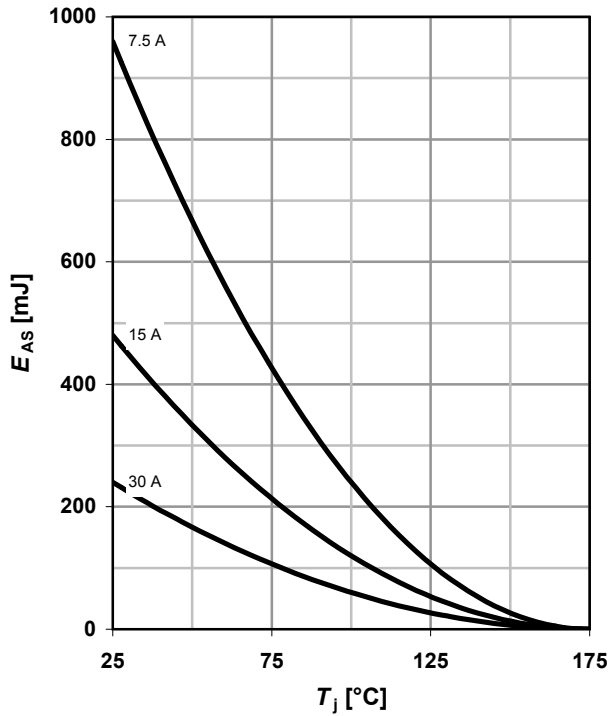
parameter:  $T_j$



**13 Typical avalanche energy**

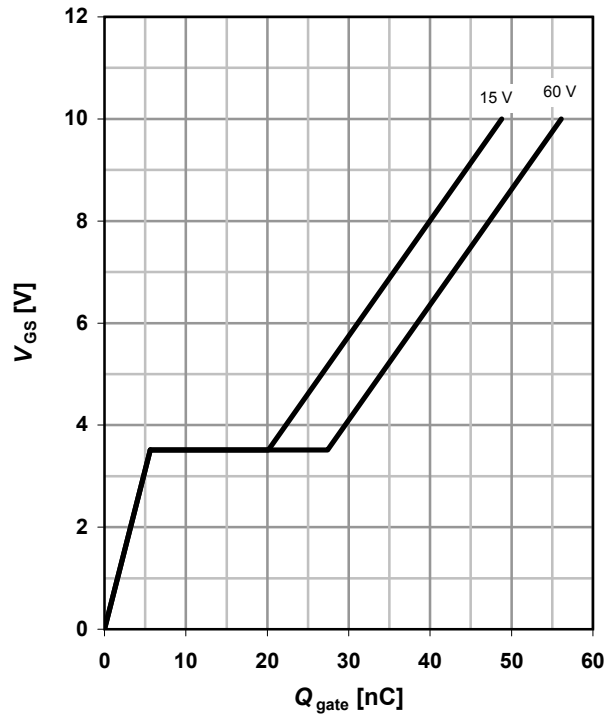
$$E_{AS} = f(T_j)$$

parameter:  $I_D$



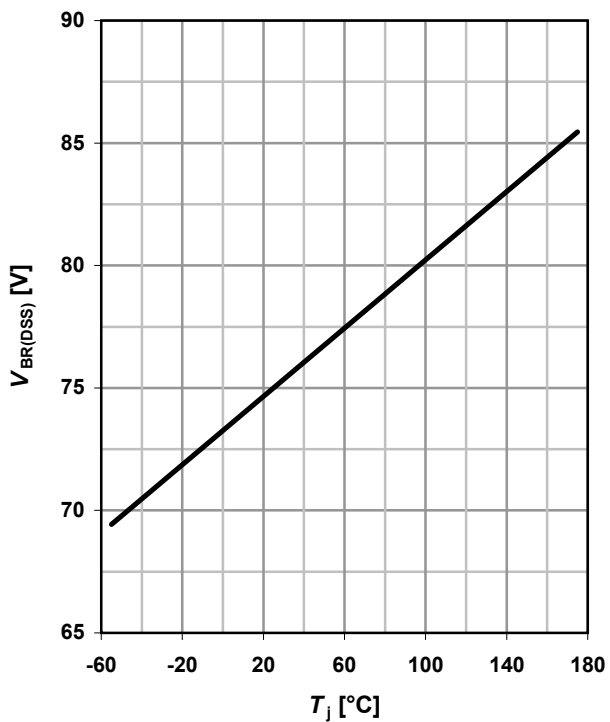
**14 Typ. gate charge**

$$V_{GS} = f(Q_{gate}); I_D = 30 \text{ A pulsed}$$

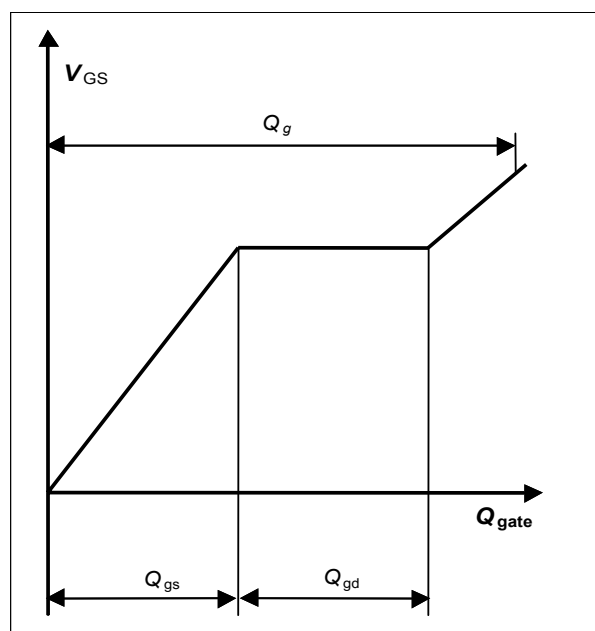


**15 Typ. drain-source breakdown voltage**

$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



**16 Gate charge waveforms**



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