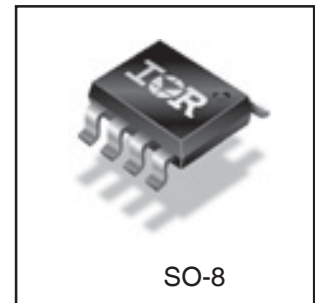
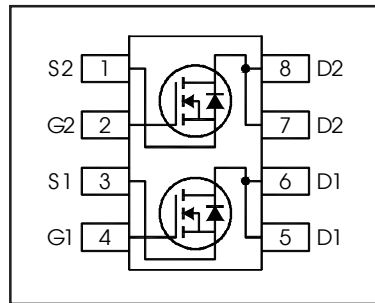


HEXFET® Power MOSFET

V_{DS}	30	V
$R_{DS(on) \max} Q1$ (@ $V_{GS} = 10V$)	16.4	m Ω
$R_{DS(on) \max} Q2$ (@ $V_{GS} = 10V$)	11.8	
Q_g (typical) Q1	6.7	nC
Q_g (typical) Q2	14	
I_D (@ $T_A = 25^\circ C$) Q1	9.1	A
I_D (@ $T_A = 25^\circ C$) Q2	11	



Applications

- Dual SO-8 MOSFET for POL Converters in Notebook Computers, Servers, Graphics Cards, Game Consoles and Set-Top Box

Features

Industry-standard pinout SO-8 Package
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1, Industrial qualification



Benefits

Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF7907PbF-1	SO-8	Tape and Reel	4000	IRF7907TRPbF-1

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{DS}	Drain-to-Source Voltage	30		V
V_{GS}	Gate-to-Source Voltage	± 20		
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	9.1	11	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	7.3	8.8	
I_{DM}	Pulsed Drain Current ①	76	85	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.0	2.0	W
$P_D @ T_A = 70^\circ C$	Power Dissipation	1.3	1.3	
	Linear Derating Factor	0.016	0.016	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead ⑤	42	42	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	62.5	62.5	

Notes ① through ⑤ are on page 11.

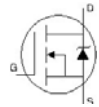
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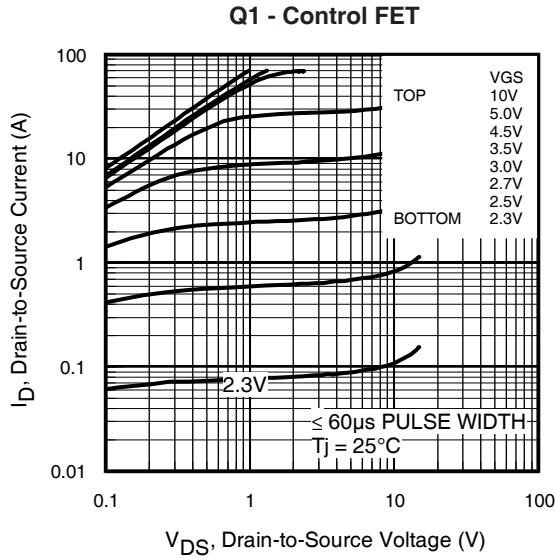
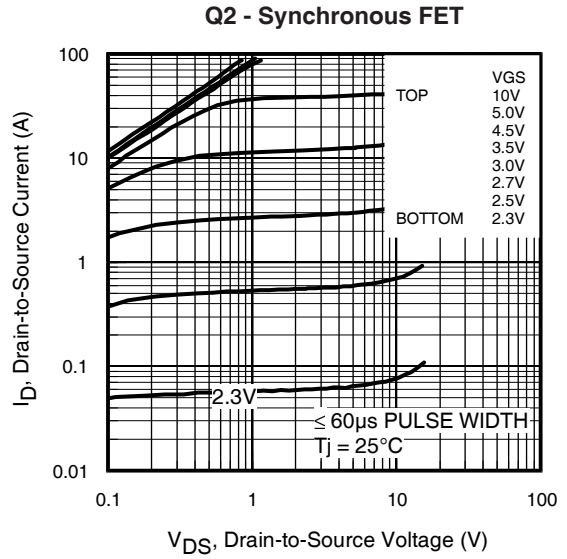
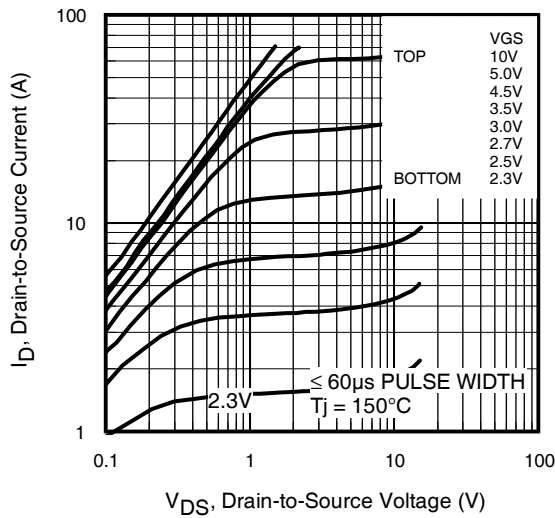
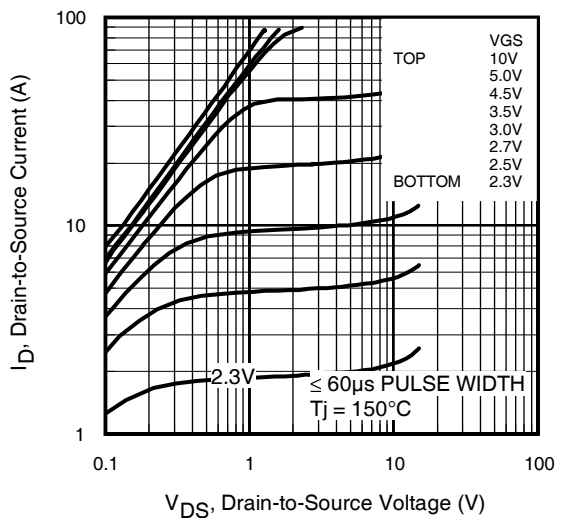
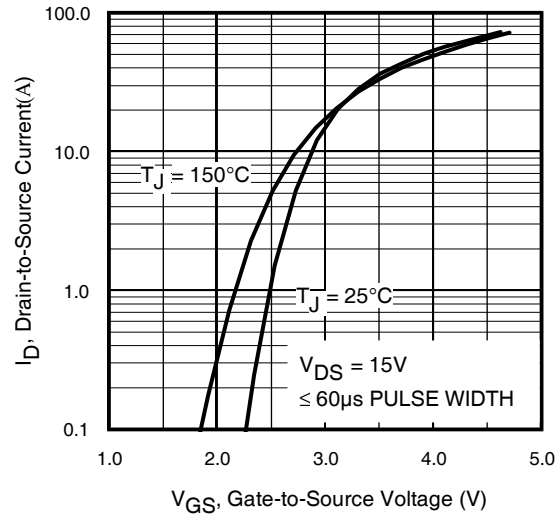
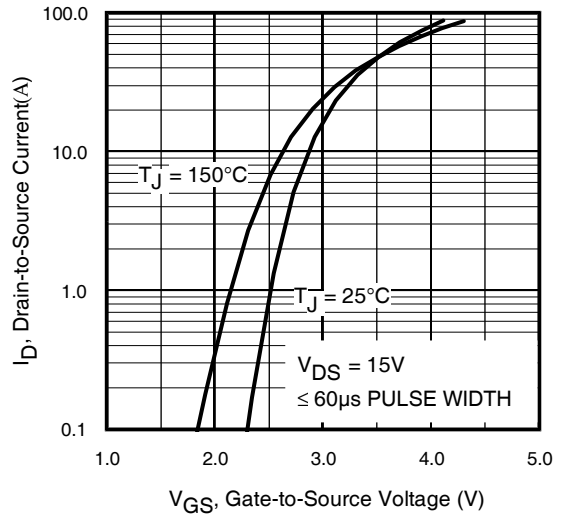
	Parameter		Min.	Typ.	Max.	Units	Conditions		
BV _{DSS}	Drain-to-Source Breakdown Voltage	Q1&Q2	30	—	—	V	V _{GS} = 0V, I _D = 250μA		
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	Q1	—	0.024	—	V/°C	Reference to 25°C, I _D = 1mA		
		Q2	—	0.024	—				
R _{DS(on)}	Static Drain-to-Source On-Resistance	Q1	—	13.7	16.4	mΩ	V _{GS} = 10V, I _D = 9.1A ③		
			—	17.1	20.5		V _{GS} = 4.5V, I _D = 7.3A ③		
		Q2	—	9.8	11.8		V _{GS} = 10V, I _D = 11A ③		
			—	11.5	13.7		V _{GS} = 4.5V, I _D = 8.8A ③		
V _{GS(th)}	Gate Threshold Voltage	Q1&Q2	1.35	1.8	2.35	V	Q1: V _{DS} = V _{GS} , I _D = 25μA		
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	Q1	—	-4.6	—	mV/°C	Q2: V _{DS} = V _{GS} , I _D = 50μA		
		Q2	—	-4.9	—				
I _{DSS}	Drain-to-Source Leakage Current	Q1&Q2	—	—	1.0	μA	V _{DS} = 24V, V _{GS} = 0V		
		Q1&Q2	—	—	150		V _{DS} = 24V, V _{GS} = 0V, T _J = 125°C		
I _{GSS}	Gate-to-Source Forward Leakage	Q1&Q2	—	—	100	nA	V _{GS} = 20V		
	Gate-to-Source Reverse Leakage	Q1&Q2	—	—	-100		V _{GS} = -20V		
g _{fs}	Forward Transconductance	Q1	19	—	—	S	V _{DS} = 15V, I _D = 7.0A		
		Q2	24	—	—		V _{DS} = 15V, I _D = 8.8A		
Q _g	Total Gate Charge	Q1	—	6.7	10	nC	Q1 V _{DS} = 15V V _{GS} = 4.5V, I _D = 7.0A Q2 V _{DS} = 15V V _{GS} = 4.5V, I _D = 8.8A		
		Q2	—	14	21				
Q _{gs1}	Pre-V _{th} Gate-to-Source Charge	Q1	—	1.3	—				
		Q2	—	3.0	—				
Q _{gs2}	Post-V _{th} Gate-to-Source Charge	Q1	—	0.7	—				
		Q2	—	1.3	—				
Q _{gd}	Gate-to-Drain Charge	Q1	—	2.5	—				
		Q2	—	4.9	—				
Q _{godr}	Gate Charge Overdrive	Q1	—	2.2	—				
		Q2	—	4.8	—				
Q _{sw}	Switch Charge (Q _{gs2} + Q _{gd})	Q1	—	3.2	—				
		Q2	—	6.2	—				
Q _{oss}	Output Charge	Q1	—	4.5	—			nC	V _{DS} = 16V, V _{GS} = 0V
		Q2	—	9.0	—				
R _G	Gate Resistance	Q1	—	2.6	4.7	Ω			
		Q2	—	3.0	5.0				
t _{d(on)}	Turn-On Delay Time	Q1	—	6.0	—	ns	Q1 V _{DD} = 15V, V _{GS} = 4.5V I _D = 7.0A Q2 V _{DD} = 15V, V _{GS} = 4.5V I _D = 8.8A Clamped Inductive Load		
		Q2	—	8.0	—				
t _r	Rise Time	Q1	—	9.3	—				
		Q2	—	14	—				
t _{d(off)}	Turn-Off Delay Time	Q1	—	8.0	—				
		Q2	—	13	—				
t _f	Fall Time	Q1	—	3.4	—				
		Q2	—	5.3	—				
C _{iss}	Input Capacitance	Q1	—	850	—			pF	V _{GS} = 0V V _{DS} = 15V f = 1.0MHz
		Q2	—	1790	—				
C _{oss}	Output Capacitance	Q1	—	190	—				
		Q2	—	390	—				
C _{rss}	Reverse Transfer Capacitance	Q1	—	88	—				
		Q2	—	190	—				

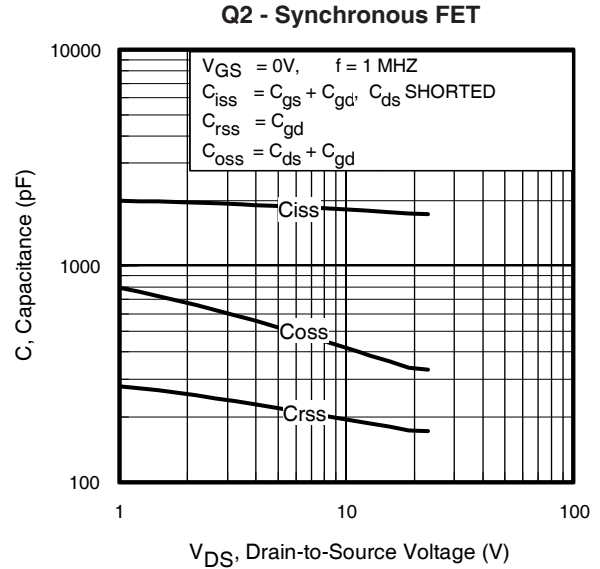
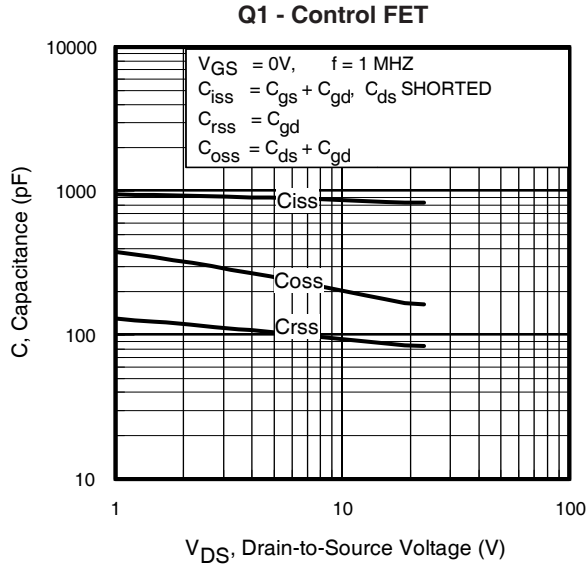
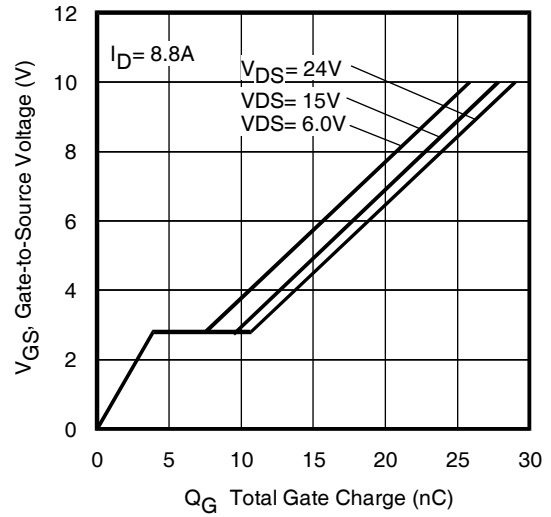
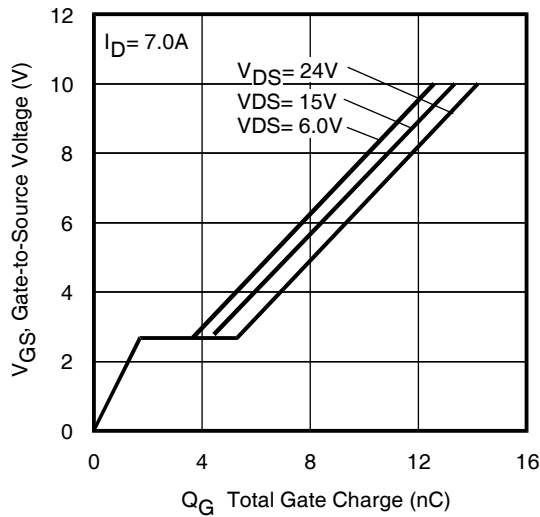
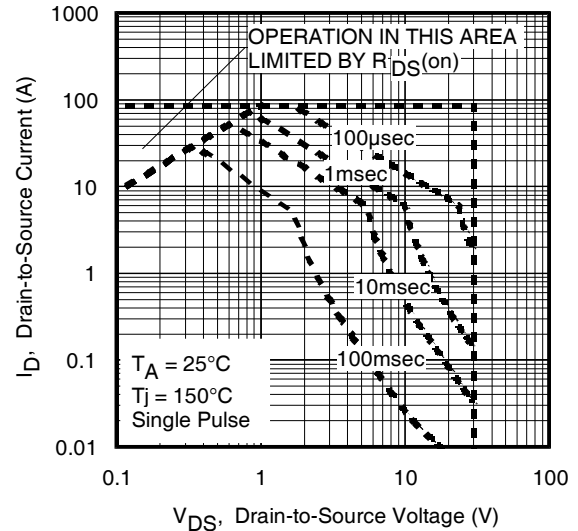
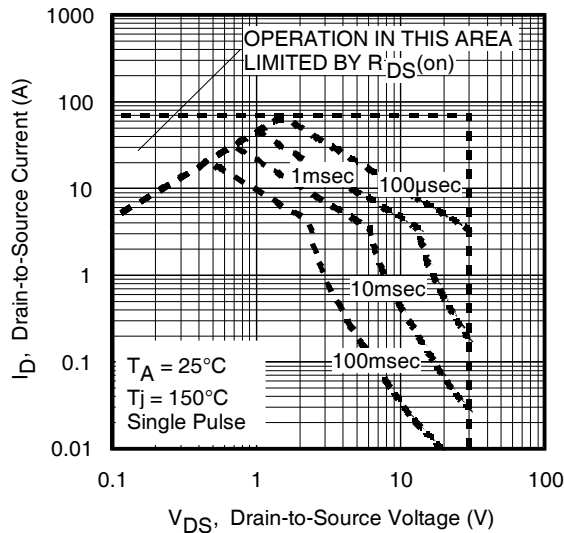
Avalanche Characteristics

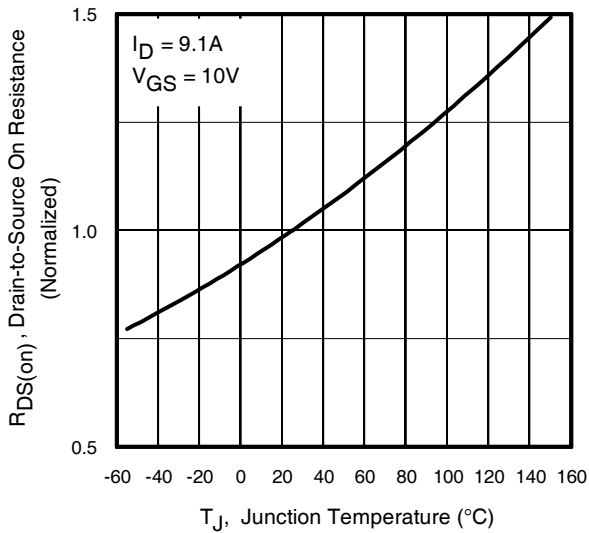
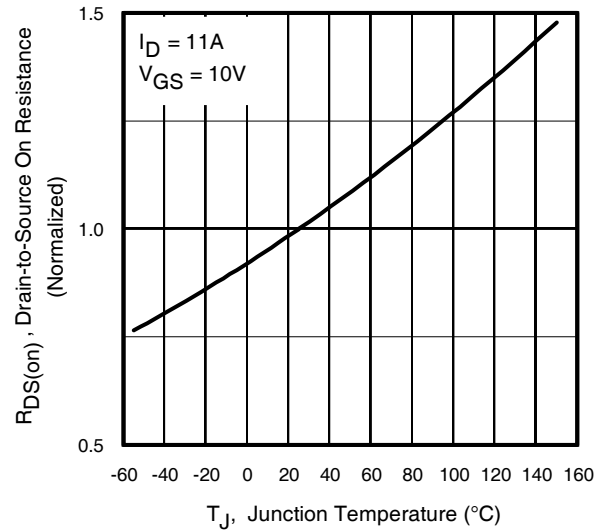
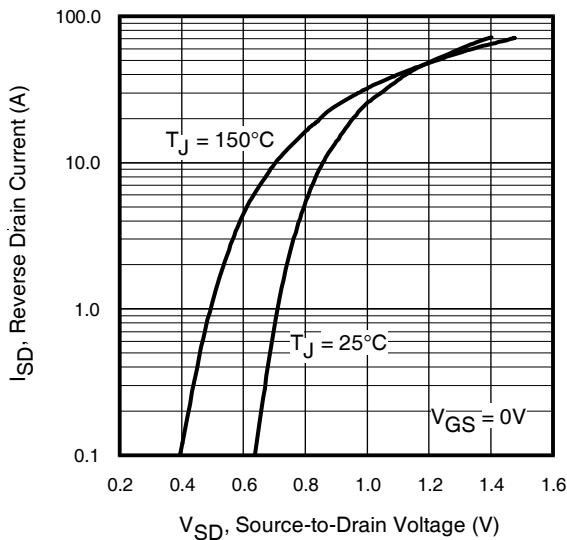
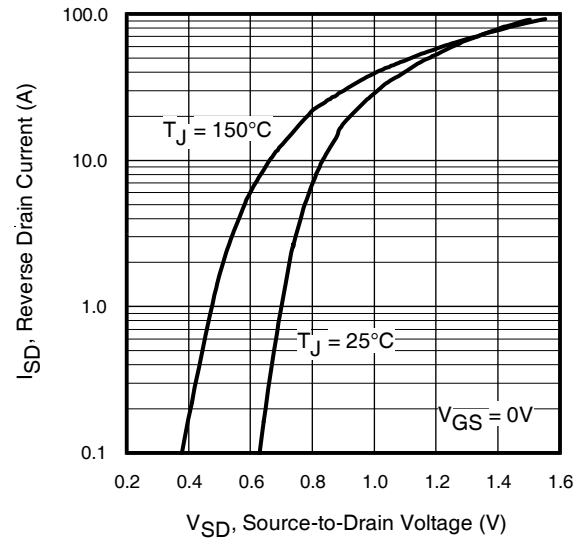
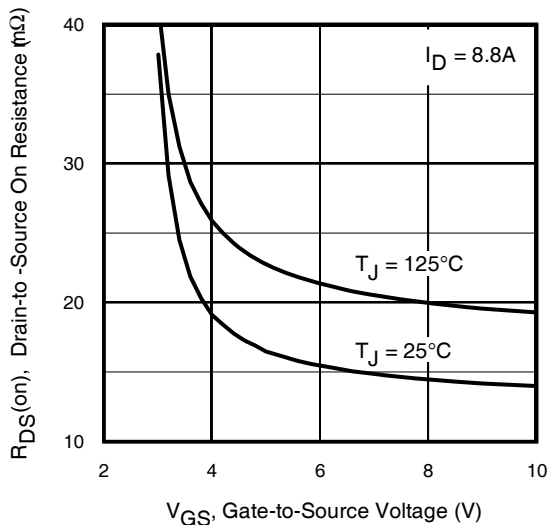
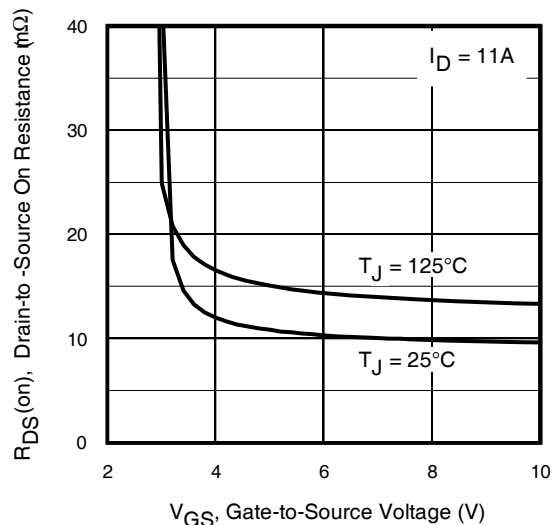
	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E _{AS}	Single Pulse Avalanche Energy ②	—	10	15	mJ
I _{AR}	Avalanche Current ①	—	7.0	8.8	A

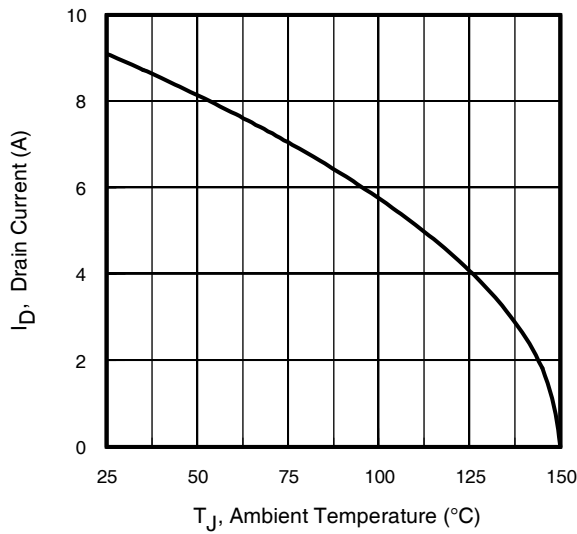
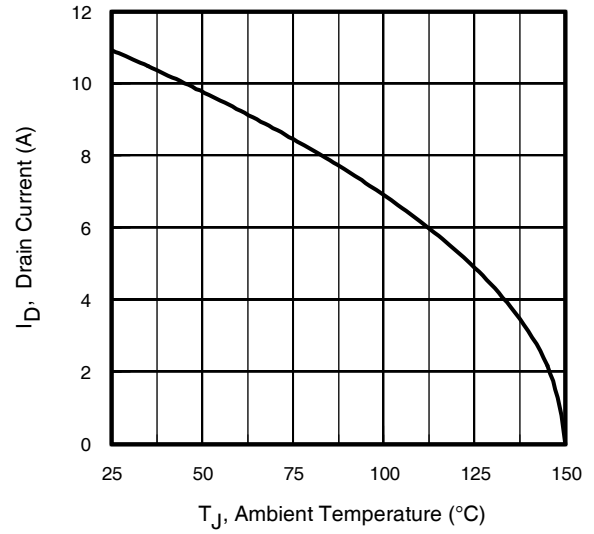
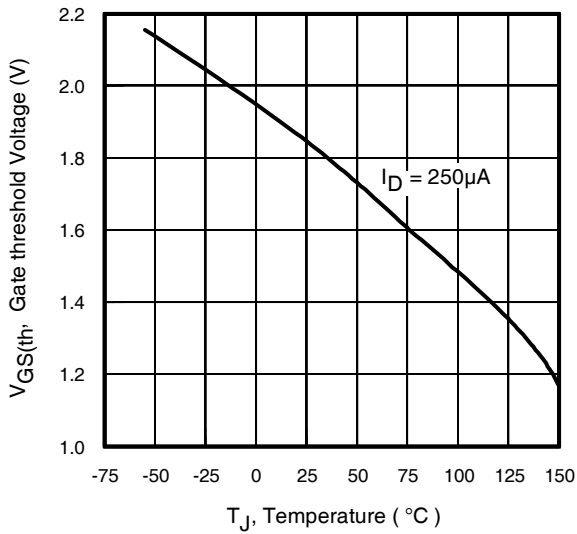
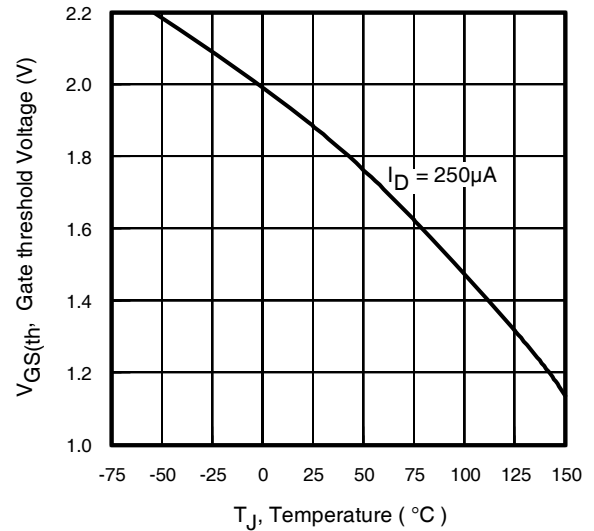
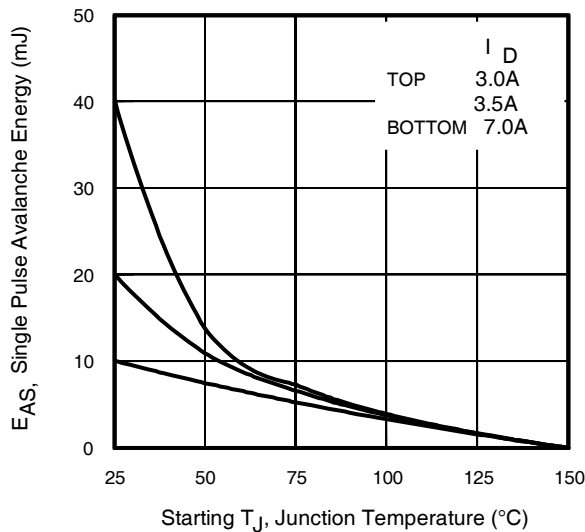
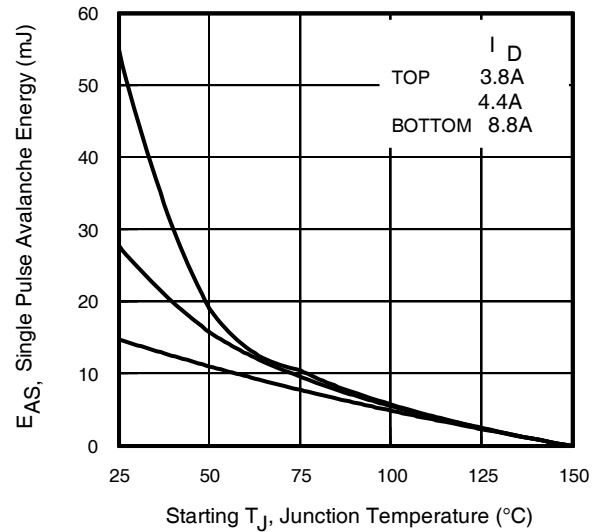
Diode Characteristics

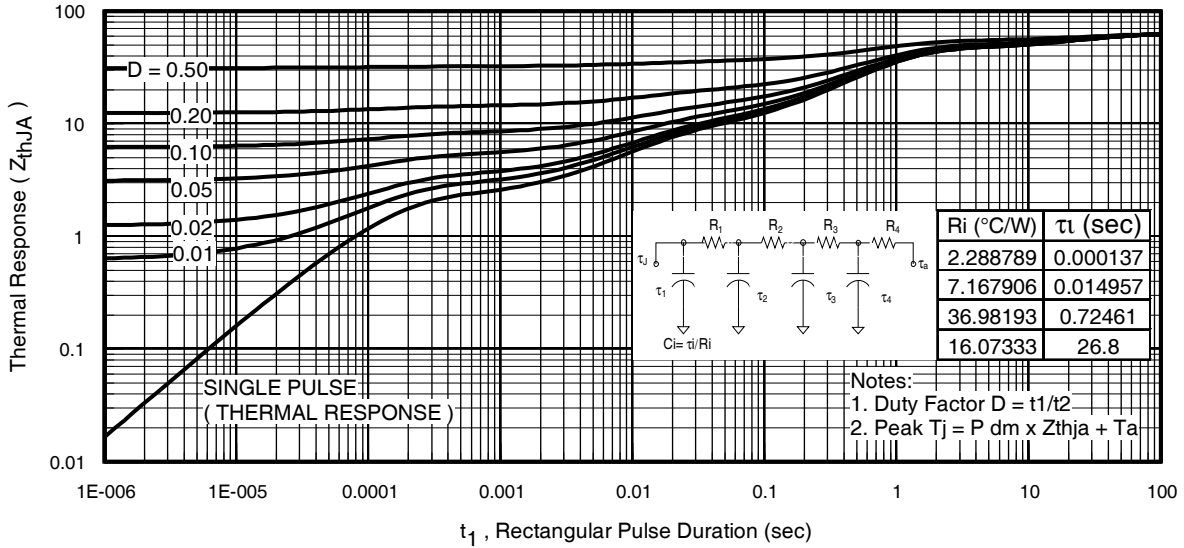
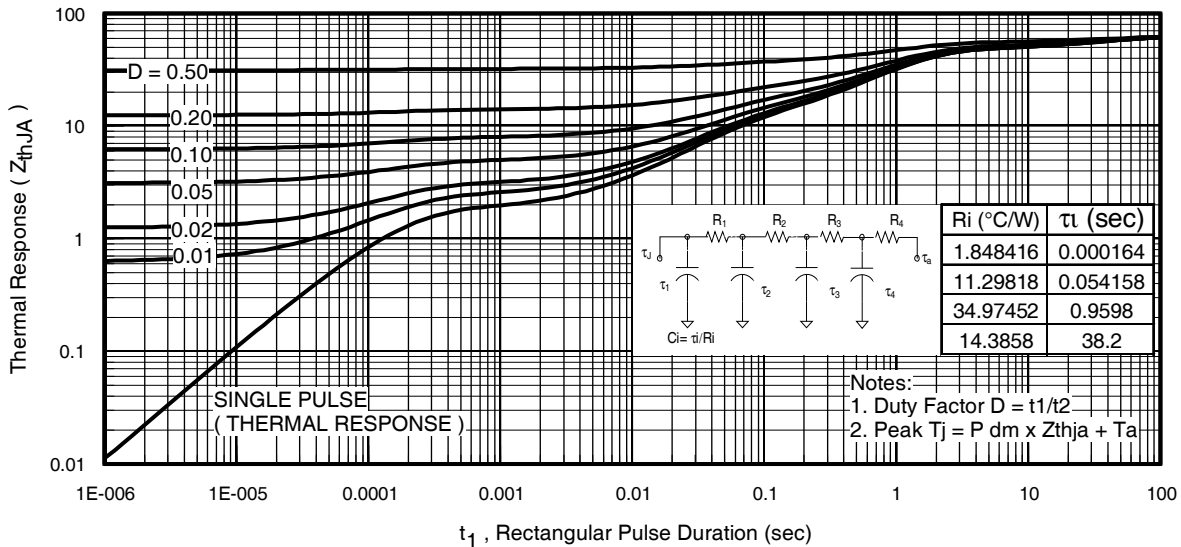
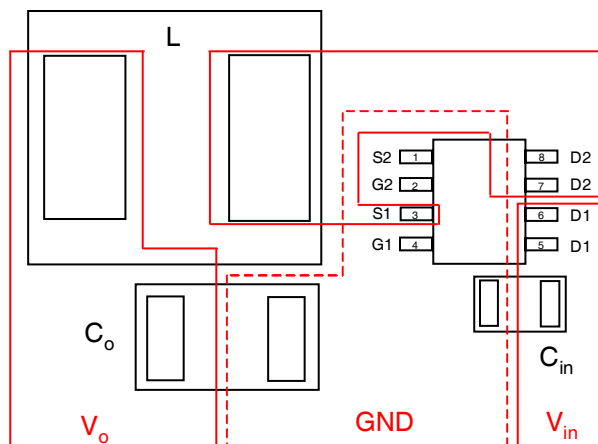
	Parameter		Min.	Typ.	Max.	Units	Conditions	
I _S	Continuous Source Current (Body Diode)	Q1	—	—	2.8	A	MOSFET symbol showing the integral reverse p-n junction diode. 	
		Q2	—	—	2.8			
I _{SM}	Pulsed Source Current (Body Diode) ①	Q1	—	—	76	A		
		Q2	—	—	85			
V _{SD}	Diode Forward Voltage	Q1	—	—	1.0	V		T _J = 25°C, I _S = 7.3A, V _{GS} = 0V ③
		Q2	—	—	1.0			T _J = 25°C, I _S = 8.8A, V _{GS} = 0V ③
t _{rr}	Reverse Recovery Time	Q1	—	12	18	ns	Q1 T _J = 25°C, I _F = 7.0A, V _{DD} = 15V, di/dt = 100A/μs ③	
		Q2	—	16	24			
Q _{rr}	Reverse Recovery Charge	Q1	—	4.1	6.1	nC	Q2 T _J = 25°C, I _F = 8.8A, V _{DD} = 15V, di/dt = 100A/μs ③	
		Q2	—	5.9	8.9			

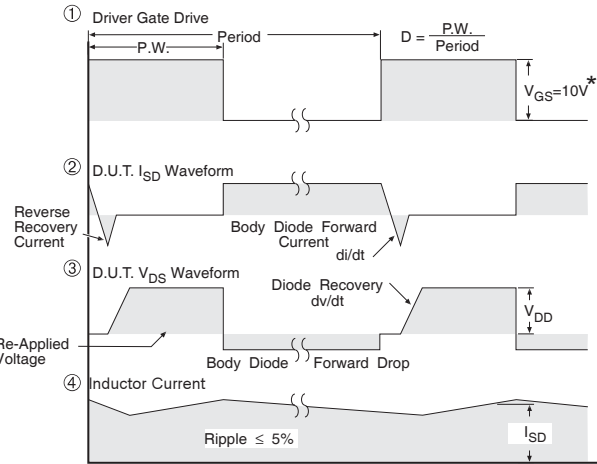
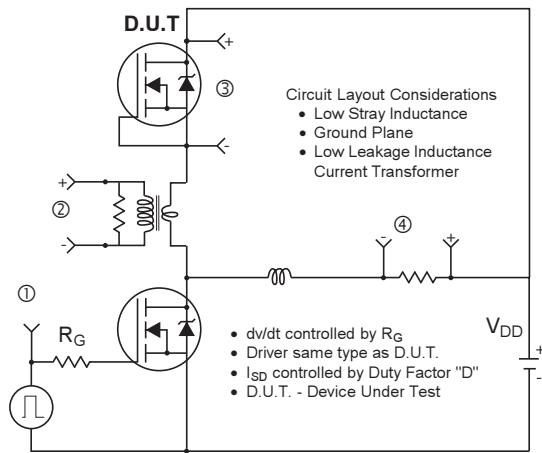
Typical Characteristics

Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Output Characteristics

Fig 4. Typical Output Characteristics

Fig 5. Typical Transfer Characteristics

Fig 6. Typical Transfer Characteristics

Typical Characteristics

Fig 7. Typical Capacitance vs. Drain-to-Source Voltage **Fig 8. Typical Capacitance vs. Drain-to-Source Voltage**

Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage
Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

Fig 11. Maximum Safe Operating Area
Fig 12. Maximum Safe Operating Area

Typical Characteristics
Q1 - Control FET

Fig 13. Normalized On-Resistance vs. Temperature
Q2 - Synchronous FET

Fig 14. Normalized On-Resistance vs. Temperature

Fig 15. Typical Source-Drain Diode Forward Voltage

Fig 16. Typical Source-Drain Diode Forward Voltage

Fig 17. Typical On-Resistance vs. Gate Voltage

Fig 18. Typical On-Resistance vs. Gate Voltage

Typical Characteristics
Q1 - Control FET

Fig 19. Maximum Drain Current vs. Ambient Temp.
Q2 - Synchronous FET

Fig 20. Maximum Drain Current vs. Ambient Temp.

Fig 21. Threshold Voltage vs. Temperature

Fig 22. Threshold Voltage vs. Temperature

Fig 23. Maximum Avalanche Energy vs. Drain Current

Fig 24. Maximum Avalanche Energy vs. Drain Current


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q1)

Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient (Q2)

Fig 27. Layout Diagram



* $V_{GS} = 5V$ for Logic Level Devices

Fig 28. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

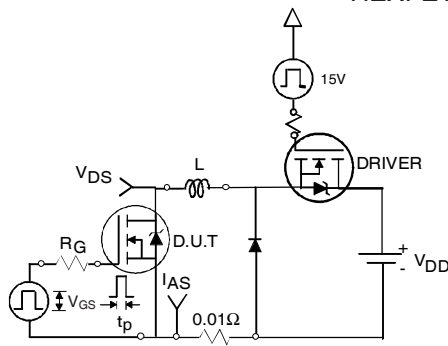


Fig 29a. Unclamped Inductive Test Circuit

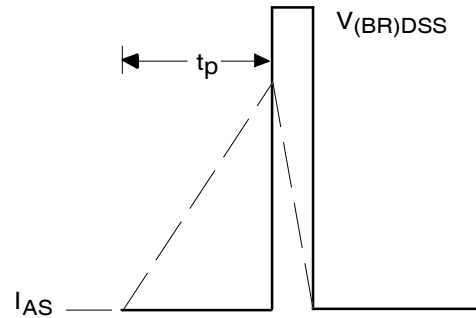


Fig 29b. Unclamped Inductive Waveforms

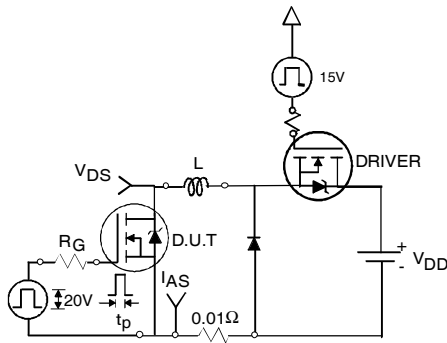


Fig 30a. Switching Time Test Circuit

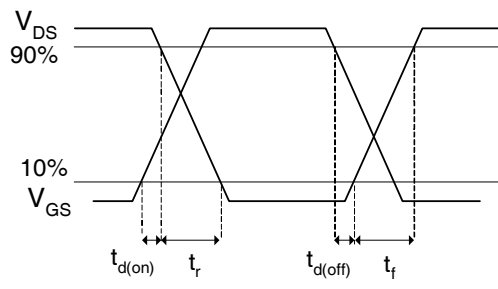


Fig 30b. Switching Time Waveforms

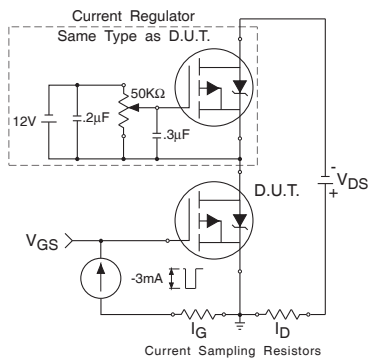


Fig 31a. Gate Charge Test Circuit

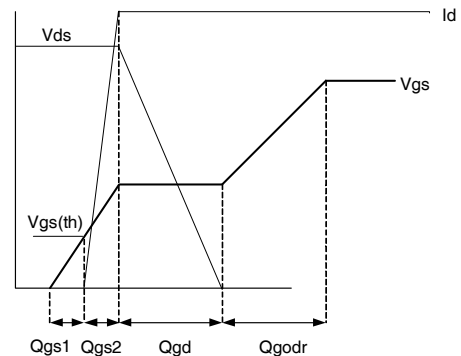
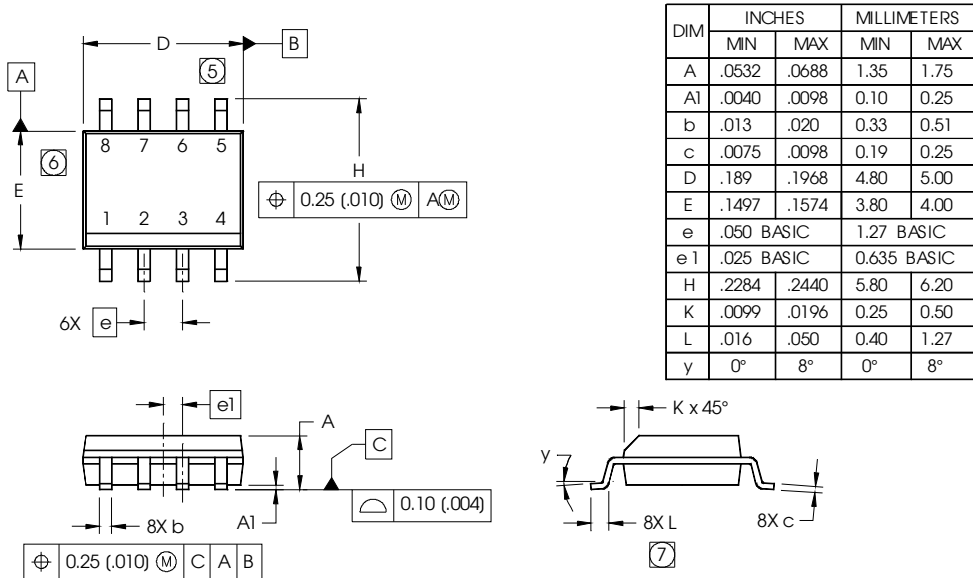


Fig 31b. Gate Charge Waveform

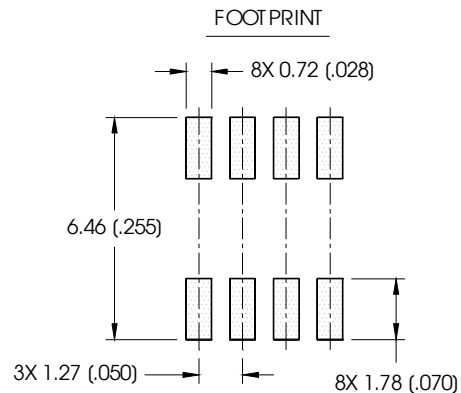
SO-8 Package Outline (MOSFET & Fetky)

Dimensions are shown in millimeters (inches)



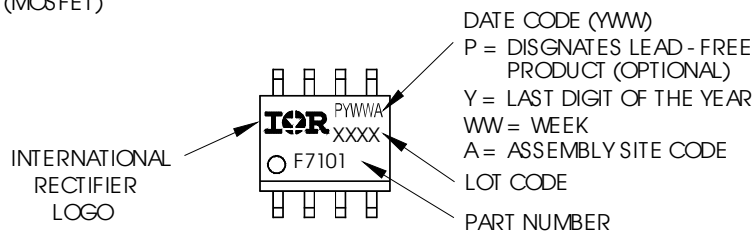
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
- ⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
- ⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
- ⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



SO-8 Part Marking Information

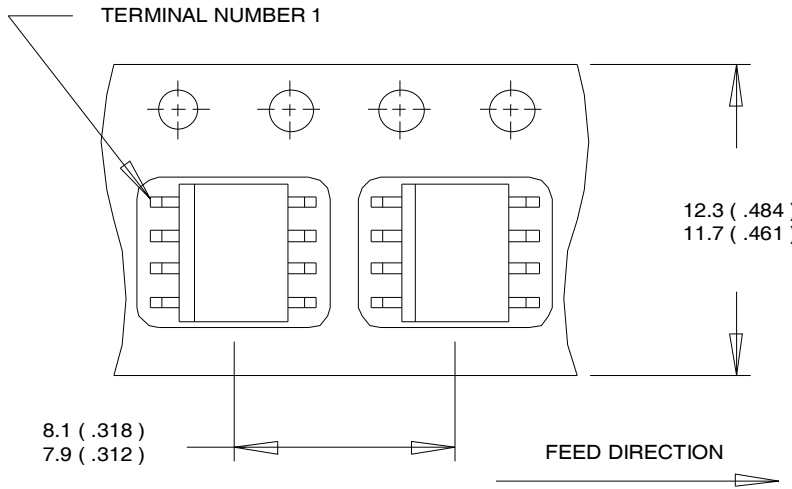
EXAMPLE: THIS IS AN IRF7101 (MOSFET)



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

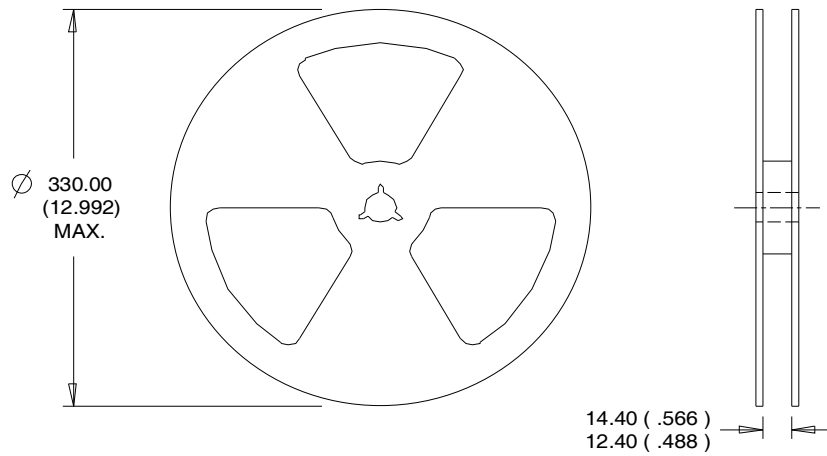
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Qualification information[†]

Qualification level	Industrial (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	SO-8	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>
^{††} Applicable version of JEDEC standard at the time of product release

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, Q1: $L = 0.41\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 7.0\text{A}$; Q2: $L = 0.38\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 8.8\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ When mounted on 1 inch square copper board.
- ⑤ R_θ is measured at T_J approximately 90°C .

Revision History

Date	Comments
10/16/2014	<ul style="list-style-type: none"> • Corrected part number from "IRF7907VPbF-1" to "IRF7907VTRPbF-1" -all pages • Removed the "IRF7907VPbF-1" bulk part number from ordering information on page1

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon Technologies\(英飞凌\)](#)