REPETITIVE AVALANCHE AND dv/dt RATED HEXFET® TRANSISTORS

TO-39

Product Summary

Part Number	BVDSS	$R_{DS(on)}$	I_D
IRLF120	100V	0.35Ω	5.3A

Description

The Logic Level 'L' series of power MOSFETs are designed to be operated with level logic gate-to-source voltage of 5V. In addition to the well established characteristics of HEXFETs®, they have the added advantage of providing low drive requirements to interface power loads to logic level IC's and microprocessors.

Fields of applications include: high speed power applications such as switching regulators, switching converters, motor drivers, solenoid and relay drivers and drivers for high power bipolar switching transistors requiring high speed and low gate drive voltage.

The HEXFET technology is the key to International Rectifier's HiRel advanced line of logic level power MOSFET transistors. The efficient geometry and unique processing of the HEXFET achieve very low on-state resistance combined with high trans conductance and great device ruggedness.

Features

- Repetitive Avalanche Ratings
- Dynamic dv/dt Rating
- Low Drive Requirements
- Excellent Temperature Stability
- Fast Switching Speeds
- Hermetically Sealed
- Light Weight
- ESD Rating: Class 1B per MIL-STD-750, Method 1020

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
I_{D1} @ V_{GS} = 5.0V, T_C = 25°C	Continuous Drain Current	5.3	A
I_{D2} @ V_{GS} = 5.0V, T_C = 100°C	Continuous Drain Current	3.4	
I_{DM} @ T_C = 25°C	Pulsed Drain Current ①	21	
P_D @T_C = 25°C	Maximum Power Dissipation	20	W
	Linear Derating Factor	0.16	W/°C
V_{GS}	Gate-to-Source Voltage	± 10	V
E_{AS}	Single Pulse Avalanche Energy ②	120	mJ
I_{AR}	Avalanche Current ①	5.3	A
E_{AR}	Repetitive Avalanche Energy ①	2.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.5	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	0.98 (Typical)	g

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.13	—	V/°C	Reference to 25°C, I_D = 250µA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.35	Ω	V_{GS} = 5.0V, I_{D2} = 3.4A ④
		—	—	0.42		V_{GS} = 4.0V, I_D = 2.7A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
Gfs	Forward Transconductance	3.1	—	—	S	V_{DS} = 15V, I_{D2} = 3.4A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	250	µA	V_{DS} = 80V, V_{GS} = 0V
		—	—	1000		V_{DS} = 80V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_G	Total Gate Charge	—	—	13	nC	I_{D1} = 5.3A
Q_{GS}	Gate-to-Source Charge	—	—	2.4		V_{DS} = 80V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	7.1		V_{GS} = 5.0V
$t_{d(on)}$	Turn-On Delay Time	—	—	13	ns	V_{DD} = 50V
tr	Rise Time	—	—	73		I_{D1} = 5.3A
$t_{d(off)}$	Turn-Off Delay Time	—	—	41		R_G = 18Ω
t_f	Fall Time	—	—	27		V_{GS} = 5.0V
Ls +L_D	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm / 0.25 in from package) to Source lead (6mm/ 0.25 in from package) with Source wire internally bonded from Source pin to Drain pin
C_{iss}	Input Capacitance	—	480	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	150	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	30	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	5.3	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	21		
V_{SD}	Diode Forward Voltage	—	—	2.5	V	T_J = 25°C,I_S = 5.3A, V_{GS} = 0V④
t_{rr}	Reverse Recovery Time	—	—	220	ns	T_J = 25°C, I_F = 5.3A, V_{DD} ≤ 50V
Q_{rr}	Reverse Recovery Charge	—	—	1.1	µC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Thermal Resistance

Symbol	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	6.25	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	175	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L = 6.1mH, Peak I_L = 5.3A, V_{GS} = 5.0V, R_G = 25Ω

③ I_{SD} ≤ 5.3A, di/dt ≤ 110A/µs, V_{DD} ≤ 100V, T_J ≤ 150°C, Suggested R_G =18 Ω

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

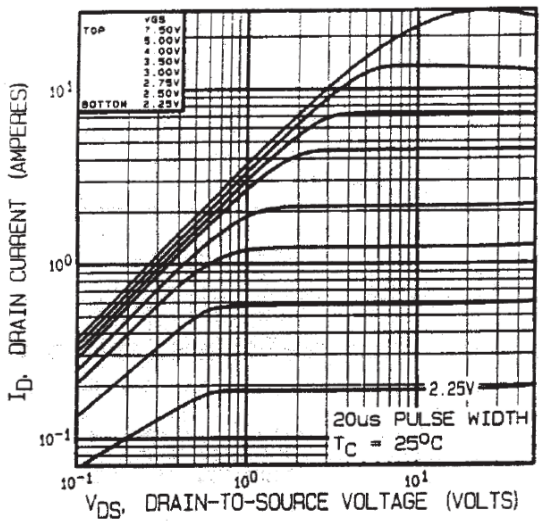


Fig 1. Typical Output Characteristics

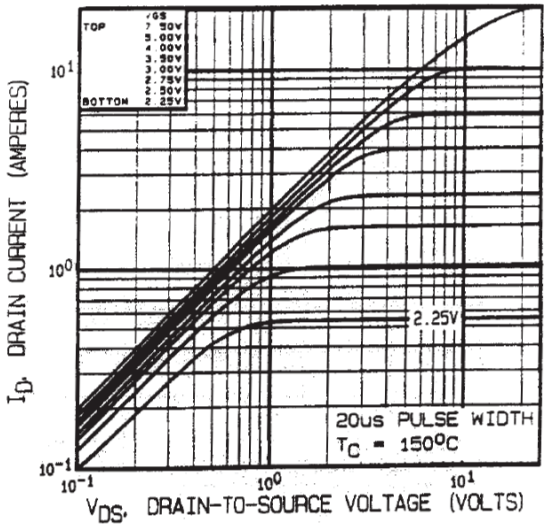


Fig 2. Typical Output Characteristics

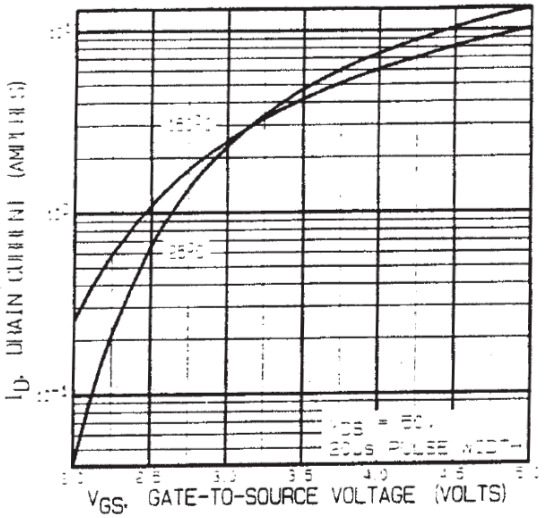


Fig 3. Typical Transfer Characteristics

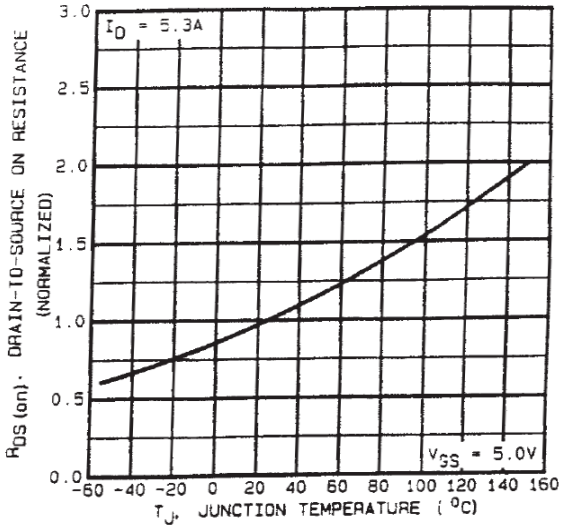


Fig 4. Normalized On-Resistance Vs. Temperature

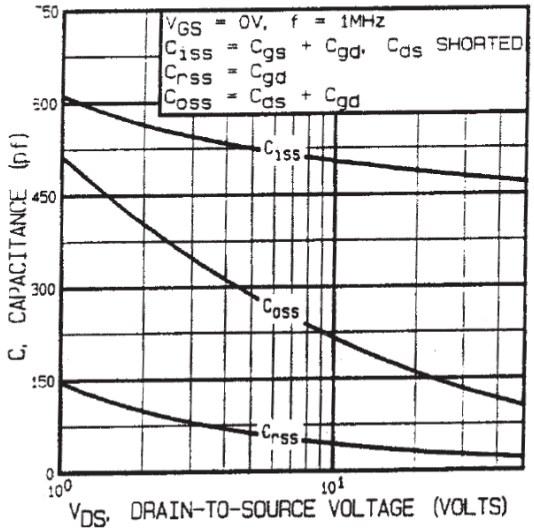


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

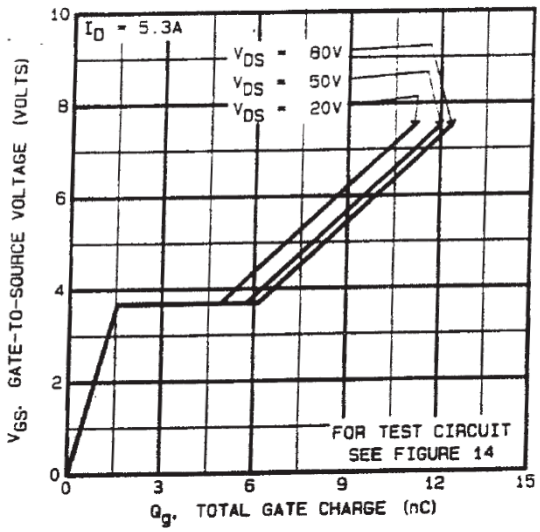


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

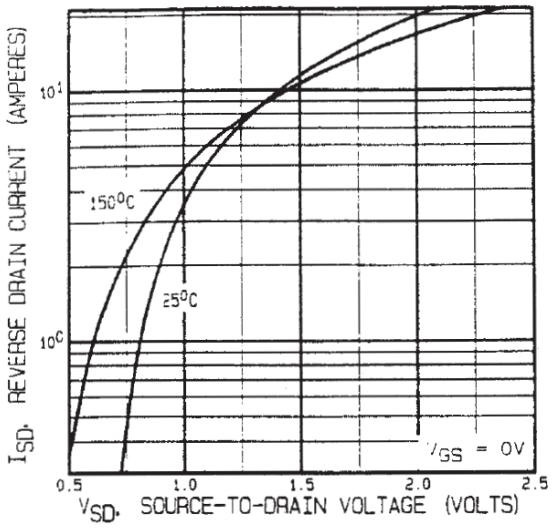


Fig 7. Typical Source-Drain Diode Forward Voltage

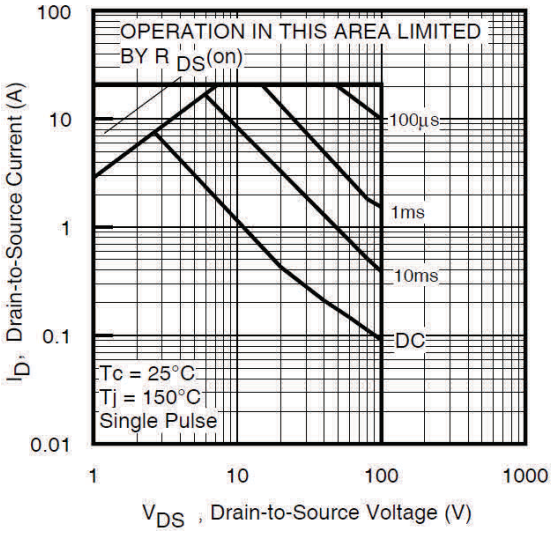


Fig 8. Maximum Safe Operating Area

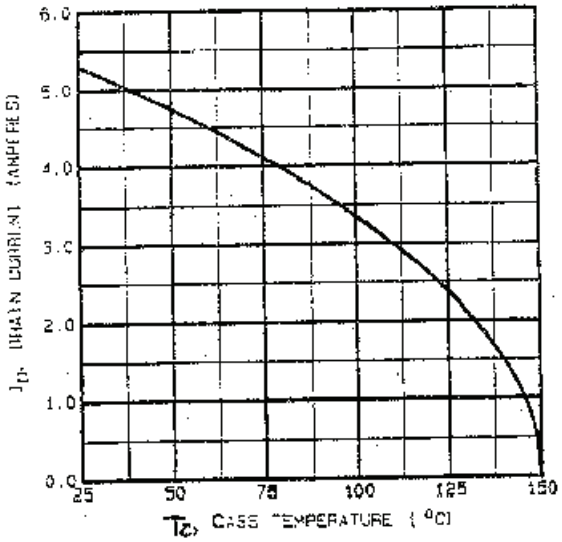


Fig 9. Maximum Drain Current Vs. Case Temperature

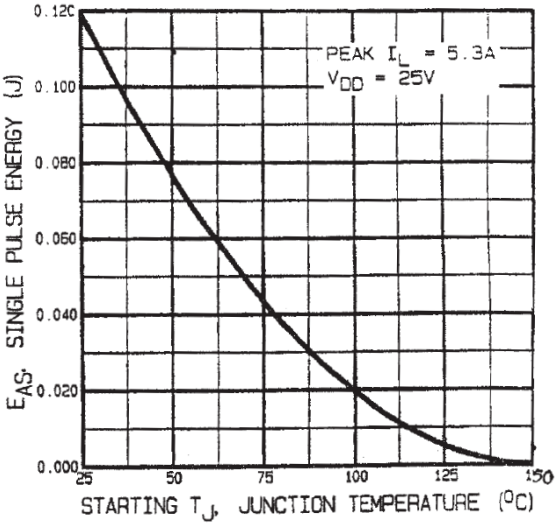


Fig 10. Maximum Avalanche Energy Vs. Drain Current

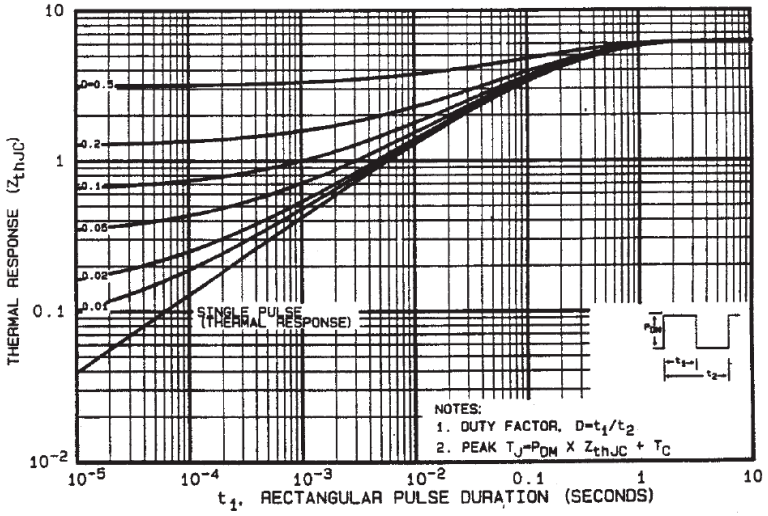


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

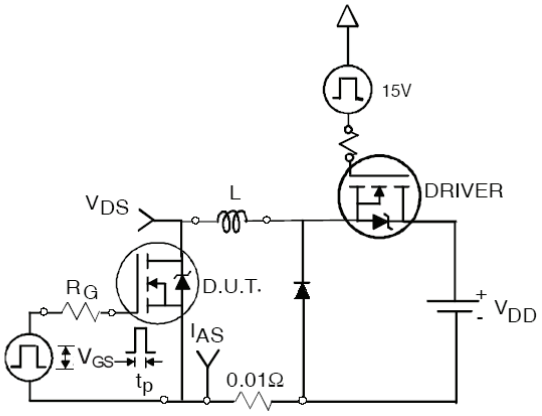


Fig 12a. Unclamped Inductive Test Circuit

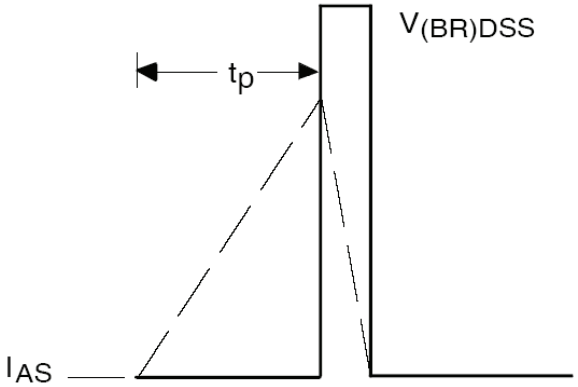


Fig 12b. Unclamped Inductive Waveforms

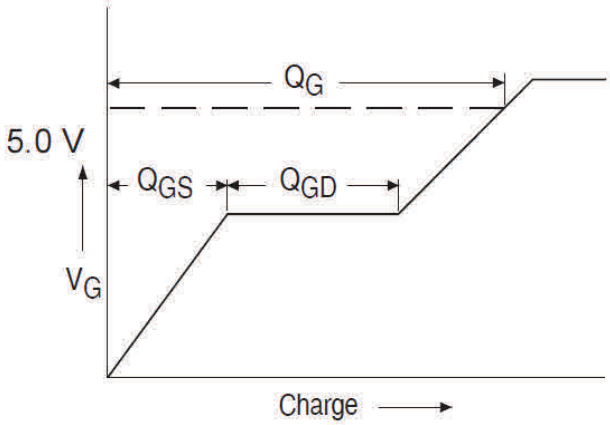


Fig 13a. Gate Charge Waveform

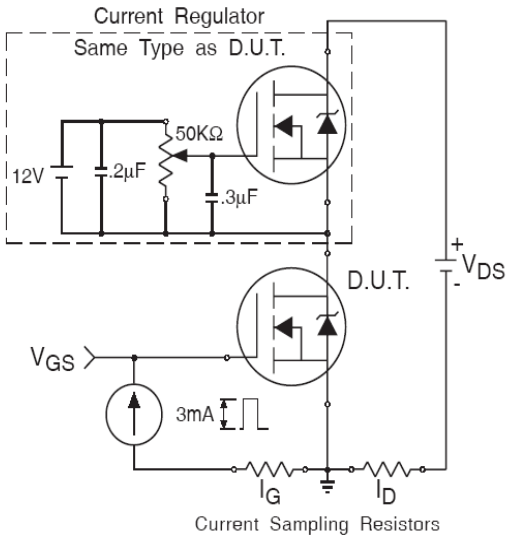


Fig 13b. Gate Charge Test Circuit

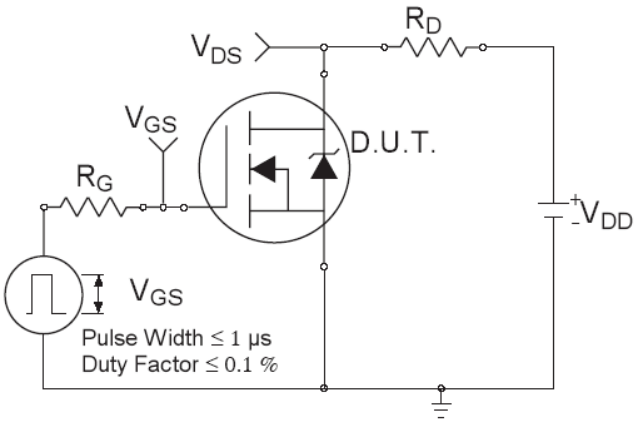


Fig 14a. Switching Time Test Circuit

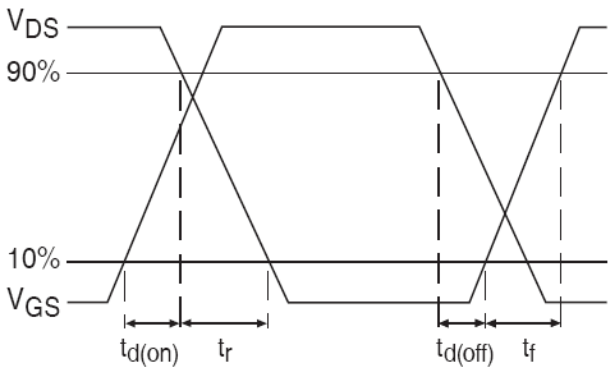
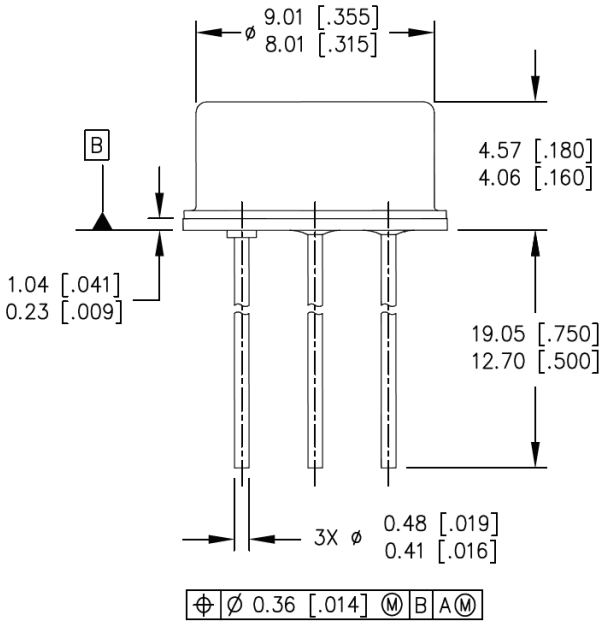
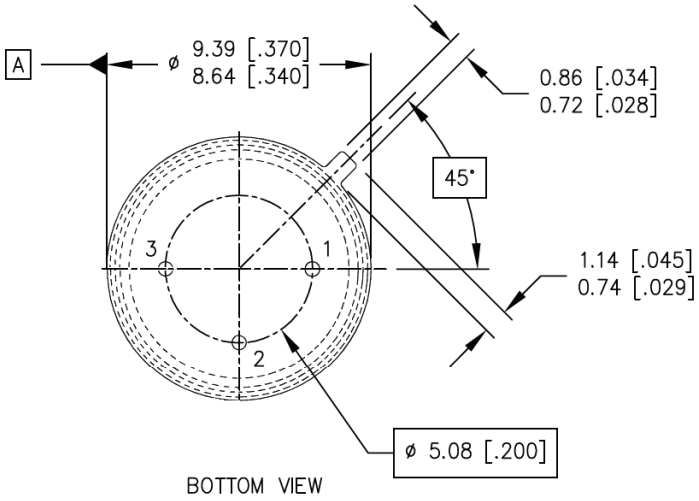


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions - TO-205AF (TO-39)



SIDE VIEW



BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M–1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO–205AF (TO–39).

LEGEND
1- SOURCE
2- GATE
3- DRAIN (CONNECTED TO THE CASE)

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