BTN7030-1EPA

NovalithIC™ Lite – smart integrated half-bridge

Features

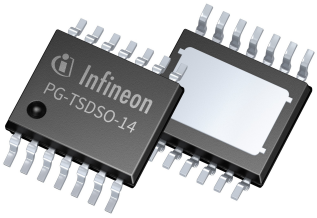
- Low-side and high-side switch in half-bridge configuration with diagnosis and embedded protection
- Part of NovalithIC™ family
- Switch ON capability while inverse current condition (InverseON)
- Green product (RoHS compliant)

Protection features

- Temperature limitation with intelligent latch
- Overcurrent protection (tripping) with intelligent latch for both the low-side and high-side output stage
- Undervoltage shutdown
- Cross current protection

Diagnostic features

- Proportional load current sense for high-side load currents
- Open load in ON and OFF state
- Short circuit to ground or battery



Potential applications

- Replaces electromechanical relays, fuses and discrete circuits
- Suitable for driving motors and solenoids of a max. inductance of 3 mH at maximal current
- Temperature dependent overload detection current level with min. 17 A (T_J < 75°C), min. 15 A (T_J = 125°C) and min. 14 A (T_J = 150°C)
- Current sense diagnosis optimized for motor and solenoid applications

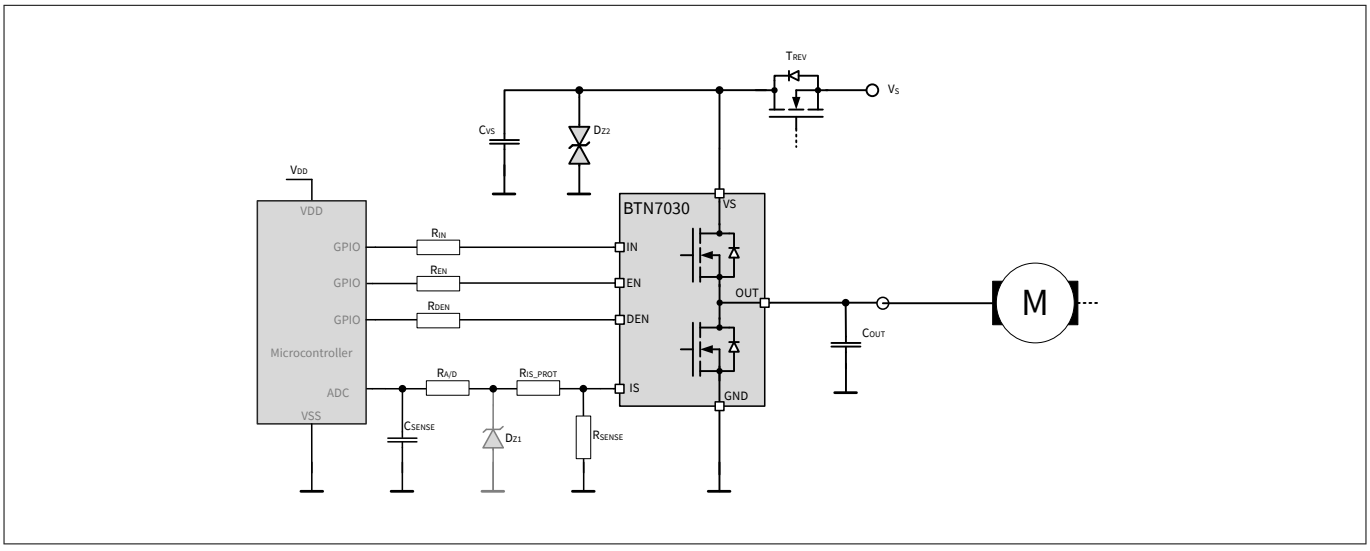


Figure 1 Potential application

Product Type	Package	Marking
BTN7030-1EPA	PG-TSDSO-14	BTN7030-1EPA

Description

The BTN7030-1EPA is a protected half-bridge with integrated driver, providing protection and diagnosis functions. The device is integrated in SMART7 technology.

Table 1 Product Summary

Parameter	Symbol	Values
Minimum operating voltage (at switch ON)	$V_{S(OP)}$	3.8 V
Minimum operating voltage (cranking)	$V_{S(UV)}$	3.5 V
Maximum operating voltage	V_S	28 V
Minimum overvoltage protection ($T_J \geq 25°C$)	$V_{DS(CLAMP)\_25}$	35 V
Maximum current in sleep mode ($T_J \leq 85°C$)	$I_{VS(SLEEP)\_85\_stdy}$	3 µA
Maximum operative current	$I_{GND(ACTIVE)}$	5 mA
Maximum ON-state resistance ($T_J = 150°C$) high-side	$R_{DS(ON)\_150(HS)}$	25.5 mΩ
Maximum ON-state resistance ($T_J = 150°C$) low-side	$R_{DS(ON)\_150(LS)}$	36.5 mΩ
Min. overload detection current at $T_J < 75°C$	$I_{L(OVL0)\_-40(HS)}$	17 A
Min. overload detection current at $T_J = 125°C$	$I_{L(OVL0)\_125(HS)}$	15 A
Min. overload detection current at $T_J = 150°C$	$I_{L(OVL0)\_150(HS)}$	14 A
Typical current sense ratio at $I_L = I_{L(NOM)}$	k_{ILIS}	4300
Nominal load current	$I_{L(NOM)}$	7 A

Product validation

Qualified for automotive applications.
Product validation according to AEC-Q100.

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1 Block diagram and terms

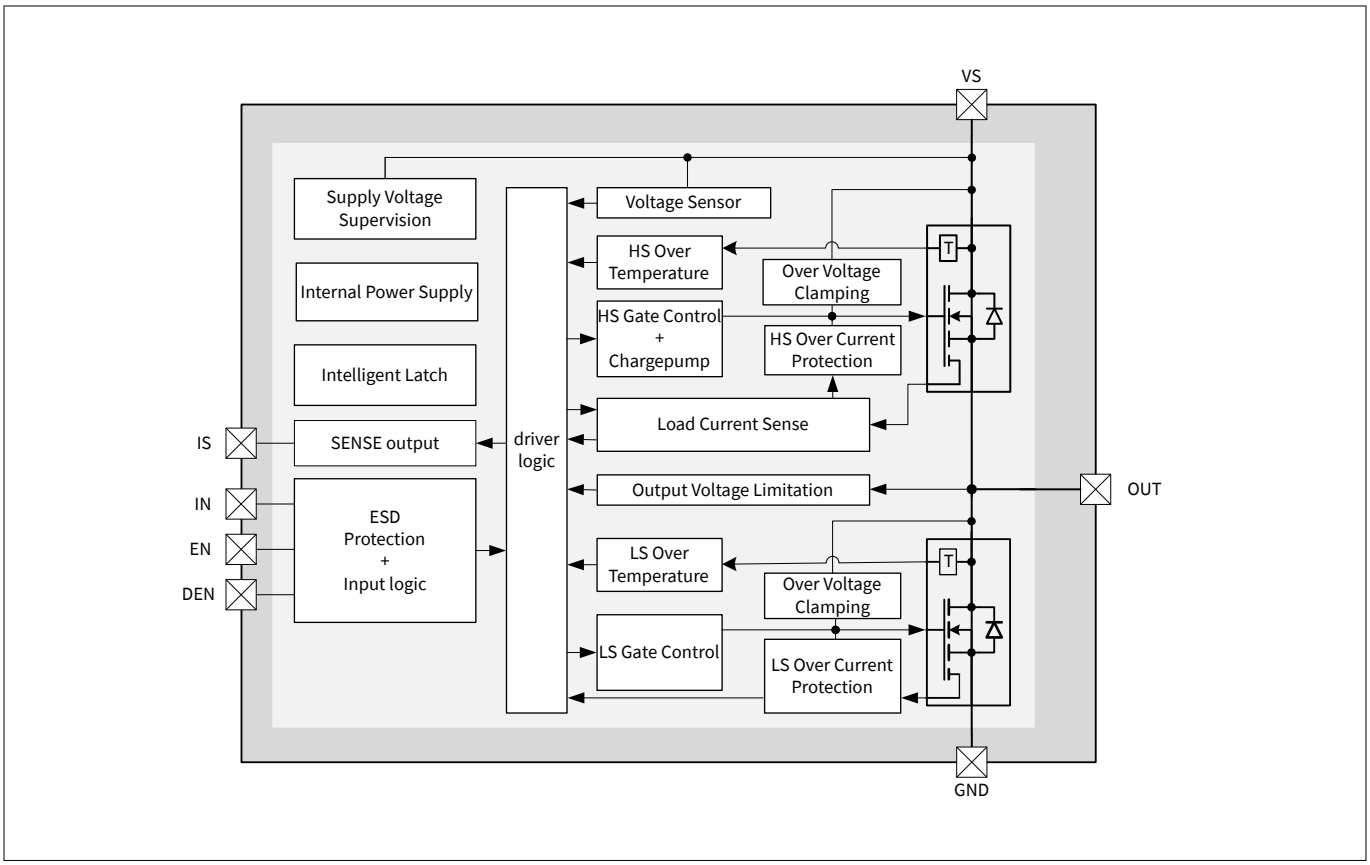


Figure 2

1.1 Terms

Figure 3 shows all terms used in this data sheet, with associated convention for positive values.

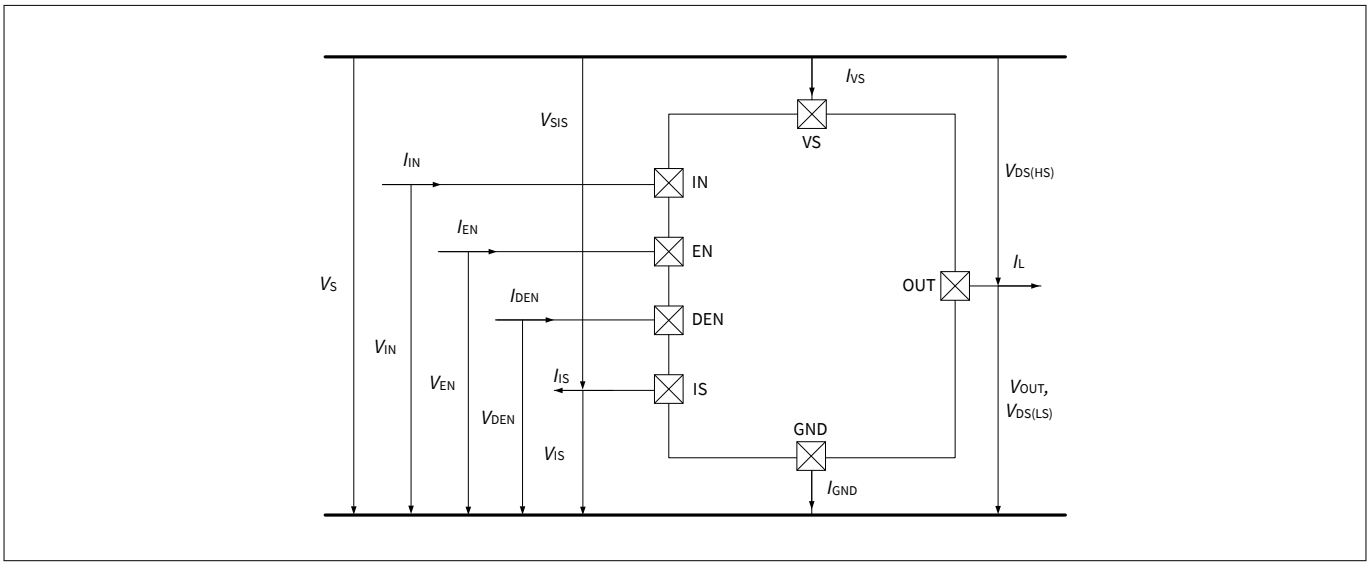


Figure 3 Voltage and current convention

2 Pin configuration

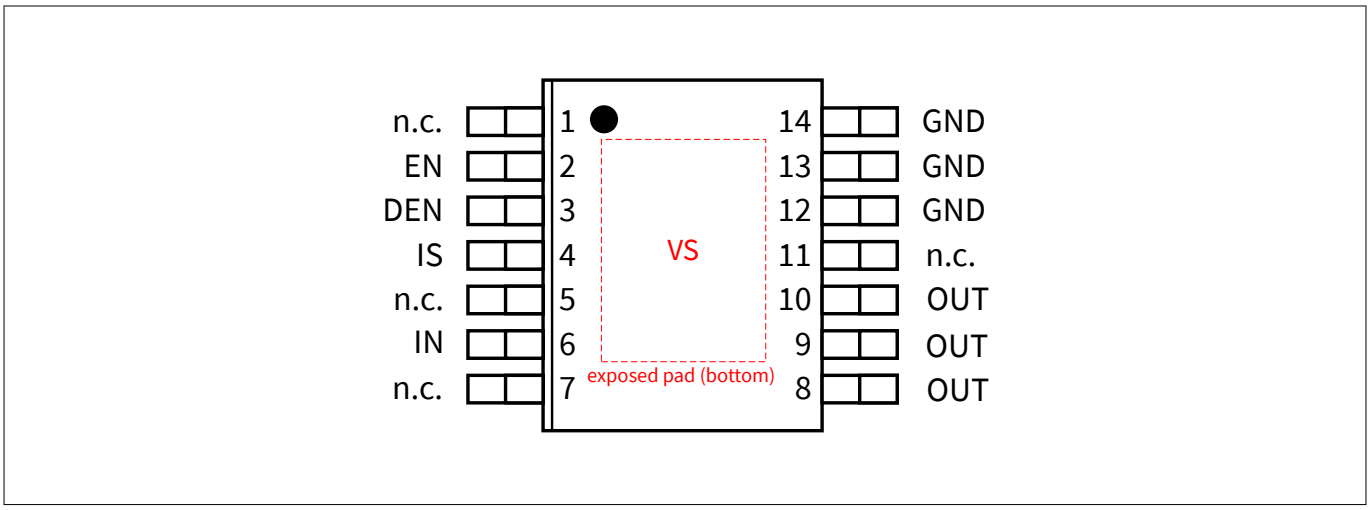


Figure 4 Pin configuration

2.1 Pin definitions and functions

Table 2 Pin Definition

Pin	Symbol	Function
EP	VS (exposed pad)	**Supply Voltage** Battery voltage
2	EN	**Enable** Digital signal to enable the normal operational mode (active mode) of the BTN7030-1EPA and to clear the protection latch
3	DEN	**Diagnostic Enable** Digital signal to enable device diagnosis ("high" active) and to clear the protection latch If not used: connect to GND pin or to module ground with a 10 kΩ resistor
4	IS	**SENSE current output** Analog/digital signal for diagnosis If not used: left open
6	IN	**Input** Digital signal to switch ON either the low-side or high-side output stage of the half-bridge
8-10	OUT	**Output** Protected half-bridge power output [1)]
12-14	GND	**Ground** Signal ground and ground connection for the low-side switch [1)]
1, 5, 7, 11	n.c.	Not connected, internally not bonded

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

3 Absolute maximum ratings

3.1 Absolute maximum ratings

Table 3 Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified); all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Not subject to production test - specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply pins							
Power supply voltage	V_S	-0.3	–	28	V	–	PRQ-6
Load dump voltage	$V_{BAT(LD)}$	–	–	35	V	Suppressed Load Dump acc. to ISO16750-2 (2010). R_i= 2 Ω	PRQ-8
Supply voltage for short circuit protection	$V_{BAT(SC)}$	0	–	24	V	Setup acc. to AEC-Q100-012	PRQ-9
Current through DI pin	I_{DI}	-1	–	2	mA	1)	PRQ-25
IS pin							
Voltage at IS pin	V_{IS}	-1.5	–	V_S	V	I_{IS}= 10 µA	PRQ-26
Current through IS pin	I_{IS}	-25	–	$I_{IS(FAULT),MAX}$	mA	–	PRQ-28
Temperatures							
Junction temperature	T_J	-40	–	150	°C	–	PRQ-29
Storage temperature	T_{STG}	-55	–	150	°C	–	PRQ-30
ESD Susceptibility							
ESD susceptibility all pins (HBM)	$V_{ESD(HBM)}$	-2	–	2	kV	HBM 2)	PRQ-31
ESD susceptibility OUT vs GND and VS connected (HBM)	$V_{ESD(HBM)\_OUT}$	-4	–	4	kV	HBM 2)	PRQ-32
ESD susceptibility all pins (CDM)	$V_{ESD(CDM)}$	-500	–	500	V	CDM 3)	PRQ-34
ESD susceptibility corner pins (CDM)	$V_{ESD(CDM)\_CRN}$	-750	–	750	V	pins 1, 7, 8, 14 CDM 3)	PRQ-35
Power stages - 12 mΩ high-side							
Load current, high-side switch	$\|I_L\|_{(HS)}$	–	–	$I_{L(OVL),MAX}$	A	–	PRQ-39
Power stages - 20 mΩ low-side							

(table continues...)

Table 3 (continued) Absolute maximum ratings

T_J = -40°C to +150°C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified); all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Not subject to production test - specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Load current, low-side switch	$\|I_L\|_{(LS)}$	–	–	$I_{L(OVL),MAX}$	A	–	PRQ-42

1) Maximum V_{DI} to be considered for latch-up tests: 5.5 V
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF)
3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

- Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.

3.2 Functional range

Table 4 Functional range

Not subject to production test - specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Supply voltage range for normal operation	$V_{S(NOR)}$	6	13.5	18	V	–	PRQ-43
Lower extended supply voltage range for operation	$V_{S(EXT,LOW)}$	3.5	–	6	V	***1)*** ***2)*** parameter deviations possible	PRQ-44
Upper extended supply voltage range for operation	$V_{S(EXT,UP)}$	18	–	28	V	***1)*** parameter deviations possible	PRQ-45

1) Protection functions still operative
2) In case of V_S voltage decreasing: $V_{S(EXT,LOW),MIN}$ = 3.5 V. In case of V_S voltage increasing: $V_{S(EXT,LOW),MIN}$ = 3.8 V

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

3.3 Thermal resistance

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to ***www.jedec.org****.*

Absolute maximum ratings

Table 5 Thermal resistance

Not subject to production test - specified by design.

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal resistance junction-to-case, high-side switch	$R_{thJC(HS)}$	–	2.7	4.3	K/W	1)	PRQ-48
Thermal resistance junction-to-case, low-side switch	$R_{thJC(LS)}$	–	0.95	1.5	K/W	1)	PRQ-540
Thermal resistance junction to ambient, high-side switch	$R_{thJA(HS)}$	–	36	–	K/W	1)	PRQ-49
Thermal resistance junction to ambient, low-side switch	$R_{thJA(LS)}$	–	32.5	–	K/W	1)	PRQ-529

1) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the Product (Chip + Package) was simulated on a 76.2 × 114.3 × 1.5 mm board with two inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at T_{AMB} = 105°C and $P_{dissipation}$ = 1 W.

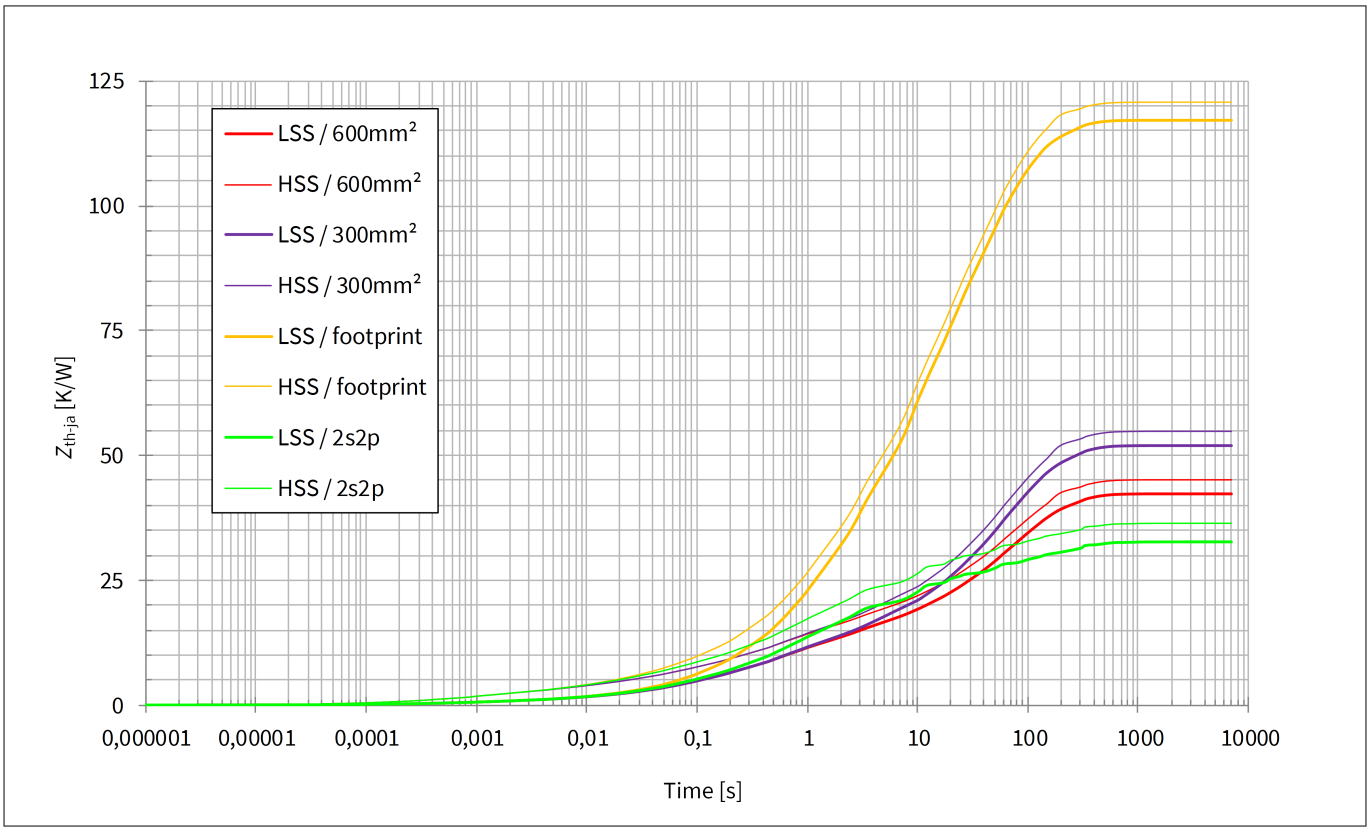


Figure 5 Typical thermal impedance for $T_{ambient}$ = 85°C; Simulation with 1 W of power dissipation

4 Logic pins

The device has 3 digital pins for direct control of the device.

The logic thresholds for "low" and "high" states are defined by parameters $V_{DI(TH)}$ and $V_{DI(HYS)}$. The relationship between these two values is shown in ***Figure 6***. The voltage V_{IN} needed to ensure an "high" state is always higher than the voltage needed to ensure a "low" state. The digital input pins are compatible with 3.3 V and 5 V micro-controllers.

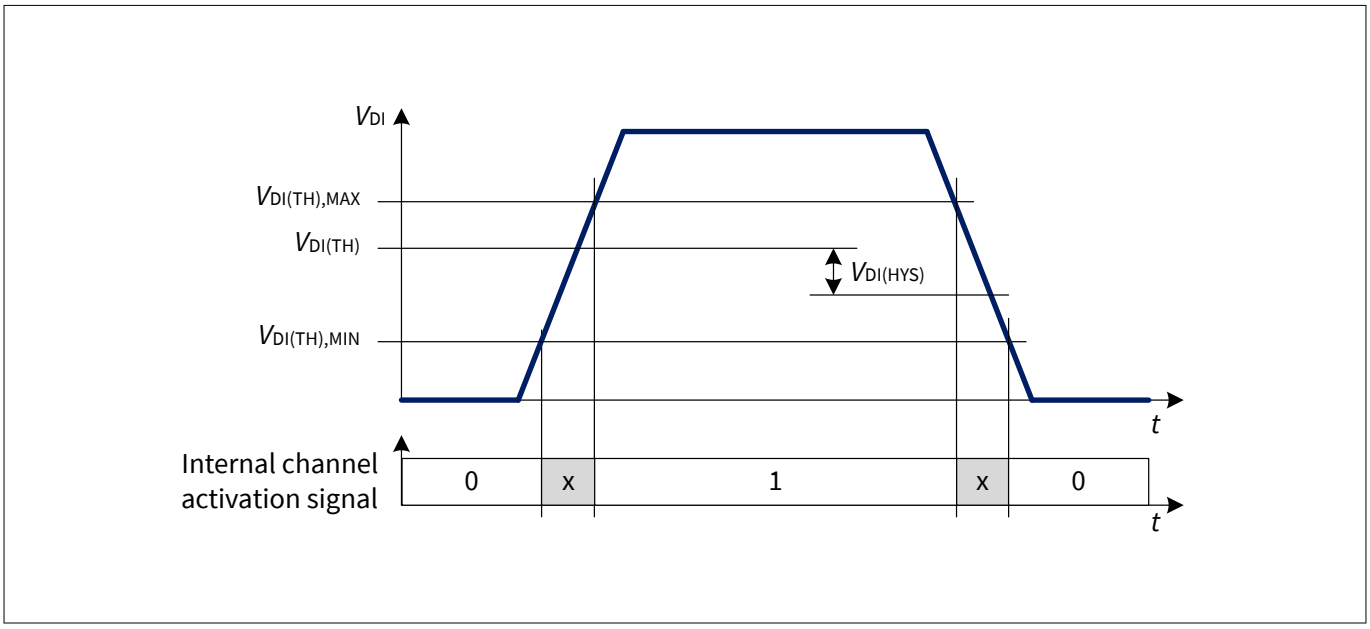


Figure 6 Input Threshold voltages and hysteresis

4.1 Input pin (IN)

The input pin IN activates either the low-side or the high-side output stage, in case the enable pin EN is set to "high" and no fault is present.

4.2 Enable pin (EN)

The Enable (EN) pin activates the device. When EN pin is set to "high", the device is in Active mode. When it is set to "low", the device goes into Sleep mode, with the output stage set to tri-state (low-side and high-side switches are set OFF). The protection latch is cleared by a "low" signal with a minimum length of $t_{DELAY(LR)}$ at the EN pin.

4.3 Diagnosis Enable pin (DEN)

The Diagnosis Enable (DEN) pin controls the diagnosis circuitry and the protection circuitry. When DEN pin is set to "high", the diagnosis is enabled (see ***Chapter 8.2*** for more details). When it is set to "low", the diagnosis is disabled (IS pin is set to high impedance).

The transition from "high" to "low" of DEN pin clears the protection latch of the channel depending on the logic state of EN pin and DEN pulse length (see ***Chapter 7.3*** for more details).

4.4 Electrical characteristics logic pins

Table 6 Electrical characteristics logic pins

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C; Digital Input (DI) pins = IN, DEN, EN; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Digital input voltage threshold	$V_{DI(TH)}$	0.8	1.3	2	V	See ***Figure 6***	PRQ-52
Digital input clamping voltage	$V_{DI(CLAMP1)}$	–	7	–	V	*1)* I_{DI} = 1 mA	PRQ-53
Digital input clamping voltage	$V_{DI(CLAMP2)}$	6.5	7.5	8.5	V	I_{DI} = 2 mA	PRQ-54
Digital input hysteresis	$V_{DI(HYS)}$	–	0.25	–	V	*1)* See ***Figure 6***	PRQ-56
Digital input current ("high")	$I_{DI(H)}$	2	10	25	µA	V_{DI} = 2 V	PRQ-57
Digital input current ("low")	$I_{DI(L)}$	2	10	25	µA	V_{DI} = 0.8 V	PRQ-58

1) Not subject to production test - specified by design

5 Power supply

The BTN7030-1EPA is supplied by V_S, which is used for the internal logic as well as supply for the power output stage. V_S has an undervoltage detection circuit, which prevents the activation of the power output stage and diagnosis in case the applied voltage is below the undervoltage threshold.

5.1 Operation modes

BTN7030-1EPA has three operation modes, with the transition between the operation modes is determined according to these variables:

- logic level at EN pin
- logic level at DEN pin

The state diagram including the operation modes and the possible transitions is shown in ***Figure 7***. The behavior of BTN7030-1EPA as well as some parameters may change in dependence from the operation mode of the device. Furthermore, due to the undervoltage detection circuitry which monitors V_S supply voltage, some changes within the same operation mode can be seen accordingly. In case of a fault, the BTN7030-1EPA will not go into sleep mode, unitl the latch is cleared.

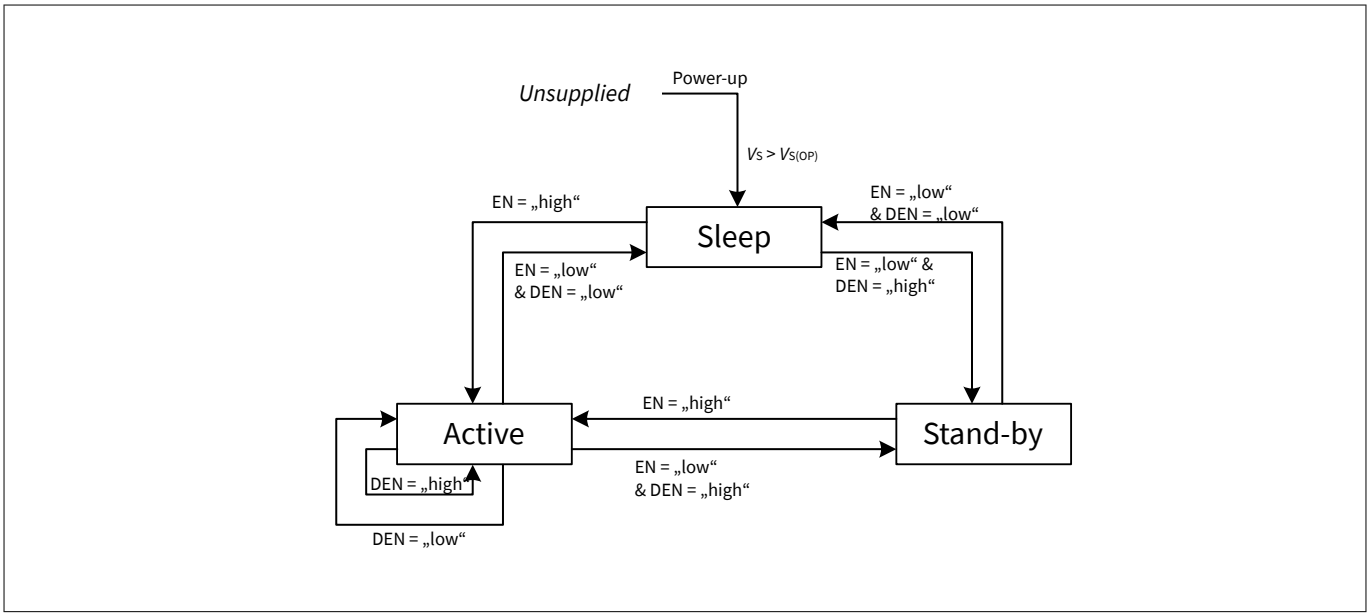


Figure 7 Operation mode state diagram

5.1.1 Unsupplied

In this state, the device is either unsupplied (no voltage applied to VS pin) or the supply voltage is below the undervoltage threshold.

5.1.2 Power-up

The Power-up condition is entered when the supply voltage (V_S) is applied to the device. The supply is rising until it is above the undervoltage threshold $V_{S(OP)}$ therefore the internal power-on signals are set.

5.1.3 Sleep mode

The device is in Sleep mode when all Digital Input pins (IN, DEN, EN) are set to "low". When BTN7030-1EPA is in Sleep mode, both high-side and low-side power stages are OFF. The current consumption is minimum (see

parameter $I_{VS(SLEEP)\_85\_stdy}$). No Overtemperature or Overload protection mechanism is active when the device is in Sleep mode, only the InverseON protection for the low-side power output stage is active (see ***Chapter 6.3.1*** for further details). In case of activation, the current consumption of the device is increased.The device can go in Sleep mode only if the protection is not active (latch = 0, see ***Chapter 7.3.1*** for further details).

5.1.4 Stand-by mode

The device is in Stand-by mode as long as DEN pin is set to "high" while the EN pin is set to "low". Both the high-side and low-side power stages are OFF, therefore only Open Load in OFF diagnosis is possible. Depending on the load condition, either a fault current $I_{IS(FAULT)}$ or an Open Load in OFF current $I_{IS(OLOFF)}$ may be present at IS pin. In such a situation, the current consumption of the device is increased.

5.2 Undervoltage on VS

Between $V_{S(OP)}$ and $V_{S(UV)}$ the undervoltage mechanism is triggered. If the device is operative (in Active mode) and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the internal logic switches OFF the output channel.

As soon as the supply voltage V_S is above the operative threshold $V_{S(OP)}$, the channel is switched ON again with a hysteresis of $V_{S(HYS)}$.

5.3 Electrical characteristics power supply

Table 7 Electrical characteristics power supply

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C

Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply undervoltage shutdown	$V_{S(UV)}$	1.8	2.7	3.5	V	V_S decreasing EN = "high" From $V_{DS} \le 0.5$ V to $V_{DS} = V_S$	PRQ-63
Power supply minimum operating voltage	$V_{S(OP)}$	2.0	3.0	3.8	V	V_S increasing EN = "high" From $V_{DS} = V_S$ to $V_{DS} \le 0.5$ V	PRQ-65
Power supply undervoltage shutdown hysteresis	$V_{S(HYS)}$	–	0.3	–	V	*1)* $V_{S(OP)} - V_{S(UV)}$	PRQ-67
Power supply current consumption in sleep mode with loads at TJ ≤ 85°C after settling time	$I_{VS(SLEEP)\_85\_stdy}$	-	0.01	3	µA	*1)* V_S = 18 V EN = IN = DEN = “low” OUT = “floating” steady state $T_J \le 85$ °C	PRQ-70

(table continues...)

Table 7 (continued) Electrical characteristics power supply

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Power supply current consumption in sleep mode with loads at TJ = 150°C after settling time	$I_{VS(SLEEP)\_150\_stdy}$	-	8	20	µA	*1)* V_S = 18 V EN = IN = DEN = “low” OUT = “floating” steady state T_J = 150°C	PRQ-72
Operating current in active mode (GND)	$I_{GND(ACTIVE)}$	–	2	5	mA	V_S =18 V EN = IN = DEN = "high"	PRQ-73
Operating current in active mode (VS)	$I_{VS(ACTIVE)}$	–	2	5	mA	V_S =18 V IN = "low" EN = DEN = "high" fault-latch ≠ 0	PRQ-74
Operating current in stand-by mode/OLOFF	$I_{GND(STBY)}$	–	1.2	1.8	mA	V_S = 18 V EN = IN = "low" DEN = "high"	PRQ-76
Operating current during low-side inverseON activation	$I_{VS(INVON)(LS)}$	–	–	5	mA	V_S = 6 V I_L = -200 mA EN = IN = "low"	PRQ-77

1) Not subject to production test - specified by design

6 Power stages

The high-side power stage is built using a N-channel vertical Power MOSFET with charge pump, while the low-side power stage uses no charge pump.

6.1 Output ON-state resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature T_J. ***Figure 8*** shows the variation of $R_{DS(ON)}$ across the whole T_J range. The value "2" on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at T_J = 150°C.

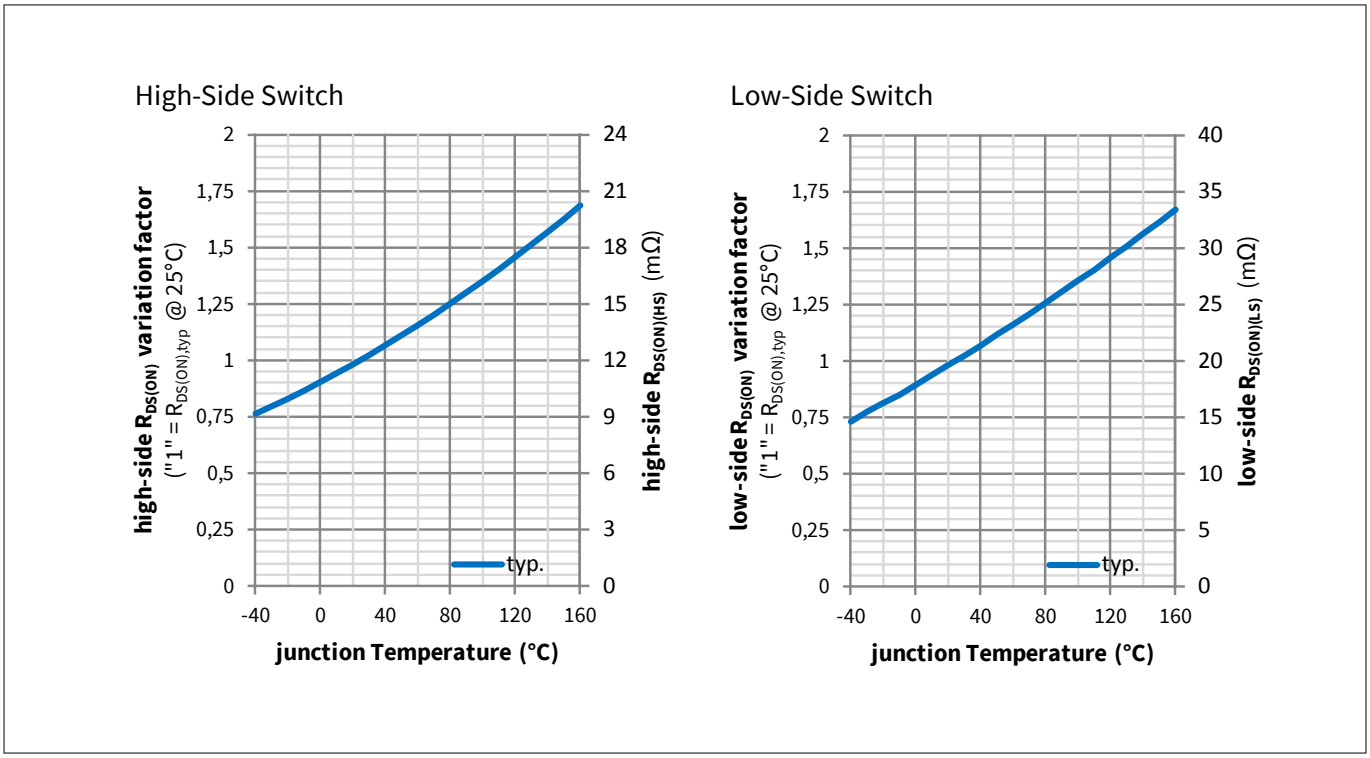


Figure 8 Typical $R_{DS(ON)}$ vs. junction temperature for low-side and high-side output stage

6.2 Switching loads

6.2.1 Switching times

When switching resistive loads, the switching times and slew rates shown in ***Figure 9*** and ***Figure 10*** can be considered. The switch energy values $E_{ON(xS)}$ and $E_{OFF(xS)}$ are proportional to the load resistance and times $t_{ON(xS)}$ and $t_{OFF(xS)}$.

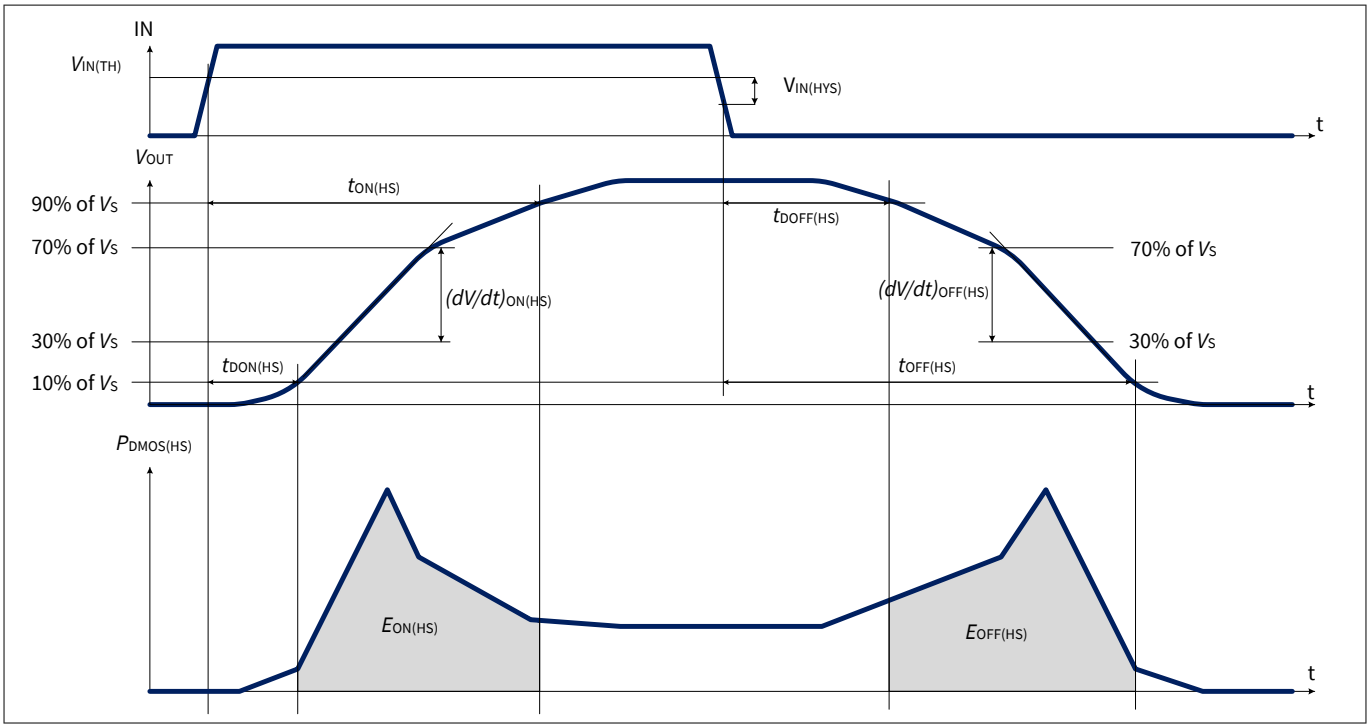


Figure 9 Switching a resistive load to ground (high-side), for EN="high"

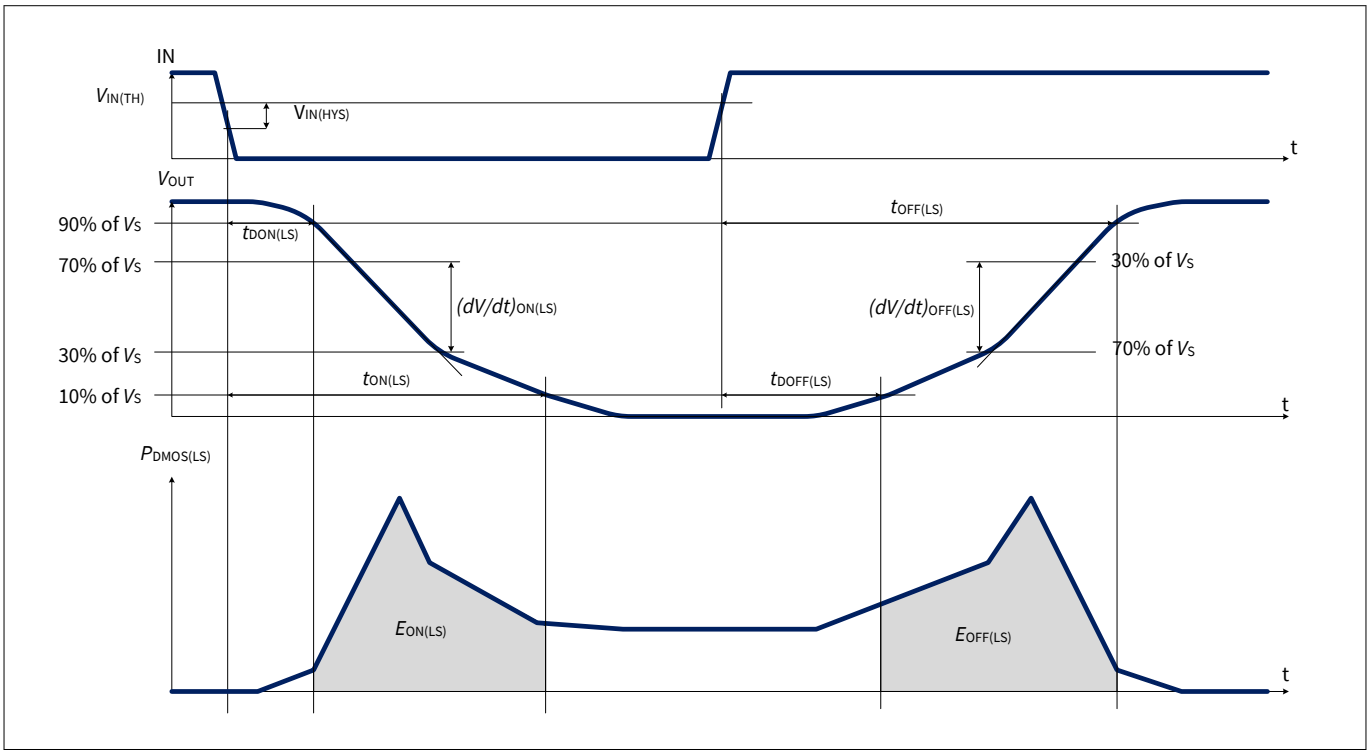


Figure 10 Switching a resistive load to supply voltage (low-side), for EN="high"

6.2.2 Output voltage limitation

To increase the current sense accuracy of the high-side output stage, V_{DS} voltage is monitored.

When the output current I_L decreases while the channel is diagnosed (DEN pin set to "high" - see ***Figure 11***) bringing V_{DS} equal or lower than $V_{DS(SLC)(HS)}$, the output DMOS gate is partially discharged. This increases the output resistance so that $V_{DS} = V_{DS(SLC)(HS)}$ even for very small output currents.

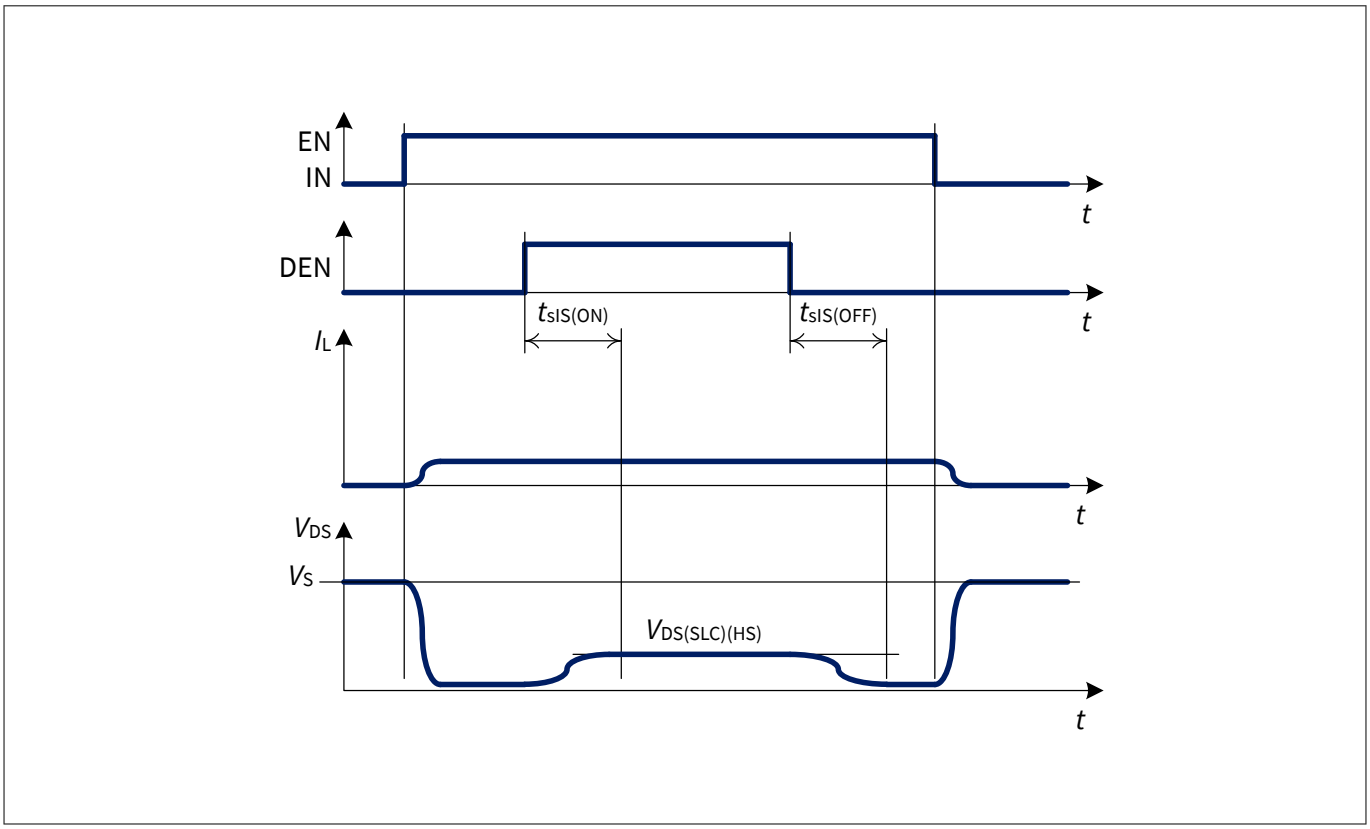


Figure 11 Output voltage limitation activation during diagnosis, with EN="high"

The V_{DS} increase allows the current sensing circuitry to work more efficiently, providing better k_{ILIS} accuracy for output current in the low range.

6.3 Advanced switching characteristics

6.3.1 Inverse current behavior for the high-side switch

When $V_{OUT} > V_S$, a current I_{INV} flows into the high-side power output transistor (see ***Figure 12***). Similar for V_{OUT} < GND (0 V), a current I_{INV} flows into the low-side power output transistor. This condition is known as "Inverse Current".

If the channel is in OFF- state, the current flows through the intrinsic body diode generating high power losses therefore an increase of overall device temperature. If the channel is in ON- state, $R_{DS(INV)}$ can be expected and power dissipation in the output stage is comparable to normal operation in $R_{DS(ON)}$.

With InverseON, it is possible to switch ON or OFF the high-side power output channel during inverse current condition.

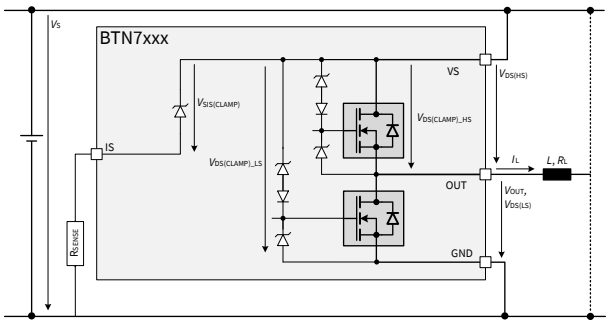


Figure 12 Inverse current circuitry for low-side and high-side

6.3.2 Inverse current behavior for the low-side switch

With InverseON, the low-side power output channel is activated under all operational conditions for $V_{OUT} < V_{INV(LS)}$, also in case of any fault to protect the low-side power output transistor.

The circuitry is active in any operational condition, fault condition, stand-by or sleep mode.

The power supply consumption for voltage monitoring, without activation of the power output stage, is included in ***Table 7***. In case of activation of the low-side power output stage, when switched on by the protection circuitry, an operating supply current of $I_{VS(INVON)(LS)}$ is required during activation.

When V_{OUT} is small again, the low-side output-stage is switched according to the EN and IN pin.

Note: No protection mechanism like Overtemperature or Overload protection is active during applied Inverse Currents for both low-side and high-side output transistor.

6.4 Electrical characteristics power stages

Table 8 Electrical characteristics power stages switching

T_J = -40°C to +150°C; R_{load} = 3.3 Ω, single pulse,
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
High-side switch timings							
Switch-ON delay, high-side switch	$t_{DON(HS)}$	30	60	110	µs	V_S =13.5 V V_{OUT} = 10% V_S See ***Figure 9***	PRQ-146
Switch-OFF delay, high-side switch	$t_{DOFF(HS)}$	10	33	60	µs	V_S =13.5 V V_{OUT} = 90% V_S See ***Figure 9***	PRQ-147
Switch-ON time, high-side switch	$t_{ON(HS)}$	45	85	135	µs	V_S =13.5 V V_{OUT} = 90% V_S See ***Figure 9***	PRQ-148

(table continues...)

Table 8 (continued) Electrical characteristics power stages switching

T_J = -40°C to +150°C; R_{load} = 3.3 Ω, single pulse,
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switch-OFF time, high-side switch	$t_{OFF(HS)}$	25	55	82	µs	V_S = 13.5 V V_{OUT} = 10% V_S See ***Figure 9***	PRQ-149
Switch-ON/OFF matching tON-tOFF, high-side switch	$\Delta t_{SW(HS)}$	0	35	70	µs	V_S = 13.5 V See ***Figure 9***	PRQ-150
Blank time between switches activation HS to LS (to avoid cross-current)	$t_{BLANK(HS-LS)}$	–	20	–	µs	V_S = 13.5 V	PRQ-528
Low-side switch timings							
Switch-ON delay, low-side switch	$t_{DON(LS)}$	50	90	130	µs	V_S = 13.5 V V_{OUT} = 90% V_S See ***Figure 10***	PRQ-151
Switch-OFF delay, low-side switch	$t_{DOFF(LS)}$	10	33	60	µs	V_S = 13.5 V V_{OUT} = 10% V_S See ***Figure 10***	PRQ-152
Switch-ON time, low-side switch	$t_{ON(LS)}$	70	115	160	µs	V_S = 13.5 V V_{OUT} = 10% V_S See ***Figure 10***	PRQ-153
Switch-OFF time, low-side switch	$t_{OFF(LS)}$	25	55	85	µs	V_S = 13.5 V V_{OUT} = 90% V_S See ***Figure 10***	PRQ-154
Switch-ON/OFF matching tON-tOFF, low-side switch	$\Delta t_{SW(LS)}$	25	60	95	µs	V_S = 13.5 V See ***Figure 10***	PRQ-155
Blank time between switches activation LS to HS (to avoid cross-current)	$t_{BLANK(LS-HS)}$	–	40	–	µs	V_S = 13.5 V	PRQ-156
High-side switch voltage slope							
Switch-ON slew rate, high-side switch	$(dV/dt)_{ON(HS)}$	0.35	0.6	0.9	V/µs	V_S = 13.5 V V_{OUT} = 30% to 70% of V_S	PRQ-157
Switch-OFF slew rate, high-side switch	$-(dV/dt)_{OFF(HS)}$	0.35	0.6	0.9	V/µs	V_S = 13.5 V V_{OUT} = 70% to 30% of V_S	PRQ-158
Low-side switch voltage slope							
Switch-ON slew rate, low-side switch	$-(dV/dt)_{ON(LS)}$	0.35	0.6	0.9	V/µs	V_S =13.5 V V_{OUT} = 70% to 30% of V_S	PRQ-160
Switch-OFF slew rate, low-side switch	$(dV/dt)_{OFF(LS)}$	0.35	0.6	0.9	V/µs	V_S = 13.5 V V_{OUT} = 30% to 70% of V_S	PRQ-161
High-side voltages							

(table continues...)

Table 8 (continued) Electrical characteristics power stages switching

T_J = -40°C to +150°C; R_{load} = 3.3 Ω, single pulse,
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Output voltage drop limitation at small load currents	$V_{DS(SLC)(HS)}$	2	7	18	mV	I_{OUT} = $I_{OUT(OL)}$ = 20 mA IN=DEN=EN="high"	PRQ-163

Table 9 Electrical characteristics - power output stages

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
12 mΩ high-side							
Output characteristics							
ON-state resistance at TJ = 25°C, high-side switch	$R_{DS(ON)\_25(HS)}$	–	12	–	mΩ	1) T_J = 25 °C	PRQ-164
ON-state resistance at TJ = 150°C, high-side switch	$R_{DS(ON)\_150(HS)}$	–	–	25.5	mΩ	T_J = 150°C	PRQ-165
ON-state resistance in inverse current at TJ = 150°C, high-side switch	$R_{DS(INV)\_150(HS)}$	–	–	26	mΩ	T_J = 150°C V_S = 13.5 V I_L = -4 A See ***Figure 12***	PRQ-168
Output leakage current at TJ ≤ 85°C, high-side switch	$I_{L(OFF)\_85(HS)}$	–	0.01	1	µA	1) V_{OUT} = 0 V EN = "low" T_A ≤ 85°C	PRQ-169
Output leakage current at TJ = 150°C, high-side switch	$I_{L(OFF)\_150(HS)}$	–	16	43	µA	V_{OUT} = 0 V EN = "low" T_A = 150°C	PRQ-170
Voltages							
Drain source diode voltage at -40°C, high-side switch	$\lvert V_{DS(DIODE)\_-40(HS)}\rvert$	–	800	–	mV	1) I_L = -190 mA T_J = -40°C	PRQ-536
Drain source diode voltage at 25°C, high-side switch	$\lvert V_{DS(DIODE)\_25(HS)}\rvert$	–	700	–	mV	1) I_L = -190 mA T_J = 25°C	PRQ-537
Drain source diode voltage at 150°C, high-side switch	$\lvert V_{DS(DIODE)\_150(HS)}\rvert$	–	500	650	mV	I_L = -190 mA T_J = 150°C	PRQ-172
Switching energy							

(table continues...)

Table 9 (continued) Electrical characteristics - power output stages

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switch-ON energy, high-side switch	$E_{ON(HS)}$	–	0.44	–	mJ	1) V_S = 18 V See ***Figure 9***	PRQ-173
Switch-OFF energy, high-side switch	$E_{OFF(HS)}$	–	0.49	–	mJ	1) V_S = 18 V See ***Figure 9***	PRQ-174
20 mΩ low-side							
Output characteristics							
ON-state resistance at TJ = 25°C, low-side switch	$R_{DS(ON)\_25(LS)}$	–	20	–	mΩ	1) T_J = 25°C	PRQ-175
ON-state resistance at TJ = 150°C, low-side switch	$R_{DS(ON)\_150(LS)}$	–	–	36.5	mΩ	T_J = 150°C	PRQ-176
ON-state resistance in inverse current at TJ = 150°C, low-side switch	$R_{DS(INV)\_150(LS)}$	–	–	40	mΩ	T_J = 150°C V_S = 13.5 V I_L = -4 A See ***Figure 12***	PRQ-179
Output leakage current at TJ ≤ 85°C, low-side switch	$I_{L(OFF)\_85(LS)}$	–	0.05	5	µA	1) V_{OUT} = V_S EN = "low" T_A ≤ 85°C	PRQ-190
Output leakage current at TJ = 150°C, low-side switch	$I_{L(OFF)\_150(LS)}$	–	2	117	µA	V_{OUT} = V_S EN = "low" T_A = 150°C	PRQ-181
Voltages							
Drain source diode voltage at -40°C, low-side switch	$\lvert V_{DS(DIODE)\_-40(LS)}\rvert$	–	600	–	mV	1) I_L = -190 mA T_J = -40°C	PRQ-539
Drain source diode voltage at 25°C, low-side switch	$\lvert V_{DS(DIODE)\_25(LS)}\rvert$	–	700	–	mV	1) I_L = -190 mA T_J = 25°C	PRQ-538
Drain source diode voltage at 150°C, low-side switch	$\lvert V_{DS(DIODE)\_150(LS)}\rvert$	–	500	650	mV	I_L = -500 mA T_J = 150 °C	PRQ-183
Voltage threshold for first inverse current low-side activation, low-side switch	$V_{INV(LS)}$	–	-300	–	mV	1) EN = IN = DEN = “low” V_S = 6 V I_L = -200 mA	PRQ-184
Switching energy							

(table continues...)

Table 9 (continued) Electrical characteristics - power output stages

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Switch-ON energy, low-side switch	$E_{ON(LS)}$	–	0.42	–	mJ	1) V_S = 18 V See ***Figure 10***	PRQ-187
Switch-OFF energy, low-side switch	$E_{OFF(LS)}$	–	0.46	–	mJ	1) V_S = 18 V See ***Figure 10***	PRQ-188

1) Not subject to production test - specified by design

7 Protection

The BTN7030-1EPA is protected against overtemperature, overload and overvoltage.

Overtemperature and overload protections are working when the device is not in sleep mode.

Overvoltage protection works in all operation modes.

7.1 Overtemperature protection

An increase of the junction temperature T_J above the thresholds $T_{J(SD)}$ switches OFF both the high-side and low-side output stages to prevent destruction. The channel remains switched OFF until the temperature has reached the "Restart" condition described in ***Table 10***. The behavior is shown in ***Figure 13***. From protection point of view, pins IN and EN are equivalent.

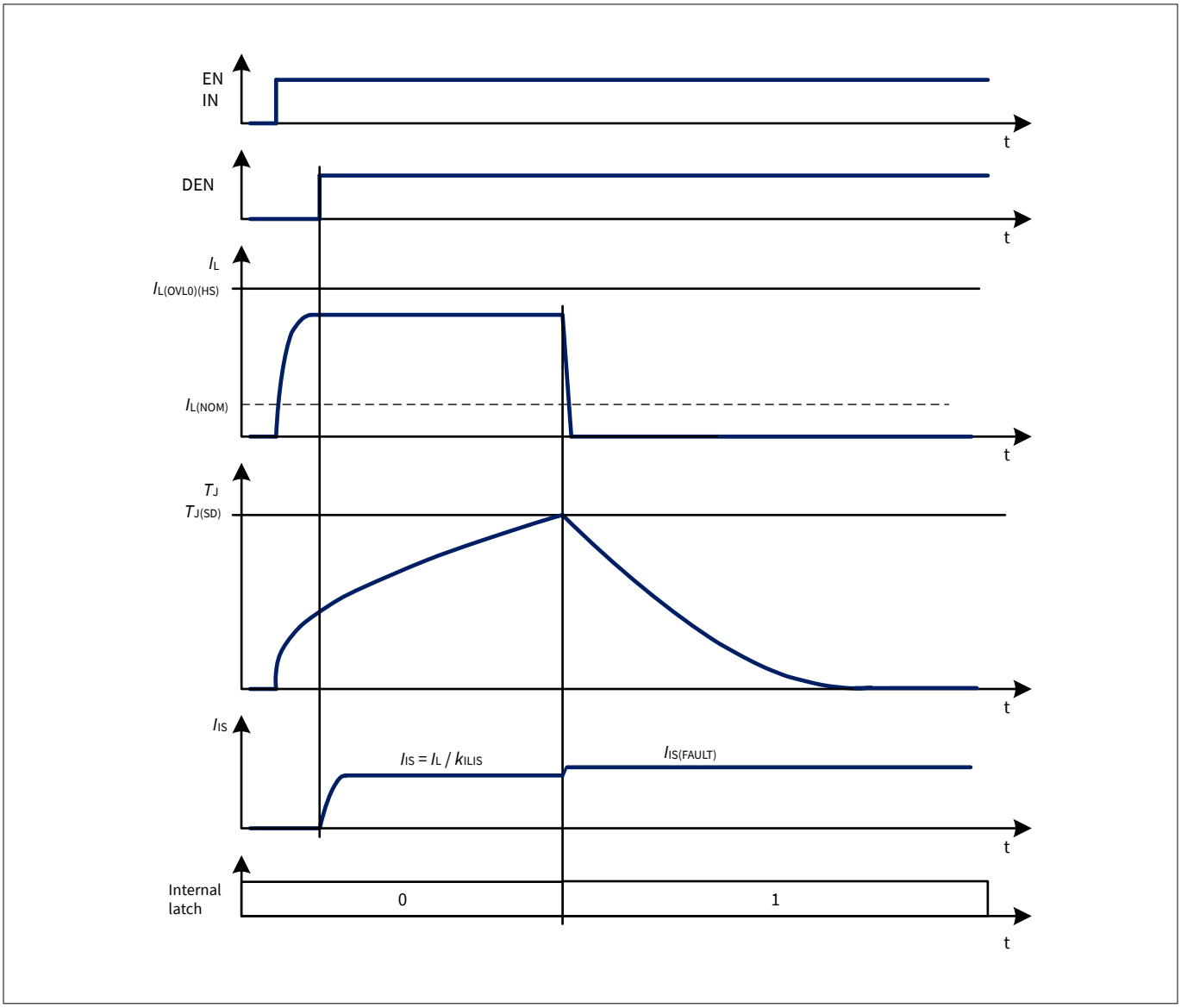


Figure 13 Overtemperature protection, with EN = "high" and load to GND

When the overtemperature protection circuitry allows the channel to be switched ON again, the Intelligent latch strategy described in ***Chapter 7.3.1*** is followed.

7.2 Overload protection

The BTN7030-1EPA is protected in case of overload, short circuit to battery (low-side output stage) or short circuit to ground (high-side output stage). For the high-side output stage, two overload thresholds are defined (see ***Figure 14***) and selected automatically depending on the voltage V_{DS} across the power DMOS:

Overload current thresholds variation with V_{DS} for the high-side output stage

- $I_{L(OVL0)}$ when V_{DS} < 13 V
- $I_{L(OVL1)}$ when V_{DS} > 22 V

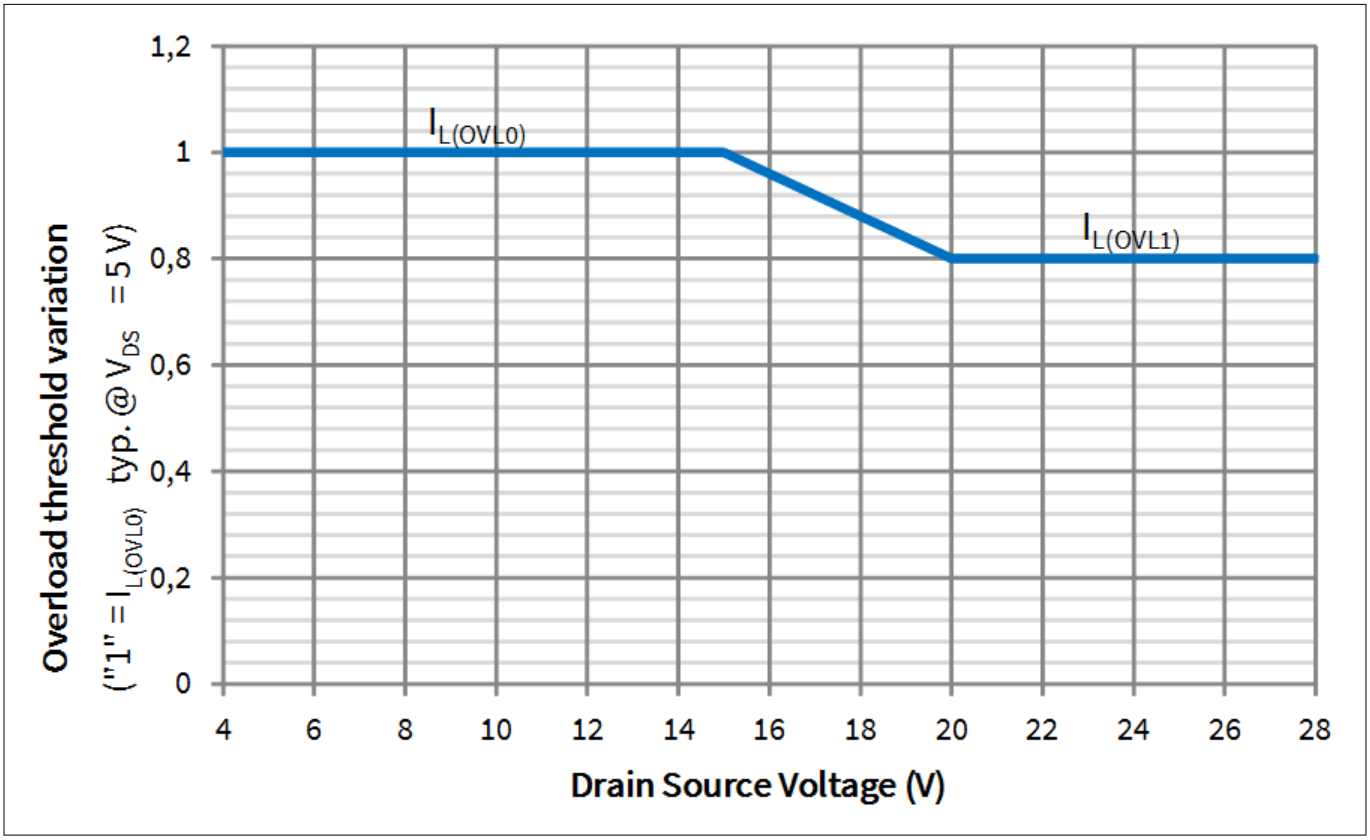


Figure 14 Typical Overload current thresholds variation with VDS for the high-side output stage

In order to allow a higher load inrush at low ambient temperature, the overload threshold for the high-side output stage is maximum at low temperature and decreases when T_J increases (see ***Figure 15***).

For the high-side output stage, $I_{L(OVL0)}$ typical value remains constant up to a junction temperature of +75°C.

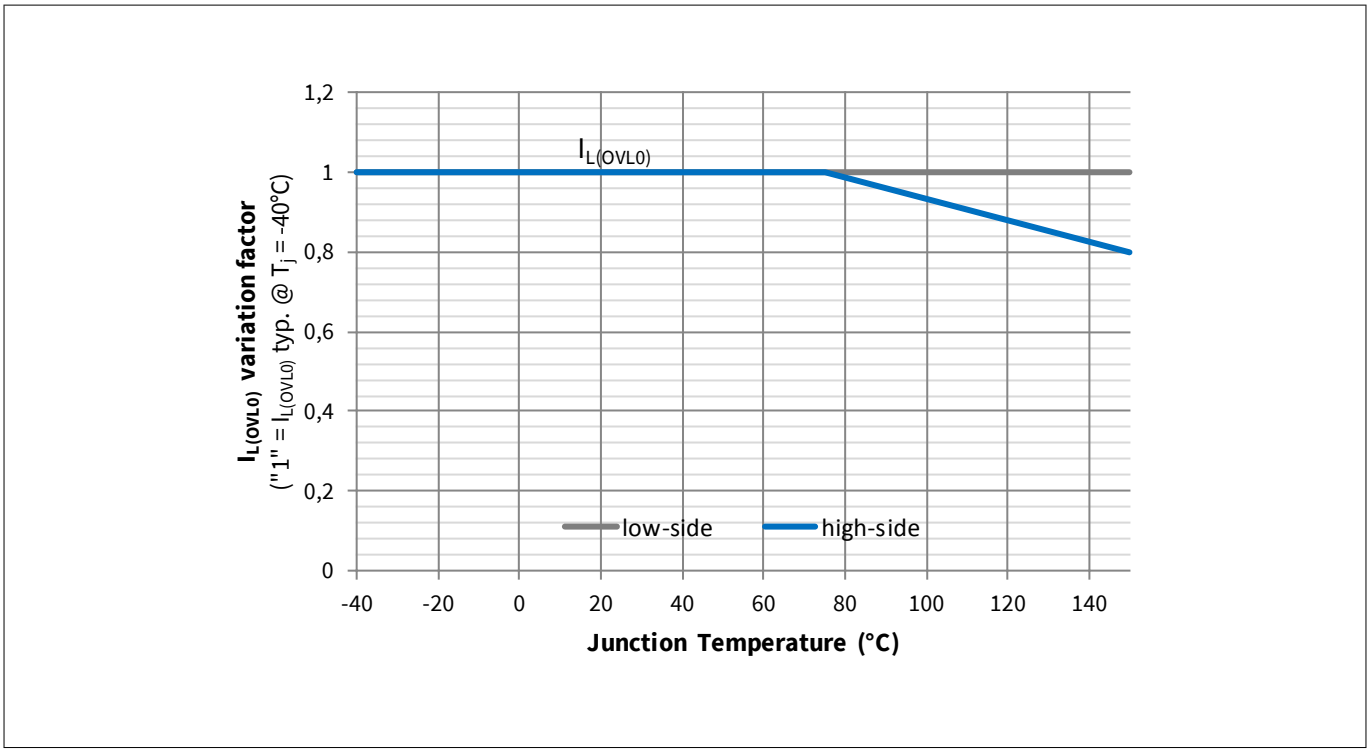


Figure 15 Overload current thresholds variation with T_J

The power supply voltage V_S can increase above 18 V for short time, for instance in load dump or in jump start condition. Whenever $V_S \geq V_{S(JS)}$, the overload detection current for the high-side output stage is set to $I_{L(OVL\_JS)(HS)}$ as shown in ***Figure 16***.

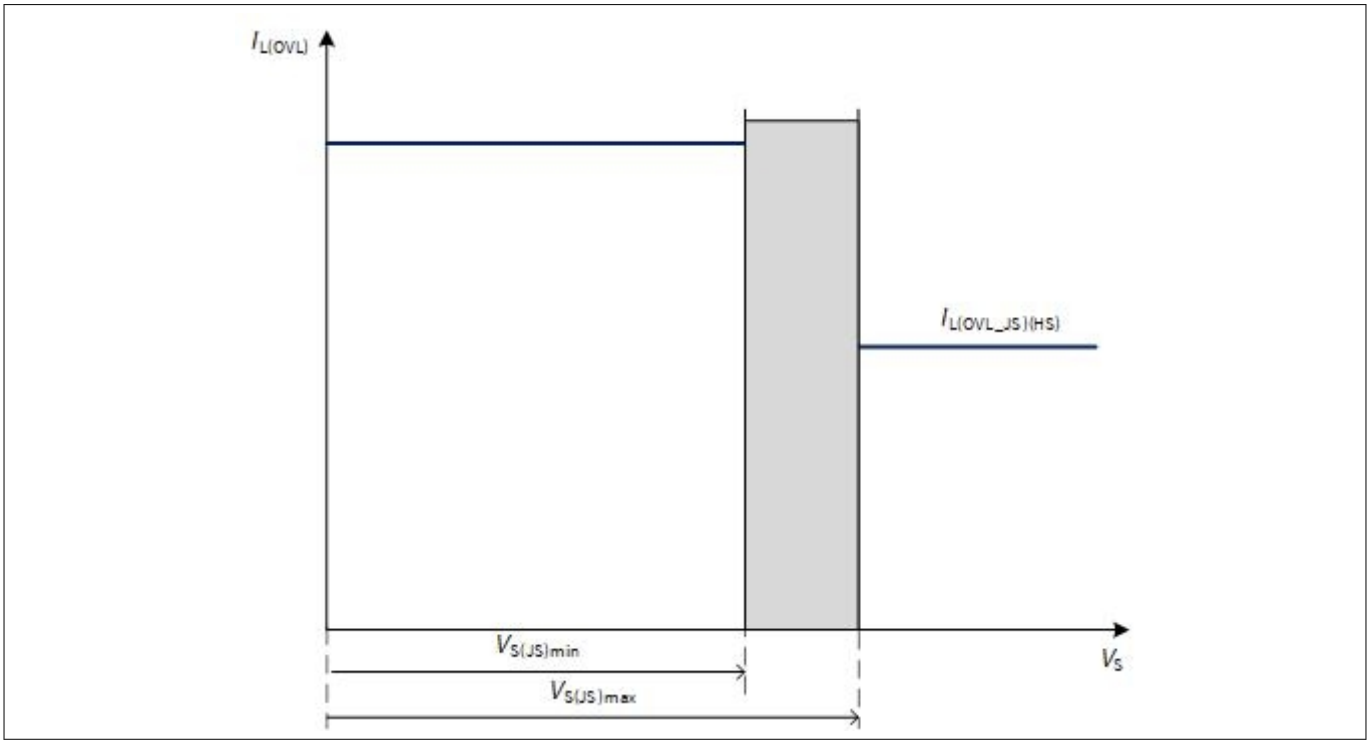


Figure 16 Overload detection current variation with V_S voltage for the high-side output stage

When $I_L \geq I_{L(OVL)}$ (either $I_{L(OVL0)}$ or $I_{L(OVL1)}$, in either the low-side or high-side output stages) the output stage is switched OFF (both low-side and high-side). The output stage is allowed to be reactivated according to the strategy described in ***Chapter 7.3***.

7.3 Protection and diagnosis in case of fault

Any event that triggers a protection mechanism (either Overtemperature or Overload) has consequences:

- the output stage switches OFF and the internal latch is set to "1"
- if the diagnosis is active for the channel, a current $I_{IS(FAULT)}$ is provided by IS pin (see ***Chapter 8.2.2*** for further details)

If all the "restart" conditions described in ***Table 10*** are fullfilled, the latch can be reset, thus the output stage can be switched ON again.

Furthermore, the device has the intelligent latch to protect itself against unwanted repetitive restart in fault condition.

Table 10 Protection “restart” condition

Fault condition	Switch OFF event	"Restart" Condition
Overtemperature	$T_J \geq T_{J(SD)}$	$T_J < T_{J(SD)} - T_{J(HYS)}$
Overload	$I_L \geq I_{L(OVL)}$	$I_L < 50$ mA

7.3.1 Intelligent latch strategy (INTLAT)

When EN is set to "high", the channel is switched ON. In case of fault condition the output stage latches OFF. There are two ways to de-latch the switch.

With EN pin:

It is necessary to set the pin to "low" for a time longer than $t_{DELAY(LR)}$ ("latch reset delay" time) to de-latch the channel. This is independent from the state of the IN pin. The channel can be allowed to restart only if the "restart" conditions for the protection mechanisms are fulfilled (see ***Table 10***).

During the "latch reset delay" time, if the pin is set to "high" the channel remains switched OFF and the timer $t_{DELAY(LR)}$ is reset and it is not started as long as the pin remains at "high". It restarts as soon as the pin is set to "low" again.

The intelligent latch strategy is shown in ***Figure 17***.

With DEN pin:

It is possible to "force" a reset of the internal latch without waiting for $t_{DELAY(LR)}$ by applying a pulse (rising edge followed by a falling edge) to the DEN pin while EN pin is "low". The pulse applied to DEN pin must have a duration longer than $t_{DEN(LR)}$ to ensure a reset of the internal latch.

The timing is shown in ***Figure 18***.

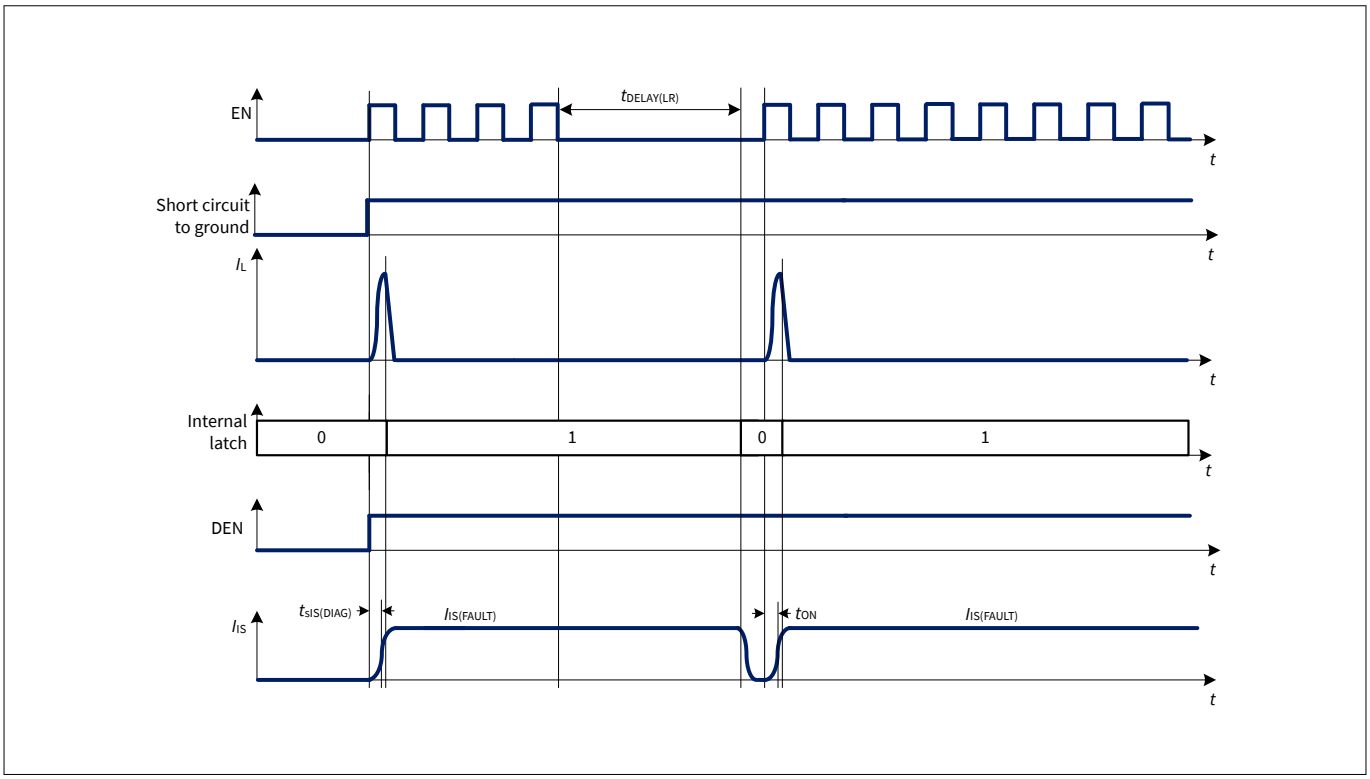


Figure 17 **Intelligent latch timing diagram, with IN = ”high” and load to GND**

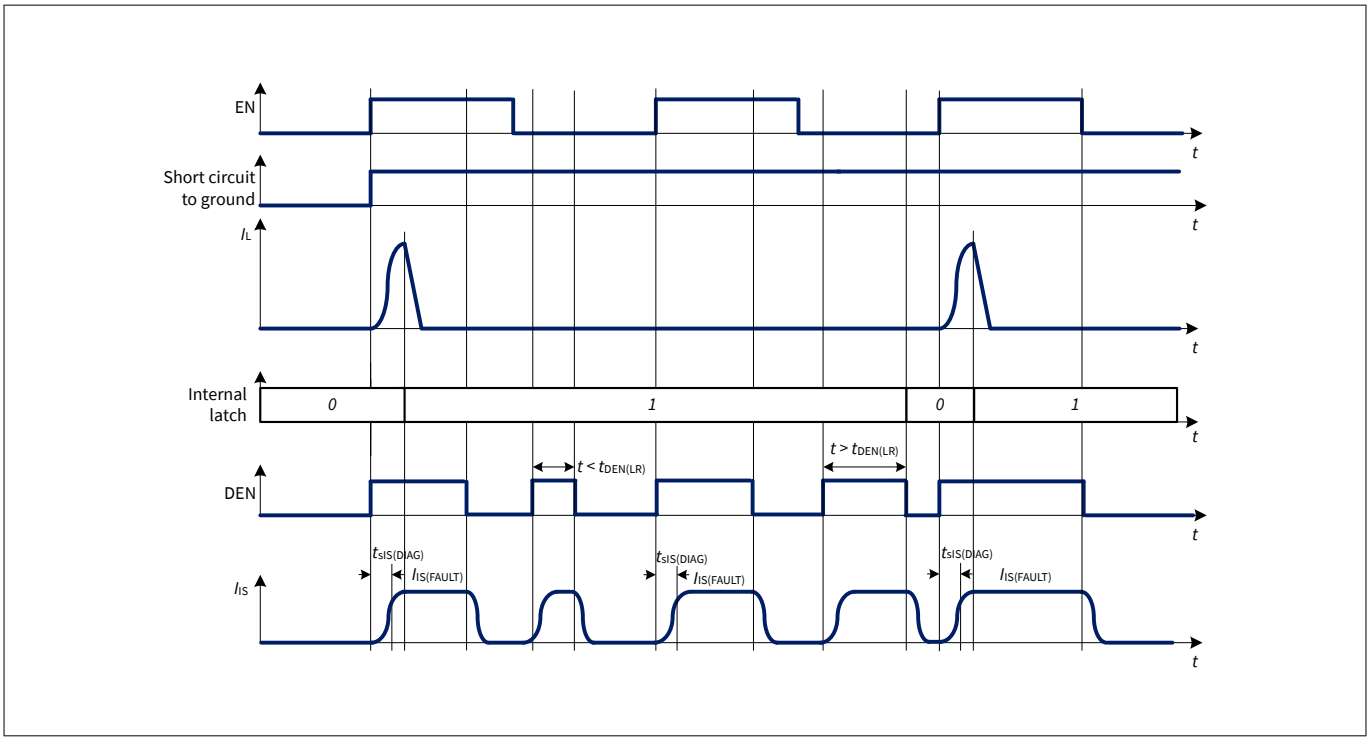


Figure 18 **Intelligent latch timing diagram with forced reset, with IN = “high” and load to GND**

7.4 Additional protections

7.4.1 Overvoltage protection

The clamping structure limits the negative / positive output voltage so that $V_{DS(xS)} = V_{DS(CLAMP)}$, for both the high-side and low-side output stage. The clamping structure protects the device in all operative modes listed in Chapter ***Chapter 6.1***.

In the case of supply voltages between $V_{S(EXT,UP)}$ and $V_{BAT(LD)}$, the output transistor is still operational and follows the input pin.

In addition, there is a clamp mechanism available for Overvoltage protection for the logic and the output channel, monitoring the voltage between VS and GND pins ($V_{S(CLAMP)}$).

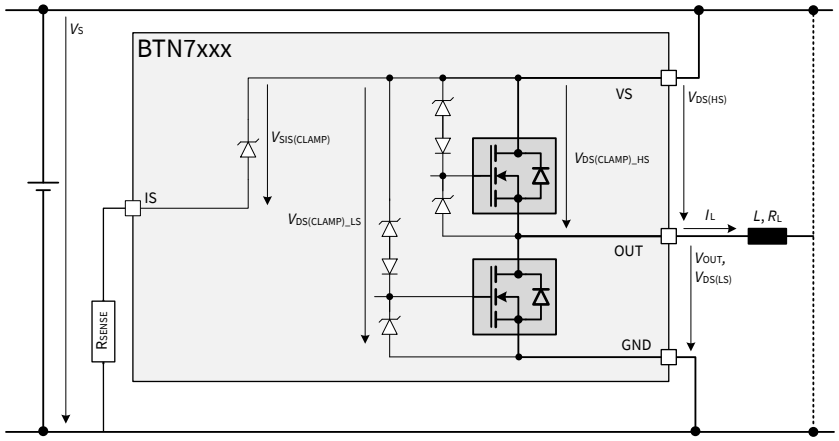


Figure 19 Output clamp concept

7.4.2 Cross current protection

In half-bridge applications it has to be assured that the high-side and low-side power output stages are not conducting at the same time, connecting directly the battery voltage to GND. This is assured by a circuit in the driver logic, generating a so called dead time between switching off one power output stages and switching on the other. This is ensured by monitoring the state of the MOSFETs.

7.5 Electrical characteristics protection

Table 11 Electrical characteristics protection

V_S = 6 V to 18 V, T_J = -40°C to +150°C; typical values: V_S= 13.5 V, T_J = 25 °C; typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Thermal shutdown temperature	$T_{J(SD)}$	150	175	200	°C	1) 2) See ***Figure 13***	PRQ-191
Thermal shutdown hysteresis	$T_{J(HYS)}$	–	30	–	K	3) See ***Figure 13***	PRQ-193
Drain to source clamping voltage at TJ = -40°C for HS and LS switches	$V_{DS(CLAMP)\_-40}$	33	36.5	42	V	I_L = |5 mA| T_J = -40°C See ***Figure 19***	PRQ-144
Drain to source clamping voltage at TJ ≥ 25 °C for HS and LS switches	$V_{DS(CLAMP)\_25}$	35	38	44	V	2) I_L = |5 mA| T_J ≥ 25°C See ***Figure 19***	PRQ-145
Power supply clamping voltage at TJ = -40°C	$V_{S(CLAMP)\_-40}$	33	36.5	42	V	I_{VS} = 5 mA T_J = -40°C See ***Figure 19***	PRQ-197
Power supply clamping voltage at TJ ≥ 25°C	$V_{S(CLAMP)\_25}$	35	38	44	V	2) I_{VS} = 5 mA T_J ≥ 25 °C See ***Figure 19***	PRQ-198
Power supply voltage threshold for overcurrent threshold reduction in case of short circuit	$V_{S(JS)}$	20.5	22.5	24.5	V	3) Setup acc. to AEC-Q100-012	PRQ-199
Protection timings							
Latch reset delay time after fault condition	$t_{DELAY(LR)}$	40	70	100	ms	1)	PRQ-200
Minimum DEN Pulse duration for latch reset	$t_{DEN(LR)}$	50	100	150	µs	3)	PRQ-201
Protection power output stage - 12 mΩ high-side							
Overload detection current at TJ = -40°C, high-side switch	$I_{L(OVL0)\_-40(HS)}$	17	21	25	A	1) T_J = -40°C dI/dt = 0.05 A/µs See ***Figure 15***	PRQ-202

(table continues...)

Table 11 (continued) Electrical characteristics protection

V_S = 6 V to 18 V, T_J = -40°C to +150°C; typical values: V_S= 13.5 V, T_J = 25 °C; typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Overload detection current at TJ= 25°C, high-side switch	$I_{L(OVL0)\_25(HS)}$	17	21	25	A	*1)* T_J = 25°C dI/dt = 0.05 A/µs See ***Figure 15***	PRQ-203
Overload detection current at TJ= 125°C, high-side switch	$I_{L(OVL0)\_125(HS)}$	15	–	–	A	*3)* T_J = 125°C dI/dt = 0.05 A/µs See ***Figure 15***	PRQ-535
Overload detection current at TJ = 150°C, high-side switch	$I_{L(OVL0)\_150(HS)}$	14	16.5	19	A	*3)* T_J = 150°C dI/dt = 0.05 A/µs See ***Figure 15***	PRQ-204
Overload detection current at high VDS, high-side switch	$I_{L(OVL1)(HS)}$	–	15	–	A	*3)* dI/dt= 0.05 A/µs T_J = 25°C See ***Figure 15***	PRQ-205
Overload detection current - jump start condition, high-side switch	$I_{L(OVL\_JS)(HS)}$	–	15	–	A	*3)* $V_S > V_{S(JS)}$ dI/dt = 0.05 A/µs T_J = 25°C See ***Figure 16***	PRQ-206
Protection power output stage - 20 mΩ low-side							
Overload detection current, low-side switch	$I_{L(OVL0)(LS)}$	16	21	28	A	*1)* dI/dt = 0.05 A/µs See ***Figure 15***	PRQ-207

1) Functional test only
2) Tested at T_J = 150°C only
3) Not subject to production test - specified by design

8 Diagnosis

For diagnosis purpose, the BTN7030-1EPA provides a combination of digital and analog signals at pin IS. These signals are generically named SENSE and written I_{IS}. In case of disabled diagnostic, IS pin becomes high impedance.

A sense resistor R_{SENSE} must be connected between IS pin and module ground if the current sense diagnosis is used. A typical value is R_{SENSE} = 1.2 kΩ.

Due to the internal connection between IS pin and V_S supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices, if they are supplied by a different battery feed.

8.1 Overview

Table 12 gives a quick reference for the state of the IS pin during BTN7030-1EPA operation.

Table 12 SENSE signal, function of application condition

Application Condition	Inputs			Outputs			Diagnostic Output (IS)
	EN	IN	DEN	HSS	LSS	OUT (V_{OUT})	
Stand-by operation	0	X	1	OFF	OFF	_ [3]	Z $I_{IS(FAULT)}$ if latch ≠ 0
Open Load				OFF	OFF	< V_S - $V_{DS(OLOFF)}$ > V_S - $V_{DS(OLOFF)}$	Z $I_{IS(OLOFF)}$ $I_{IS(FAULT)}$ if latch ≠ 0
Inverse current on LSS				OFF	ON	~ V_{INV} = V_{OUT} < $V_{INV(LS)}$	Z $I_{IS(FAULT)}$ if latch ≠ 0
Inverse current on HSS				OFF	OFF	~ V_{INV} = V_{OUT} > V_S	$I_{IS(OLOFF)}$ $I_{IS(FAULT)}$ if latch ≠ 0
Normal operation	1	0		OFF	ON	~ GND	Z (= $I_{IS(OFF)}$)
		1		ON	OFF	~ V_S	I_{IS} = I_L / k_{ILIS} (> $I_{IS(EN)}$)
Overcurrent at HS or LS		X		OFF	OFF	[3]	$I_{IS(FAULT)}$
Short circuit to GND		X		OFF	OFF	~ GND	$I_{IS(FAULT)}$
Short circuit to V_S		0		OFF	OFF	~ V_S	$I_{IS(FAULT)}$
		1				~ V_S	Z
						~ GND	$I_{IS(FAULT)}$
Open Load		1		ON	OFF	~ V_S [1]	$I_{IS(EN)}$
Under load at HS (e.g. output voltage limitation condition)		1		ON	OFF	~ V_S [2]	$I_{IS(EN)}$ < I_{IS} < $I_{L(NOM)}$ / k_{ILIS}
Overtemperature at HS or LS		X		OFF	OFF	Z	$I_{IS(FAULT)}$
Inverse current on HSS		1		ON	OFF	V_{OUT} > V_S	$I_{IS(EN)}$
Inverse current on LSS	X	X	X	OFF	ON	~ V_{INV} = V_{OUT} < $V_{INV(LS)}$	–
Undervoltage at V_S	X	X	X	OFF	OFF	_ [3]	Z
Sleep Mode	0	0	0	OFF	OFF	Z	Z
All conditions	X	X	0			_ [3]	Z

Diagnosis

1) The output current has to be lower than $I_{L(OL)}$
2) The output current has to be higher than $I_{L(OL)}$
3) load dependent

Table 13 Signal value explanation

Inputs (EN, IN, DEN)	Switches (LSS, HSS)	Diagnostic Output (IS)
0 = Logic "low"	OFF = switched off	Z = high Impedance
1 = Logic "high"	ON = switched on	
X = "low" or "high"		

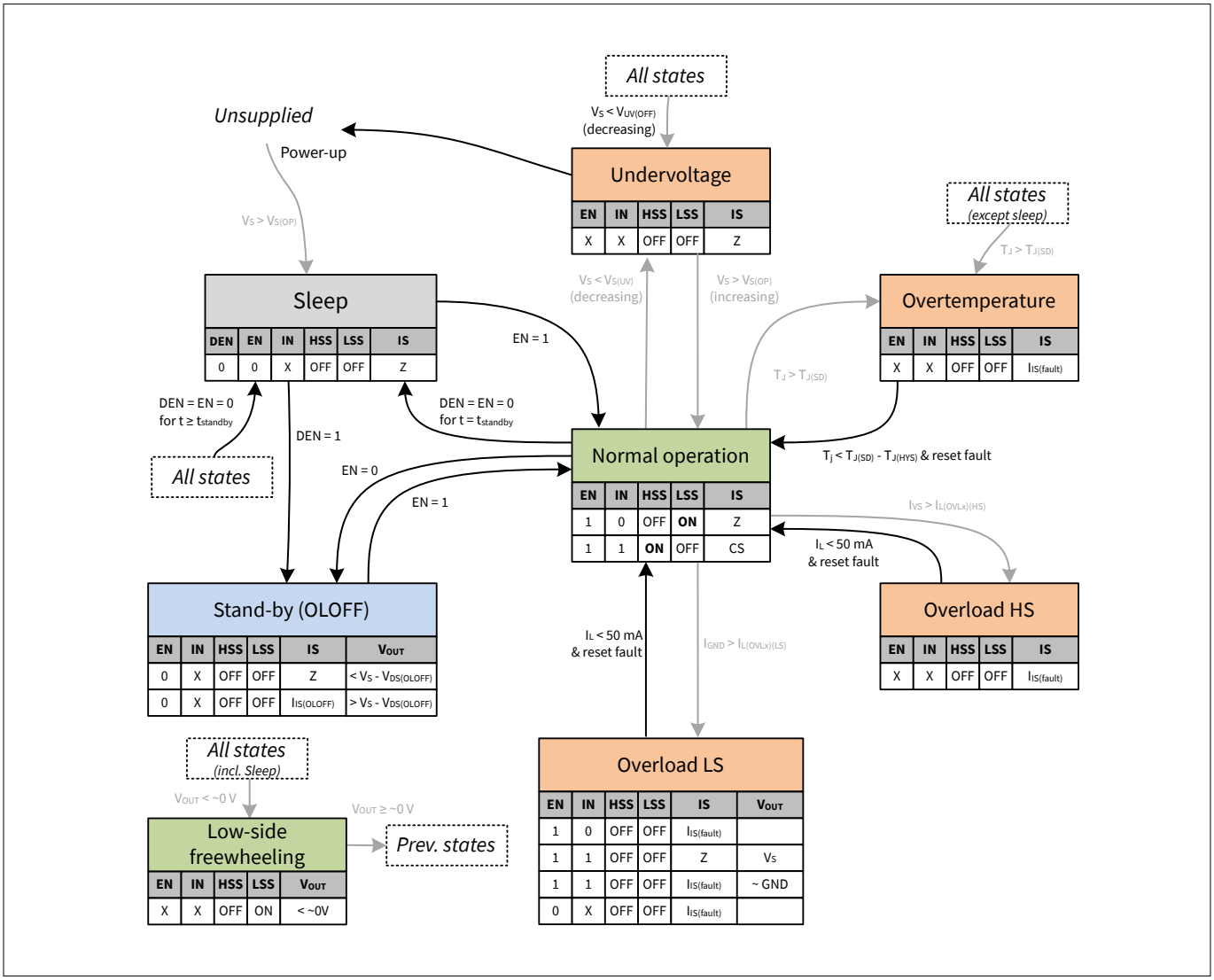


Figure 20 Simplified State Diagram for DEN = "high" (unless otherwise specified)

- Grey arrow: Transition caused by change of environmental conditions.
- Black arrow: Possible transition by digital input pins (EN, DEN or IN pin).

8.2 Diagnosis in ON state

A current proportional to the load current through the high-side output stage (ratio $k_{ILIS} = I_L / I_{IS}$) is provided at pin IS when the following conditions are fulfilled:

- the power output stage is switched ON with V_{DS} < 2 V
- the diagnosis is enabled
- no fault (as described in ***Chapter 7.3***) is present or was present and not cleared yet (see ***Chapter 8.2.2*** for further details)

If a "hard" failure mode is present or was present and not cleared yet a current $I_{IS(FAULT)}$ is provided at IS pin.

8.2.1 Current sense (k_{ILIS})

The accuracy of the sense current depends on temperature and load current. I_{IS} increases linearly with I_L output current through the high-side switch until I_L reaches the overload detection current $I_{L(OVLx)}$. In case of open load at the output stage (I_L close to 0 A), the maximum sense current $I_{IS(EN)}$ (no load, diagnosis enabled) is specified. This condition is shown in ***Figure 21***. The blue line represents the ideal k_{ILIS} line, while the red lines show the behavior of a typical product.

An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce signal ripple and oscillations (a minimum time constant of 1 µs for the RC filter is recommended).

The k_{ILIS} factor is specified with limits that take into account effects due to temperature, supply voltage and manufacturing process. Tighter limits are possible (within a defined current window) with calibration:

• a well-defined and precise current ($I_{L(CAL)}$) is applied at the output during end of line test at customer side

• the corresponding current at IS pin is measured and the k_{ILIS} is calculated (k_{ILIS} @ $I_{L(CAL)}$)

• within the current range going from $I_{L(CAL)\_L}$ to $I_{L(CAL)\_H}$ the k_{ILIS} is equal to k_{ILIS} @ $I_{L(CAL)}$ with limits defined by Δk_{ILIS}

The derating of k_{ILIS} after calibration is calculated using the formulas in ***Current sense Δk_{ILIS} calculation formulas*** and it is specified by Δk_{ILIS}

Current sense Δk_{ILIS} calculation formulas

$$\Delta k_{ILIS,MIN} = 100 * MIN\left(\frac{k_{ILIS}@I_{L(CAL)\_L}}{k_{ILIS}@I_{L(CAL)}} - 1,\quad \frac{k_{ILIS}@I_{L(CAL)H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

Equation 1

$$\Delta k_{ILIS,MAX} = 100 * MAX\left(\frac{k_{ILIS}@I_{L(CAL)\_L}}{k_{ILIS}@I_{L(CAL)}} - 1,\quad \frac{k_{ILIS}@I_{L(CAL)H}}{k_{ILIS}@I_{L(CAL)}} - 1\right)$$

Equation 2

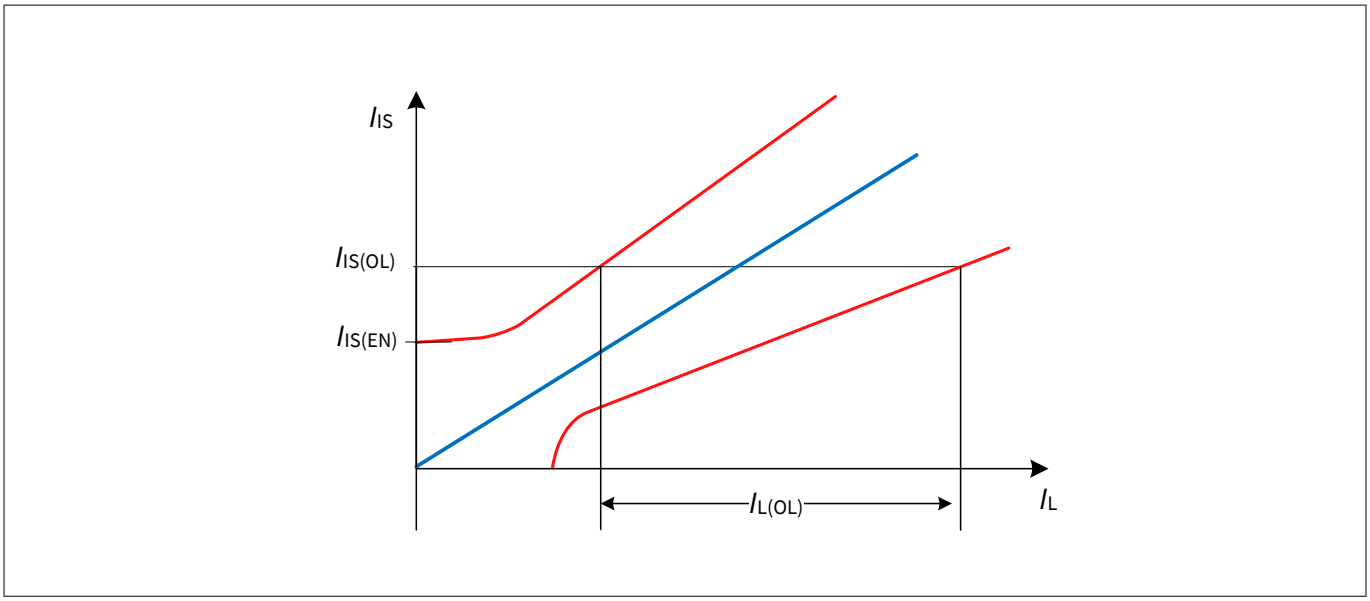


Figure 21 Current sense ratio in open load at ON condition

The calibration is intended to be performed at $T_{A(CAL)}$ = 25°C. The parameter Δk_{ILIS} includes the drift over temperature as well as the drift over the current range from $I_{L(CAL)\_L}$ to $I_{L(CAL)\_H}$.

8.2.2 Fault current ($I_{IS(FAULT)}$)

As soon as a protection event occurs, the value of the internal latch (see ***Chapter 7.3*** for more details) is changed from 0 to 1, a current $I_{IS(FAULT)}$ is provided by pin IS when DEN is set to "high"and both the high-side and low-side output stage of the affected channel are switched OFF.

If the device is switched OFF by protection event and its EN pin is driven by PWM with pulse width < $t_{DELAY(LR)}$, the internal latch could not be reset, the current $I_{IS(FAULT)}$ is provided each time the device diagnosis is activated by DEN.

If the device is OFF and the internal latch is not in the reset state, the current $I_{IS(FAULT)}$ is also provided each time the device diagnosis is checked.

Figure 22 shows the relation between high-side current sense ($I_{IS} = I_L / k_{ILIS}$) and $I_{IS(FAULT)}$.

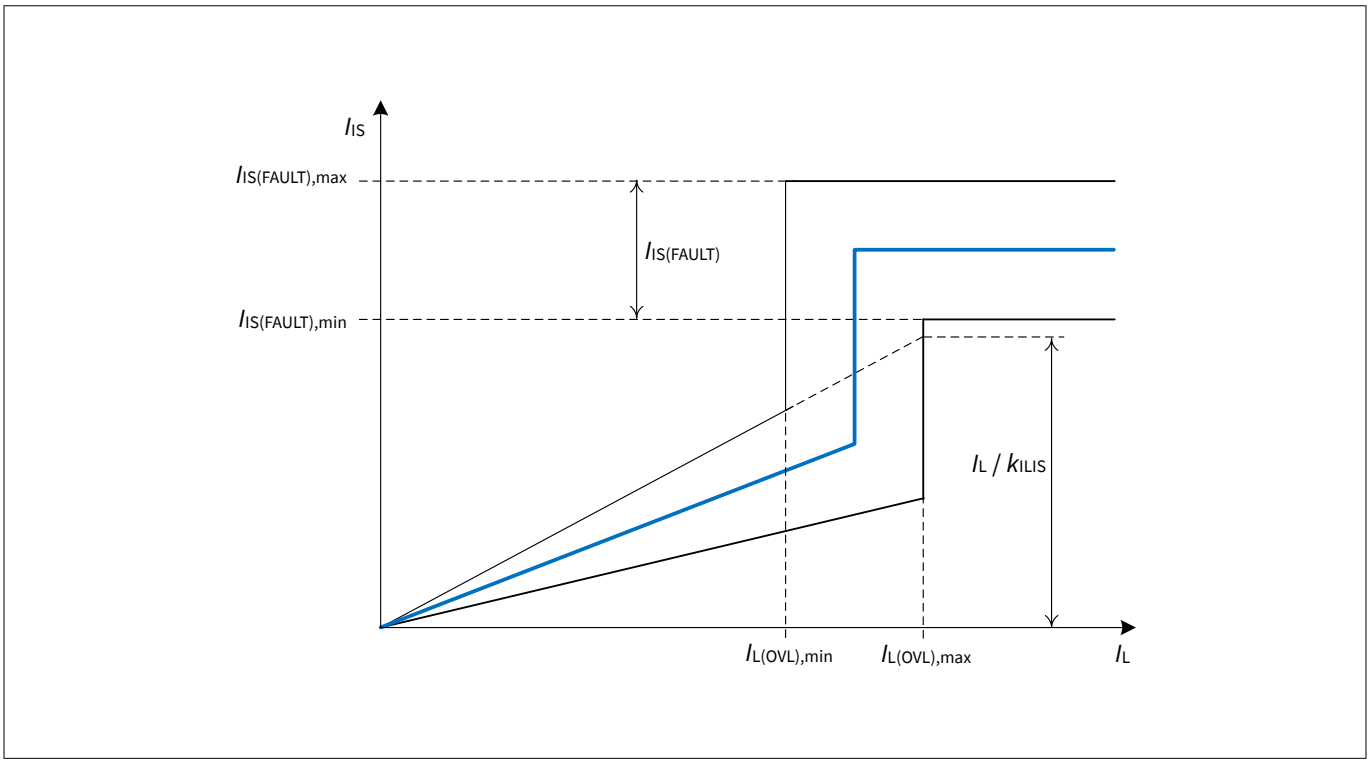


Figure 22 SENSE behavior - overview

If present (EN = IN = DEN = 1, no fault present), the current sense signal can be differentiated from the fault current $I_{IS(FAULT)}$, up to the max. possible load current $I_{L(OVL0)\_-40(HS),max}$.

8.3 Diagnosis in OFF state

When a power output stage is in OFF state, the BTN7030-1EPA can measure the output voltage and compare it with a threshold voltage. In this way, using some additional external components (a pull-down resistor and a switchable pull-up current source) it is possible to detect if the load is missing or if there is a short circuit to battery. If a fault condition was detected by the device (the internal latch has a value different from the reset value, as described in ***Chapter 8.2.2***) a current $I_{IS(FAULT)}$ is provided by IS pin each time the channel diagnosis is checked also in OFF state.

8.3.1 Open load current ($I_{IS(OLOFF)}$)

In OFF state, when DEN pin is set to "high", the V_{DS} voltage of the high-side switch is compared with a threshold voltage $V_{DS(OLOFF)}$. If the load is properly connected and there is no short circuit to battery, $V_{DS(HS)} \sim V_S$ therefore $V_{DS(HS)} > V_{DS(OLOFF)}$. When the diagnosis is active and $V_{DS(HS)} \leq V_{DS(OLOFF)}$, a current $I_{IS(OLOFF)}$ is provided by IS pin. Open Load in OFF detection is only possible for half-bridge configuration where the load is supposed to be connected between the OUT pin of the device and GND. ***Figure 23*** shows the relationship between $I_{IS(OLOFF)}$ and $I_{IS(FAULT)}$ as functions of V_{DS}. The two currents don´t overlap making always possible to differentiate between open load in OFF and fault condition.

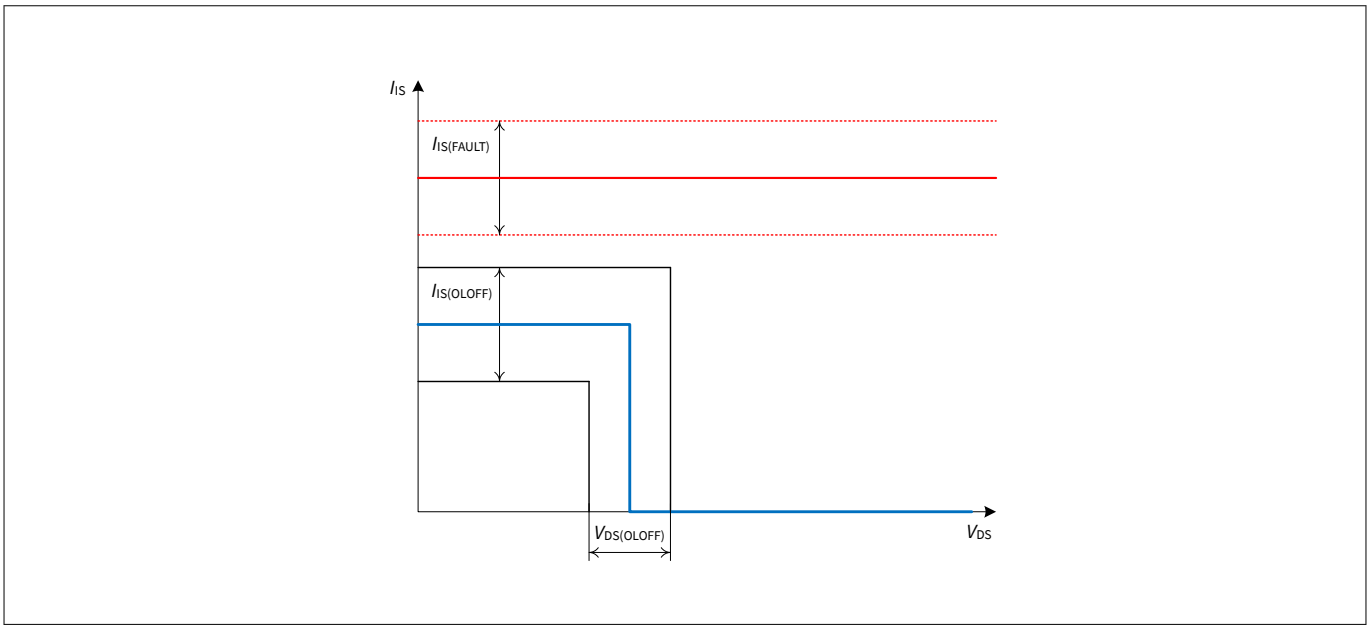


Figure 23 I_{IS} in OFF State

It is necessary to wait a time $t_{IS(OLOFF)\_D}$ between the falling edge of the pin EN and the sensing at pin IS for open load in OFF diagnosis to allow the internal comparator to settle. In ***Figure 24*** the timings for an open load detection are shown - the load is always disconnected.

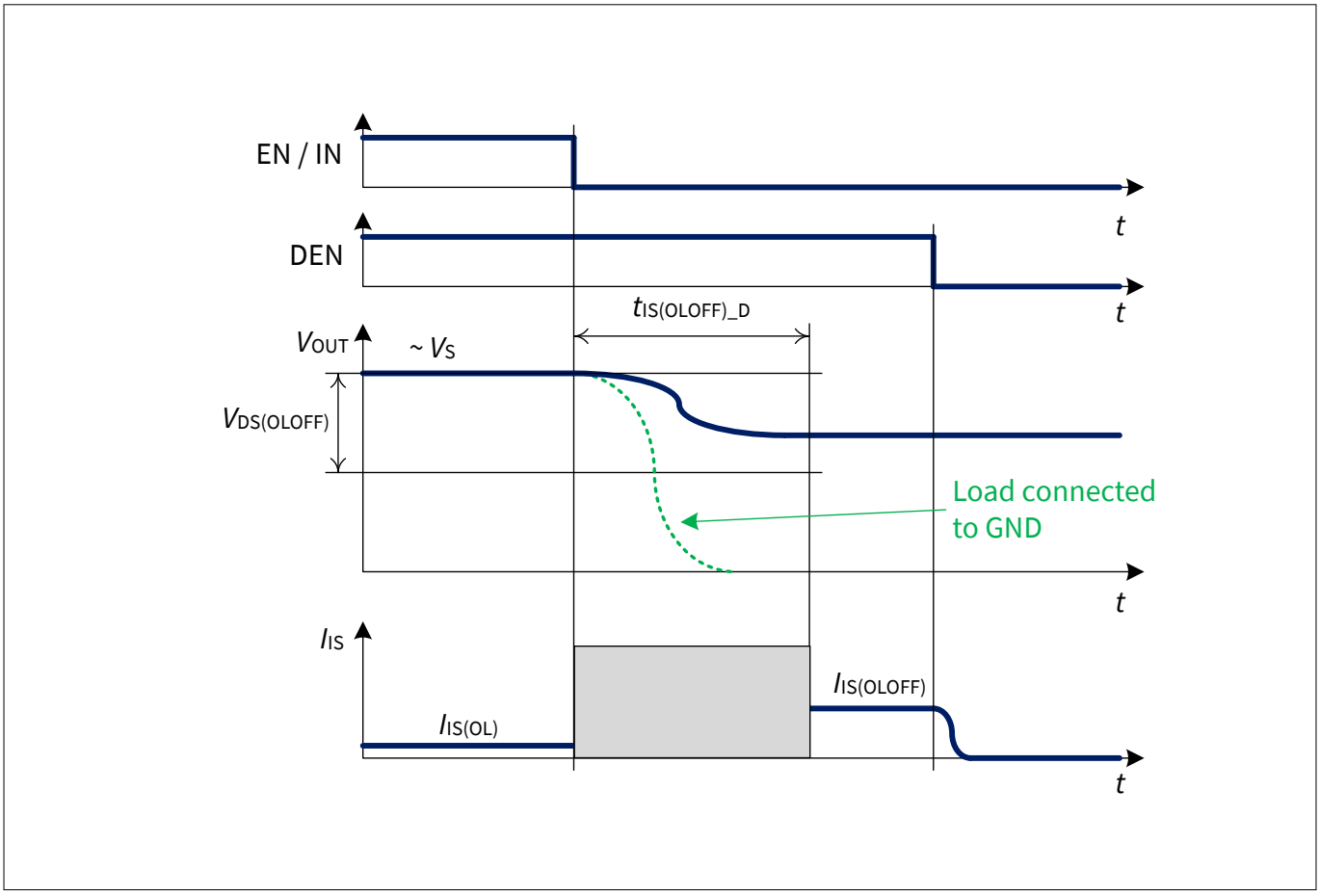


Figure 24 Open load in OFF timings - load disconnected

8.4 SENSE timings

Figure 25 shows the timing during settling $t_{sIS(ON)}$ and disabling $t_{sIS(OFF)}$ of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before t_{ON}):

$t_{sIS(DIAG)} = t_{sIS(ON)} + t_{ON}$

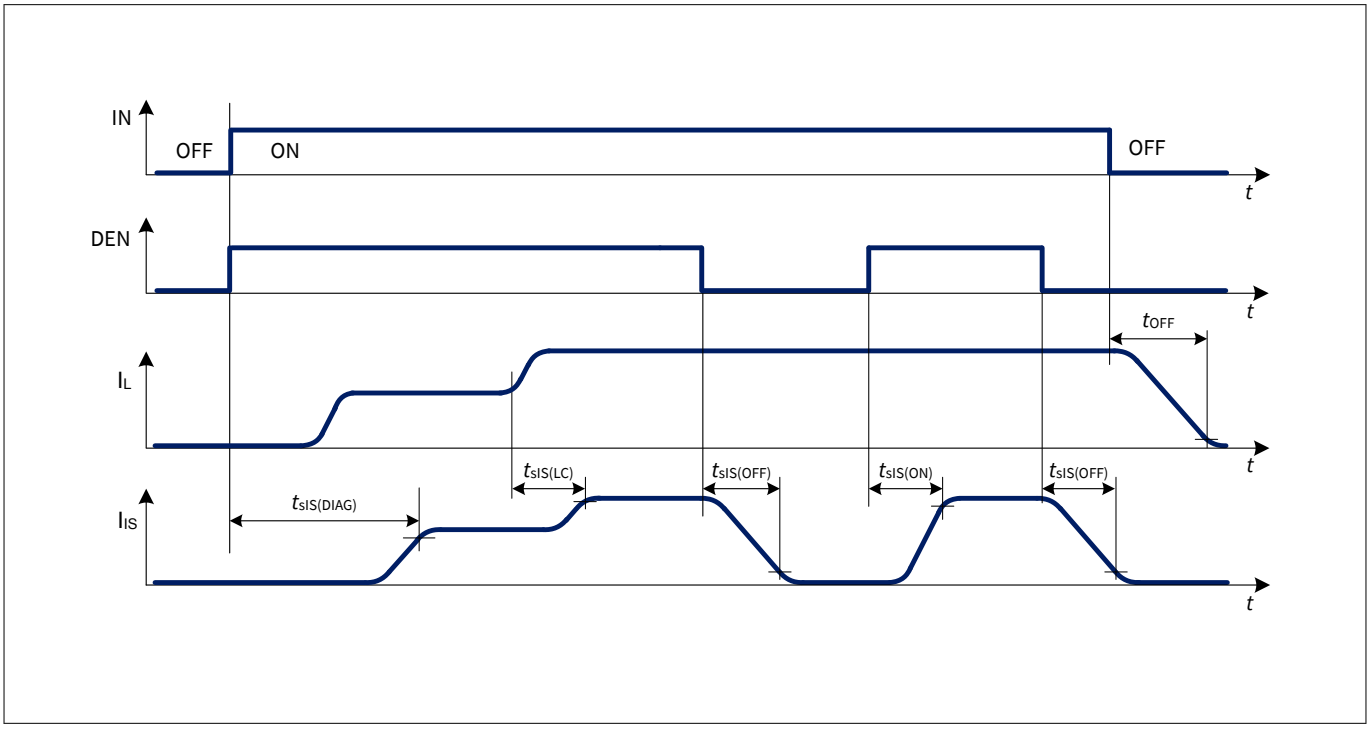


Figure 25 SENSE Settling / disabling timing, with EN = “high” and load to GND

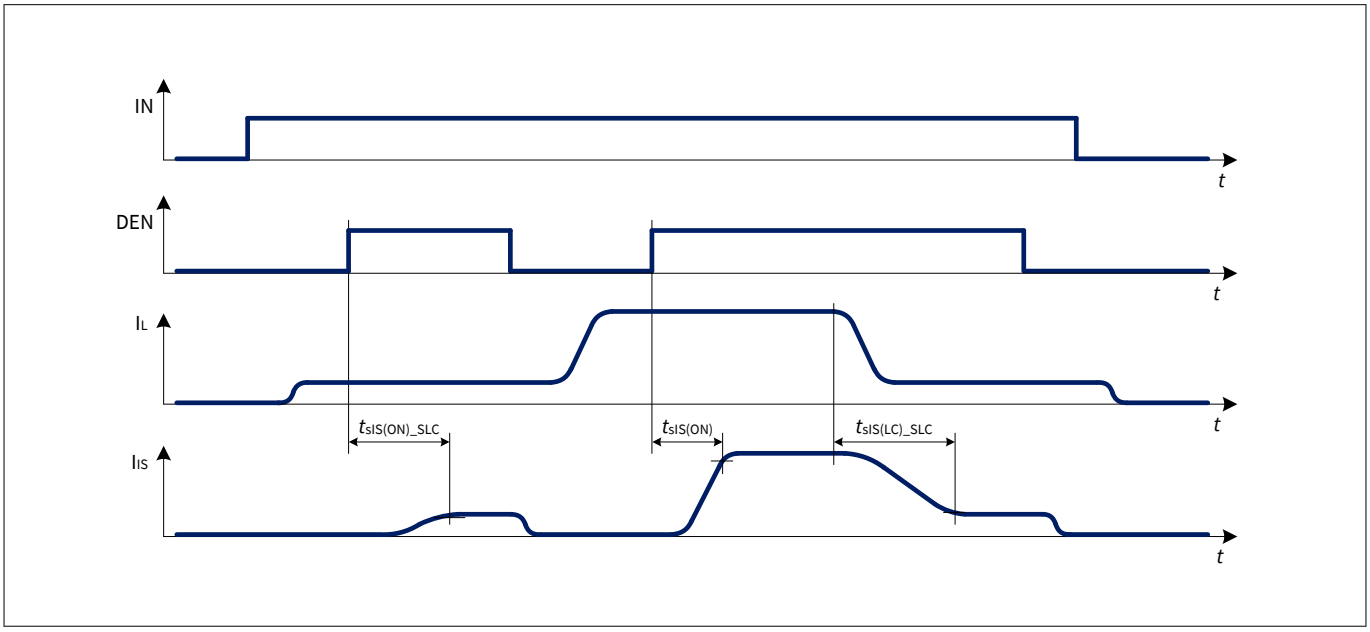


Figure 26 SENSE Timing with Small Load Current, with EN = "high" and load to GND

8.5 Electrical characteristics diagnosis

Table 14 Electrical characteristics diagnosis

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE leakage current when disabled	$I_{IS(OFF)}$	–	0.01	0.5	µA	DEN = "low" $I_L \geq I_{L(NOM)}$ V_{IS} = 0 V	PRQ-209
SENSE leakage current when enabled at TJ ≤ 85 °C	$I_{IS(EN)\_85}$	–	0.2	1	µA	1) $T_J \leq 85°C$ DEN = "high" I_L = 0 A See ***Figure 21***	PRQ-210
SENSE leakage current when enabled at TJ = 150 °C	$I_{IS(EN)\_150}$	–	0.2	1	µA	T_J = 150°C DEN = "high" I_L = 0 A See ***Figure 21***	PRQ-211
SENSE Signal Saturation Voltage for kILIS operation (VS-VIS)	V_{SIS_k}	–	0.5	1	V	1) V_S = 6 V EN = IN =DEN ="high" $I_L \leq 1.5 * I_{L(NOM)}$	PRQ-212
Power supply to IS pin clamping voltage at TJ = -40°C	$V_{IS(CLAMP)\_-40}$	33	36.5	42	V	I_{IS} = 1 mA T_J = -40 °C See ***Figure 19***	PRQ-215
Power supply to IS pin clamping voltage at TJ = 25°C	$V_{IS(CLAMP)\_25}$	35	38	44	V	2) I_{IS} = 1 mA $T_J \geq 25$ °C See ***Figure 19***	PRQ-216
Electrical characteristics diagnosis							
SENSE fault current	$I_{IS(FAULT)}$	4.4	5.5	10	mA	See ***Figure 22*** and ***Figure 23***	PRQ-217
SENSE open load in OFF current	$I_{IS(OLOFF)}$	1.9	2.5	3.5	mA	See ***Figure 22*** and ***Figure 23***	PRQ-218
SENSE open load in OFF delay time	$t_{IS(OLOFF)\_D}$	30	70	120	µs	$V_{DS} < V_{OL(OFF)}$ from EN falling edge to $I_{IS} = I_{S(OLOFF),MIN} * 0.9$ DEN = "high" latch = 0 See ***Figure 24***	PRQ-219
Open load VDS detection threshold in OFF state	$V_{DS(OLOFF)}$	1.3	1.8	2.3	V	See ***Figure 23***	PRQ-221

(table continues...)

Table 14 (continued) Electrical characteristics diagnosis

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
SENSE settling time with nominal load current stable	$t_{sIS(ON)}$	–	5	20	µs	$I_L = I_{L(CAL)}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) * 0.9$ See ***Figure 25***	PRQ-222
SENSE settling time with small load current stable	$t_{sIS(ON)\_SLC}$	–	–	60	µs	*1)* $I_L = I_{L(CAL)\_OL}$ from DEN rising edge to $I_{IS} = I_L / (k_{ILIS,MAX} @ I_L) * 0.9$ See ***Figure 26***	PRQ-223
SENSE disable time	$t_{sIS(OFF)}$	–	5	20	µs	*1)* From DEN falling edge to $I_{IS} = I_{IS(OFF)}$ See ***Figure 25***	PRQ-224
SENSE settling time after load change	$t_{sIS(LC)}$	–	5	20	µs	*1)* From $I_L = I_{L(CAL)\_L}$ to $I_L = I_{L(CAL)}$ (see $\Delta k_{ILIS(NOM)}$) See ***Figure 25***	PRQ-225
SENSE settling time after load change with small load current	$t_{sIS(LC)\_SLC}$	–	250	400	µs	*1)* DEN = "high" from Load Change to $I_{IS} = I_L / (k_{ILIS} @ I_L)$ from $I_{L(CAL)}$ to $I_{L(CAL)\_OL}$ See ***Figure 26***	PRQ-226
Diagnosis power output stage - 15 mΩ high-side							
Open load output current at IIS= 4 µA	$I_{L(OL)\_4u}$	8	21	35	mA	$I_{IS} = I_{IS(OL)}$ = 4 µA See ***Figure 21***	PRQ-227
Current sense ratio at IL=IL02	k_{ILIS02}	-50%	4300	+50%		I_{L02} = 20 mA	PRQ-232
Current sense ratio at IL=IL05	k_{ILIS05}	-42%	4300	+42%		I_{L05} = 100 mA	PRQ-235
Current sense ratio at IL=IL08	k_{ILIS08}	-40%	4300	+40%		I_{L08} = 250 mA	PRQ-238
Current sense ratio at IL=IL11	k_{ILIS11}	-25%	4300	+25%		I_{L11} = 1 A	PRQ-241
Current sense ratio at IL=IL14	k_{ILIS14}	-8%	4300	+8%		I_{L14} = 2.8 A	PRQ-244
Current sense ratio at IL=IL16	k_{ILIS16}	-6%	4300	+6%		I_{L16} = 5.5 A	PRQ-246

(table continues...)

Table 14 (continued) Electrical characteristics diagnosis

V_S = 6 V to 18 V, T_J = -40°C to +150°C; Typical values: V_S = 13.5 V, T_J = 25°C
Typical resistive load connected to the output for testing (unless otherwise specified): R_{load} = 3.3 Ω
all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or condition	P-Number
		Min.	Typ.	Max.			
Current sense ratio at IL=IL18	k_{ILIS18}	-5%	4300	+5%		1) I_{L18} = 10 A	PRQ-248
SENSE Current Derating with Low Current Calibration	$\Delta k_{ILIS(OL)}$	-30	0	+30	%	1) $I_{L(CAL)\_OL} = I_{L05}$ $I_{L(CAL)\_OL\_H} = I_{L08}$ $I_{L(CAL)\_OL\_L} = I_{L02}$ $T_{A(CAL)}$ = 25°C	PRQ-249
SENSE Current Derating with Nominal Current Calibration	$\Delta k_{ILIS(NOM)}$	-4	0	+4	%	1) $I_{L(CAL)} = I_{L16}$ $I_{L(CAL)\_H} = I_{L18}$ $I_{L(CAL)\_L} = I_{L14}$ $T_{A(CAL)}$ = 25°C	PRQ-250

1) Not subject to production test - specified by design
2) Tested at T_J = 150°C

9 Application information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

9.1 Application setup

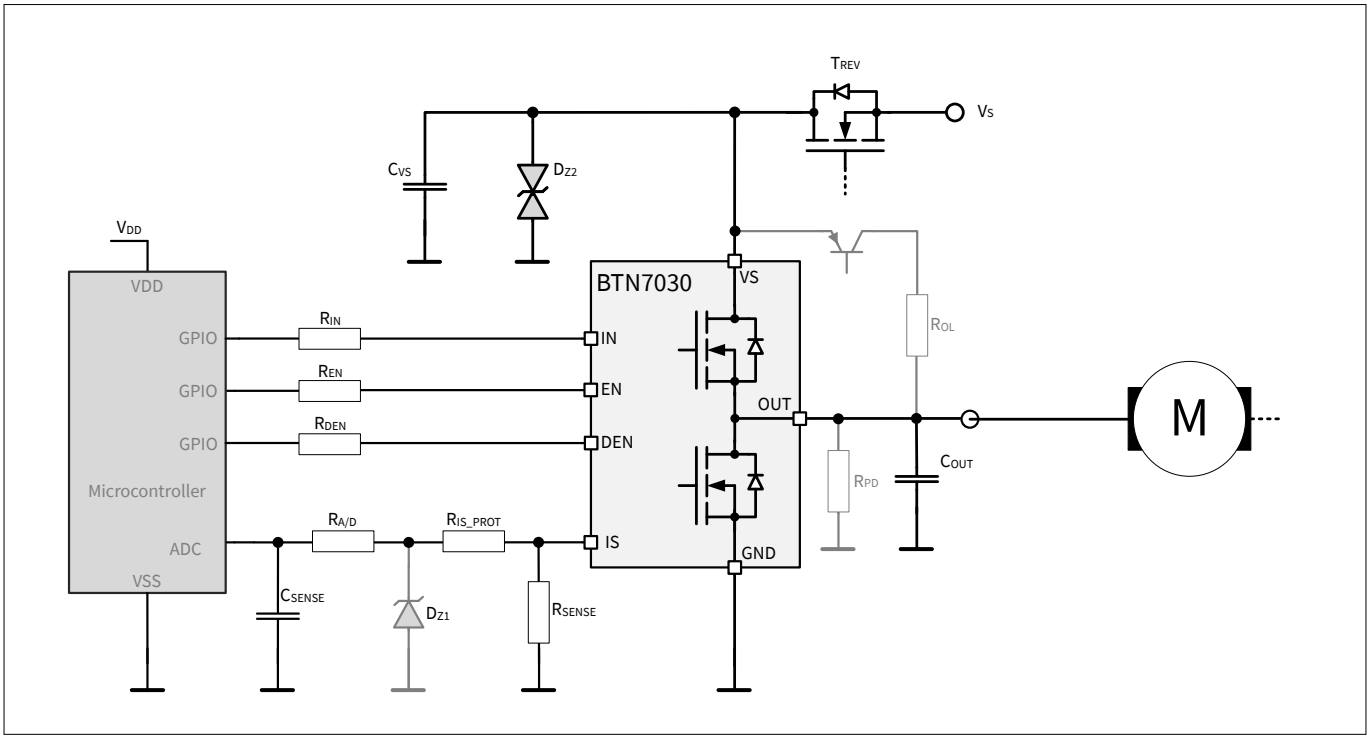


Figure 27 BTN7030-1EPA application diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

9.2 External components

Table 15 Suggested component values

Reference	Value	Purpose
R_{EN} R_{IN} R_{DEN}	4.7 kΩ	Protection of the microcontroller and device during overvoltage and during loss of ground.
R_{PD}	47 kΩ	Output polarization (pull-down, optional) Allows to detect if the OUT pin is shorted to VS.
R_{OL}	1.5 kΩ	Output polarization (pull-up, optional) Ensure polarization of BTN7030-1EPA output during open load in OFF diagnosis.
C_{OUT}	100 nF	Protection of BTN7030-1EPA output during ESD events and BCI.

(table continues...)

Table 15 (continued) Suggested component values

T_1	BC 807	Switch the battery voltage for open load in OFF diagnosis. (optional)
C_{VS}	100 nF	Filtering of voltage spikes on the battery line.
T_{REV}	-	Protection of BTN7030-1EPA during reverse polarity.
D_{Z2}	33 V Z-Diode	Suppressor diode Protection during overvoltage and in case of loss of battery while driving an inductive load.
R_{SENSE}	1.2 kΩ	SENSE resistor
R_{IS_PROT}	4.7 kΩ	Protection during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications, together with $R_{A/D}$.
D_{Z1}	7 V Z-Diode	Protection of the microcontroller during overvoltage. (Optional, depending on the microcontroller's specification)
$R_{A/D}$	4.7 kΩ	Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications, together with R_{IS_PROT}.
C_{SENSE}	220 pF	Sense signal filtering A time constant ($R_{A/D} \cdot C_{SENSE}$) longer than 1 µs is recommended.

The stray inductances have to be minimized in the power bridge design as it is necessary in all switched high power bridges. Therefore it is recommended to ensure that the offset between the BTN7030-1EPA's ground (GND pin) and the microcontroller's (signal) ground is minimized.

It is recommended to do the freewheeling in the high-side path until the load current is 0, to avoid reverse currents through the low-side power stage, thus minimizing power dissipation and avoid an unnecessary stress of the device.

If used in full bridge configuration, it is strongly recommended to change the direction of a motor not before the motor fully stopped thus motor current is 0 A, in order to avoid overvoltage at OUT due to back EMF, e.g. in load dump situations.

If the load also can provide power to the device, e.g. a motor or inductance in generator mode, it is recommended not to use only a diode for reverse polarity but to allow a current flow back to the supply V_{bat}, to prevent the device from overvoltage situations. In such a scenario, the capacitor C_{VS} between VS and GND pin has to be dimensioned accordingly.

Note: The suggested component values above are determined for typical applications. Based on the application circuit and the used components connected to BTN7030-1EPA, it could be necessary to adjust the values above to stay below the maximum ratings for all components. (e.g. reverse battery, transients on battery, ...)

9.3 Bidirectional loads and open load in OFF detection

A bidirectional load, like a motor or a solenoid, can be driven with two BTN7030-1EPA half-bridge in H-bridge configuration, as shown in ***Figure 28***.

In order to perform an open load in OFF detection, the high-side output stage of one half-bridge has to be switched on with IN = EN = "high" (right BTN7030-1EPA in ***Figure 28***). As described in ***Chapter 8.3.1***, and in combination with a pull-up resistor R_{PU} (or alternatively a pull-down resistor R_{PD}) the other half-bridge can check for open load condition.

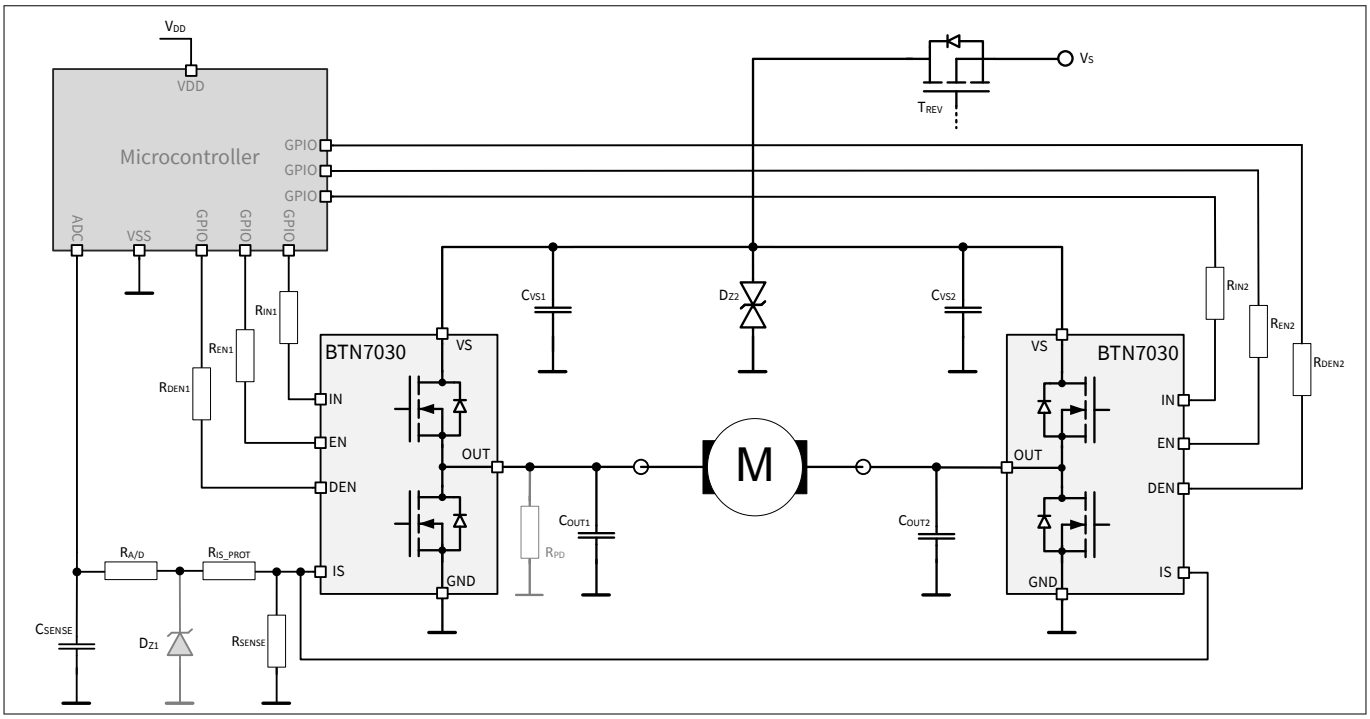


Figure 28 Application circuit: H-bridge with two BTN7030-1EPA

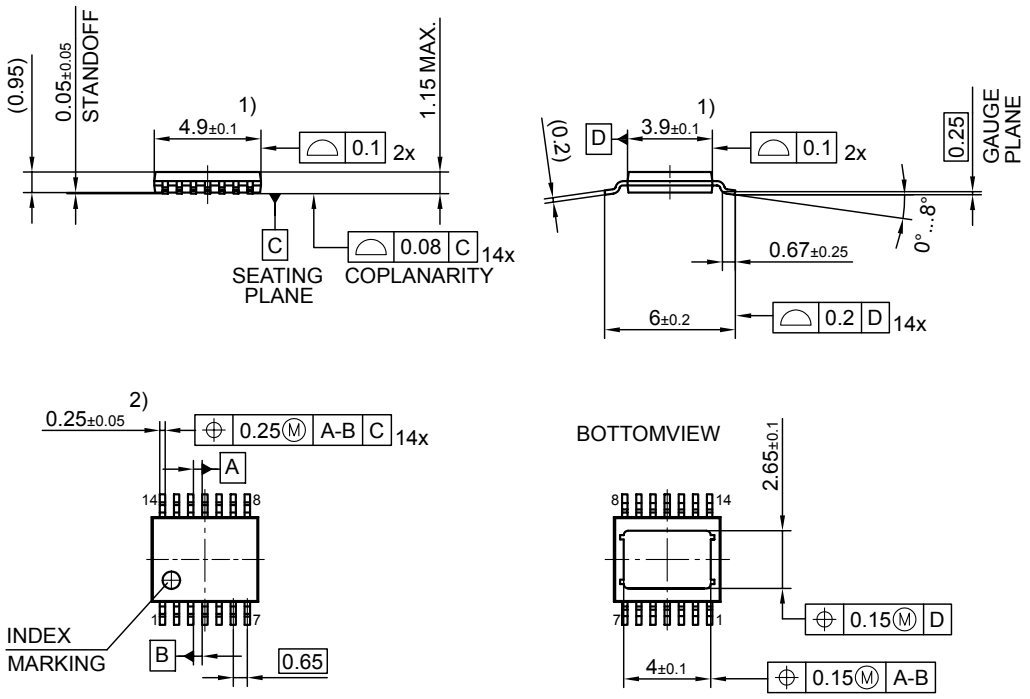
Note

This is a very simplified example of an application circuit. The function must be verified in the real application.

9.4 Further application information

- Please contact us for information regarding the Pin FMEA
- For further information you may contact **http://www.infineon.com/**

10 Package dimensions



1)DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OF 0.15 MAX. PER SIDE
2)DAMBAR PROTUSION SHALL BE MAXIMUM 0.1 MM TOTAL IN EXCESS OF LEAD WIDTH
ALL DIMENSIONS ARE IN UNITS MM
THE DRAWINGIS IN COMPLIANCE WITH ISO 128 & PROJECTION METHOD 1 [ ]

Figure 29 PG-TSDSO-14 (thin (slim) dual small outline 14 pins) package outline

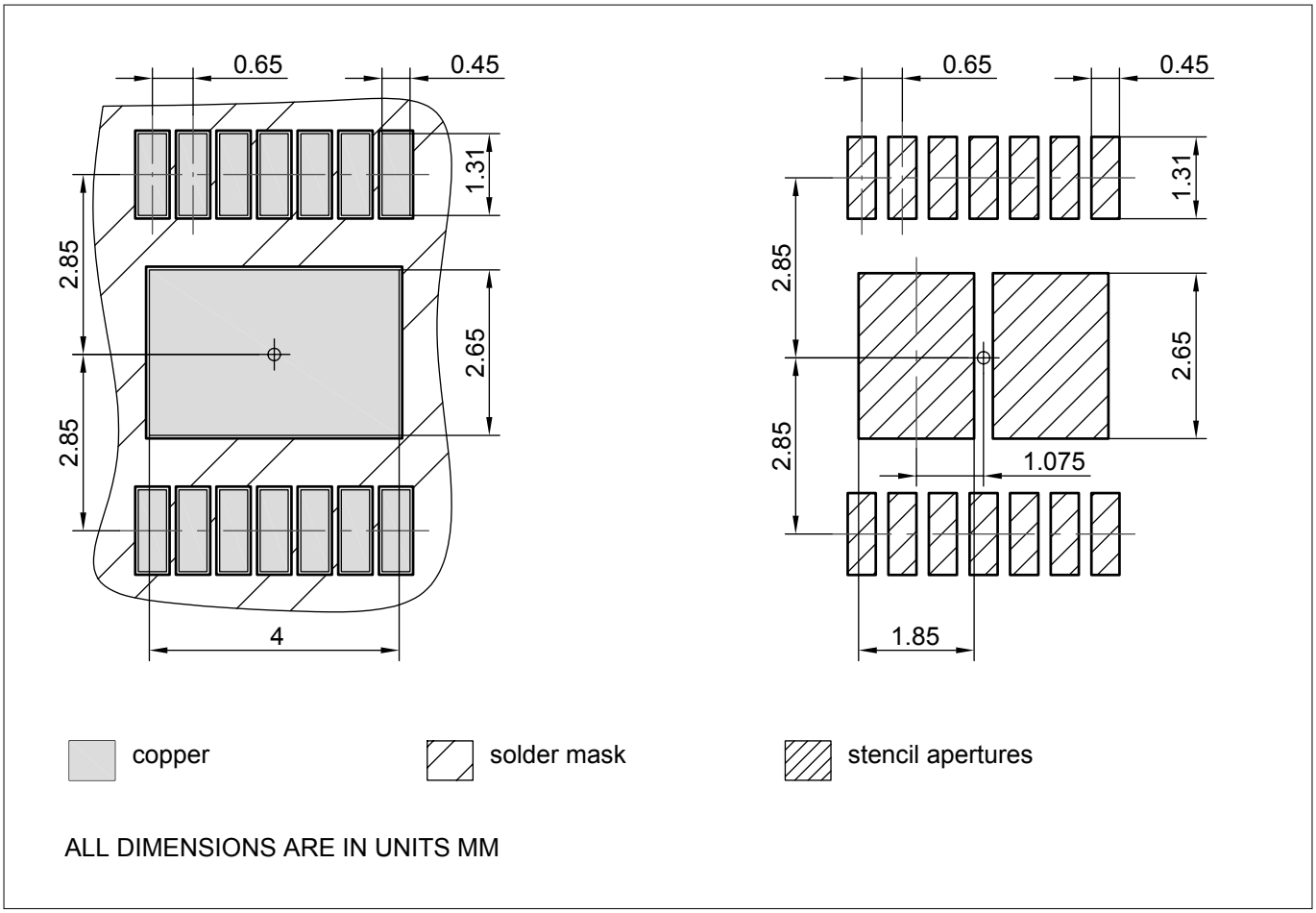


Figure 30 PG-TSDSO-14 (thin (slim) dual small outline 14 pins) package pads and stencil

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

11 References

Revision history

Table 16 Revision history

Document version	Date of release	Description of changes
1.0	2020-08-11	Initial release
1.1	2020-11-20	Chapter Open load current ($I_{IS(OLOFF)}$): refined formulation for usage Chapter External components: refine explanation to *R*PD
1.2	2021-06-24	Block diagram updated Footnote links in table SENSE signal, function of application condition added

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