PD - 90437D

International
IOR Rectifier

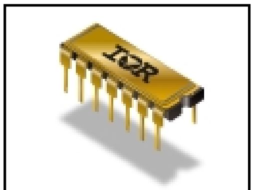
IRFG5110

POWER MOSFET
THRU-HOLE (MO-036AB)

100V, Combination 2N-2P-CHANNEL
HEXFET® MOSFET TECHNOLOGY

Product Summary

Part Number	$R_{DS(on)}$	I_D	CHANNEL
IRFG5110	0.7Ω	1.0A	N
IRFG5110	0.7Ω	-1.0A	P


MO-036AB

HEXFET® MOSFET technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance. HEXFET transistors also feature all of the well-established advantages of MOSFETs, such as voltage control, very fast switching, ease of paralleling and electrical parameter temperature stability. They are well-suited for applications such as switching power supplies, motor controls, inverters, choppers, audio amplifiers, high energy pulse circuits, and virtually any application where high reliability is required. The HEXFET transistor's totally isolated package eliminates the need for additional isolating material between the device and the heatsink. This improves thermal efficiency and reduces drain capacitance.

Features:

- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Dynamic dv/dt Rating
- Light-weight

Absolute Maximum Ratings (Per Die)

	Parameter	N-Channel	P-Channel	Units
I_D @ V_{GS} =± 10V, T_C = 25°C	Continuous Drain Current	1.0	-1.0	A
I_D @ V_{GS} =± 10V, T_C = 100°C	Continuous Drain Current	0.6	-0.6	
I_{DM}	Pulsed Drain Current ①	4.0	-4.0	
P_D @ T_C = 25°C	Max. Power Dissipation	1.4	1.4	W
	Linear Derating Factor	0.011	0.011	W/°C
V_{GS}	Gate-to-Source Voltage	±20	±20	V
E_{AS}	Single Pulse Avalanche Energy	75 ②	75 ⑤	mJ
I_{AR}	Avalanche Current ①	—	—	A
E_{AR}	Repetitive Avalanche Energy ①	—	—	mJ
dv/dt	Peak Diode Recovery dv/dt	5.5 ③	-5.5 ⑥	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150		°C
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)		
	Weight	1.3 (Typical)		g

For footnotes refer to the last page

04/16/02

Electrical Characteristics For Each N-Channel Device @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.13	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.7	Ω	V_{GS} = 10V, I_D = 0.6A ④
		—	—	0.8		V_{GS} = 10V, I_D = 1.0A
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250μA
g_{fs}	Forward Transconductance	0.86	—	—	S (℧)	V_{DS} > 15V, I_{DS} = 0.6A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	V_{DS}= 80V, V_{GS}= 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	15	nC	V_{GS} =10V, I_D = 1.0A, V_{DS} = 50V
Q_{gs}	Gate-to-Source Charge	—	—	7.5		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	7.5		
$t_{d(on)}$	Turn-On Delay Time	—	—	20	ns	V_{DD} = 50V, I_D = 1.0A, V_{GS} =10V, R_G = 24Ω
t_r	Rise Time	—	—	25		
$t_{d(off)}$	Turn-Off Delay Time	—	—	40		
t_f	Fall Time	—	—	40		
$L_S + L_D$	Total Inductance	—	10	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	180	—	pF	V_{GS} = 0V, V_{DS} = 25V f = 1.0MHz
C_{oss}	Output Capacitance	—	82	—		
C_{rss}	Reverse Transfer Capacitance	—	15	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	1.0	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	4.0		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_j = 25°C, I_S = 1.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	200	nS	T_j = 25°C, I_F = 1.0A, di/dt ≤ 100A/μs
Q_{RR}	Reverse Recovery Charge	—	—	0.83	nC	V_{DD} ≤ 50V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	17	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	90		Typical socket mount

Note: Corresponding Spice and Saber models are available on the G&S Website.

For footnotes refer to the last page

Electrical Characteristics For Each P-Channel Device @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-100	—	—	V	V_{GS} = 0V, I_D = -1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	-0.22	—	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.7	Ω	V_{GS} = -10V, I_D = -0.6A ④
		—	—	0.8		V_{GS} = -10V, I_D =- 1.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	—	-4.0	V	V_{DS} = V_{GS}, I_D = -250µA
g_{fs}	Forward Transconductance	1.1	—	—	S (℧)	V_{DS} > -15V, I_{DS} = -0.6A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	-25	µA	V_{DS}= -80V, V_{GS}= 0V
		—	—	-250		V_{DS} = -80V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	-100	nA	V_{GS} = - 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	100		V_{GS} = 20V
Q_g	Total Gate Charge	—	—	22	nC	V_{GS} = -10V, I_D = -1.0A, V_{DS} = -50V
Q_{gs}	Gate-to-Source Charge	—	—	8.0		
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	14		
$t_{d(on)}$	Turn-On Delay Time	—	—	30	ns	V_{DD} = -50V, I_D = -1.0A, V_{GS} = -10V, R_G = 24Ω
t_r	Rise Time	—	—	60		
$t_{d(off)}$	Turn-Off Delay Time	—	—	60		
t_f	Fall Time	—	—	60		
$L_S + L_D$	Total Inductance	—	10	—	nH	Measured from drain lead (6mm/ 0.25in. from package) to source lead (6mm/0.25in. from package)
C_{iss}	Input Capacitance	—	390	—	pF	V_{GS} = 0V, V_{DS} = -25V f = 1.0MHz
C_{oss}	Output Capacitance	—	170	—		
C_{rss}	Reverse Transfer Capacitance	—	45	—		

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	-1.0	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	-4.0		
V_{SD}	Diode Forward Voltage	—	—	-5.5	V	T_j = 25°C, I_S = -1.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	200	nS	T_j = 25°C, I_F = -1.0A, di/dt ≤ -100A/µs V_{DD} ≤ -50V
Q_{RR}	Reverse Recovery Charge	—	—	0.66	nC	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	17	°C/W	
R_{thJA}	Junction-to-Ambient	—	—	90		Typical socket mount

For footnotes refer to the last page

N-Channel
Q1,Q3

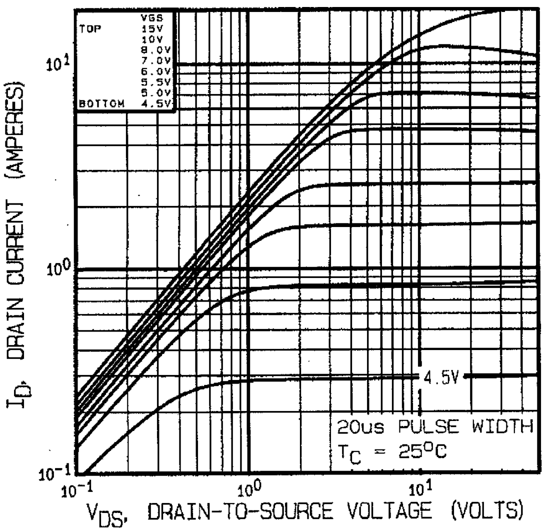


Fig 1. Typical Output Characteristics

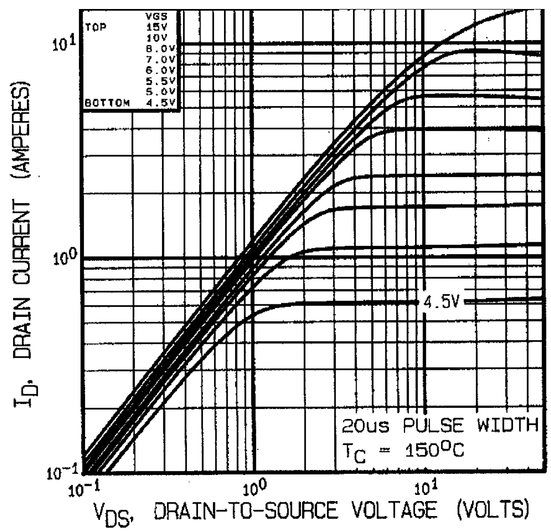


Fig 2. Typical Output Characteristics

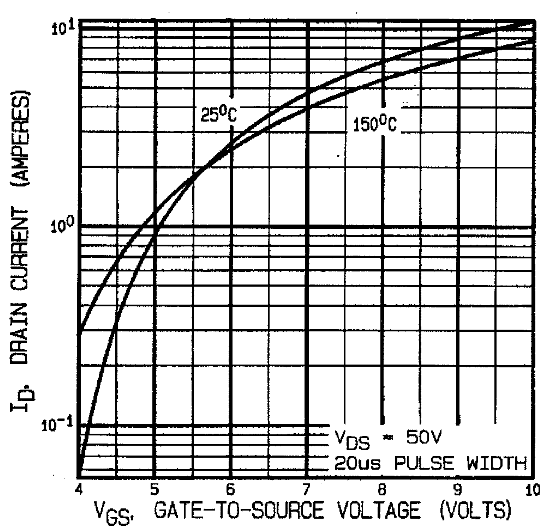


Fig 3. Typical Transfer Characteristics

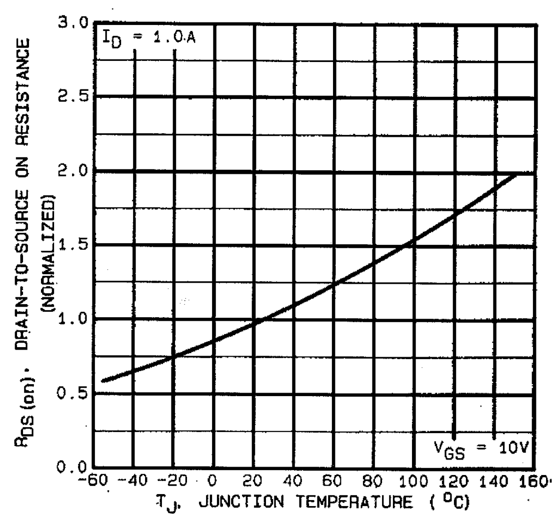


Fig 4. Normalized On-Resistance Vs. Temperature

N-Channel
Q1,Q3

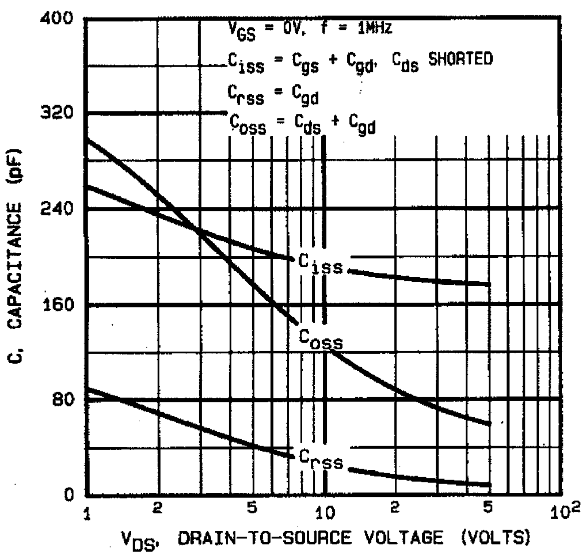


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

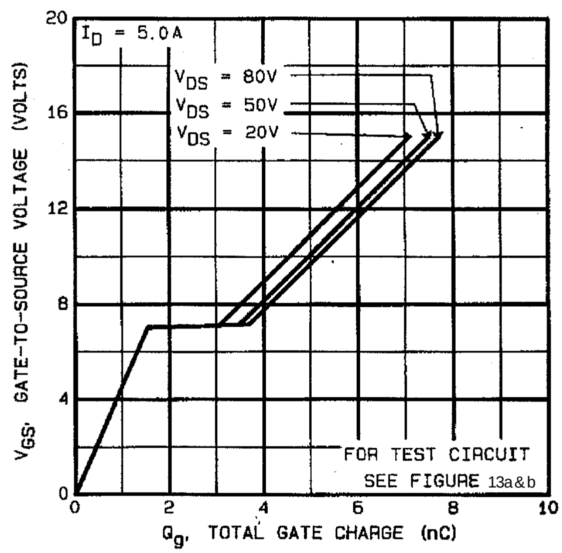


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

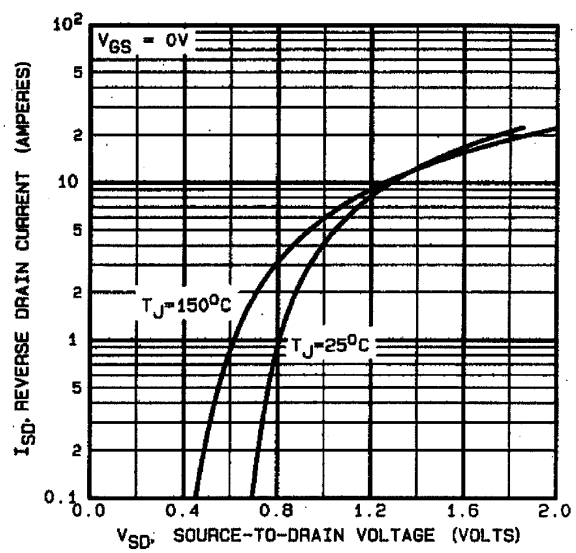


Fig 7. Typical Source-Drain Diode Forward Voltage

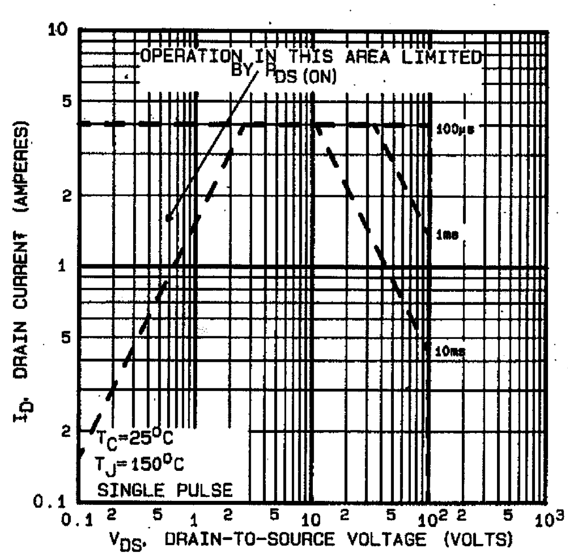


Fig 8. Maximum Safe Operating Area

N-Channel
Q1,Q3

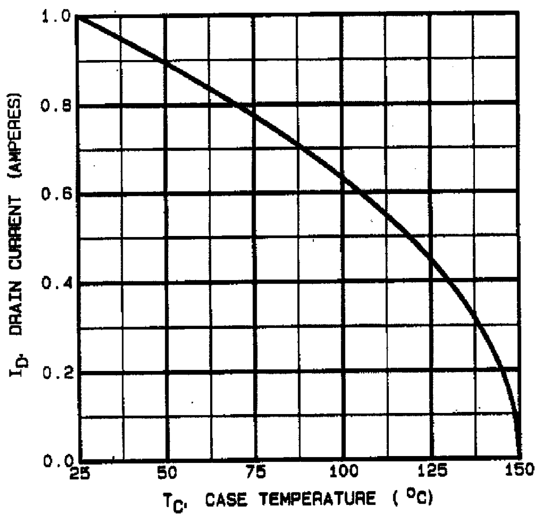


Fig 9. Maximum Drain Current Vs. Case Temperature

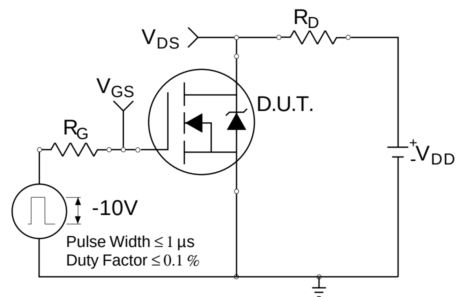


Fig 10a. Switching Time Test Circuit

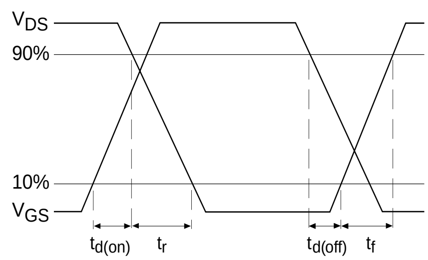


Fig 10b. Switching Time Waveforms

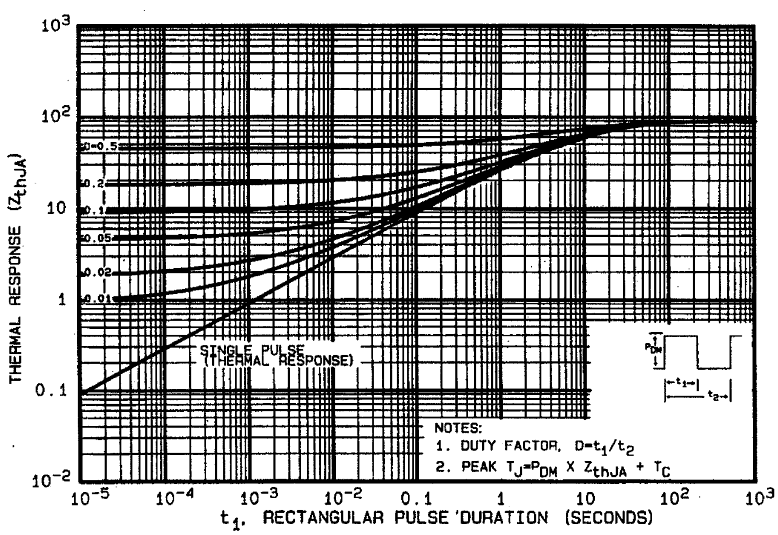


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

N-Channel
Q1,Q3

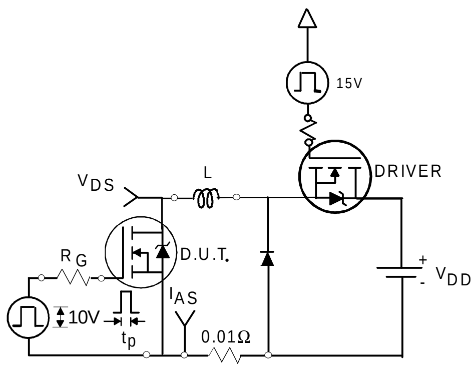


Fig 12a. Unclamped Inductive Test Circuit

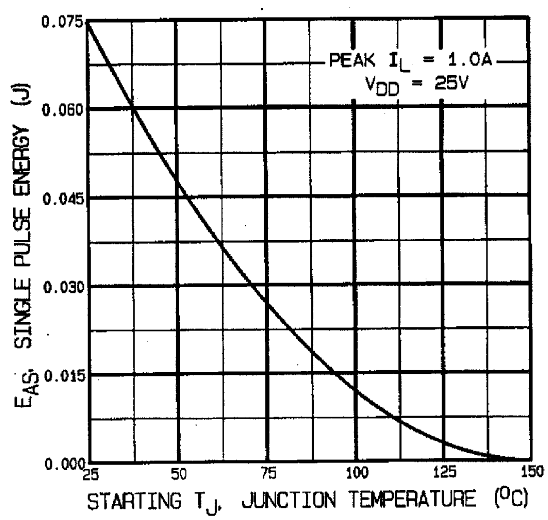


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

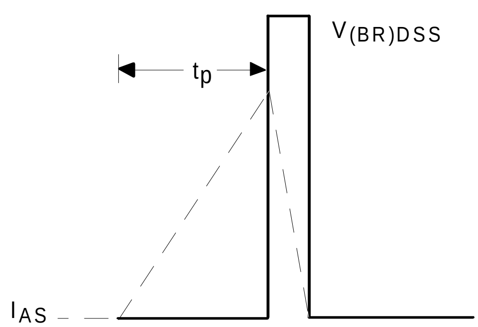


Fig 12b. Unclamped Inductive Waveforms

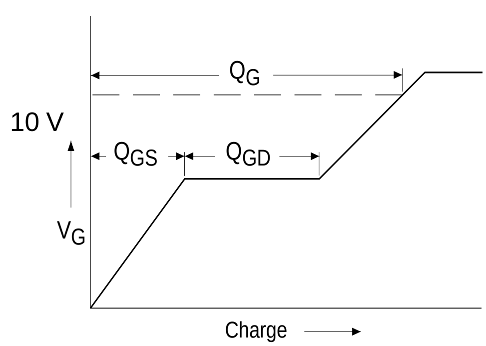


Fig 13a. Basic Gate Charge Waveform

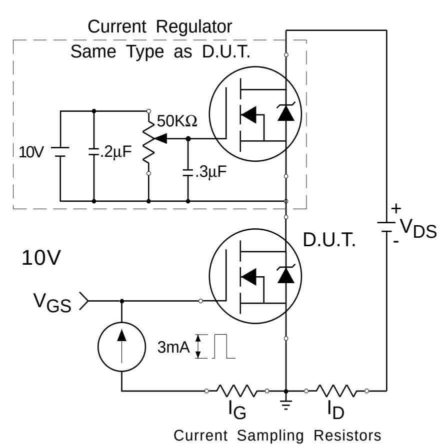


Fig 13b. Gate Charge Test Circuit

P-Channel
Q2,Q4

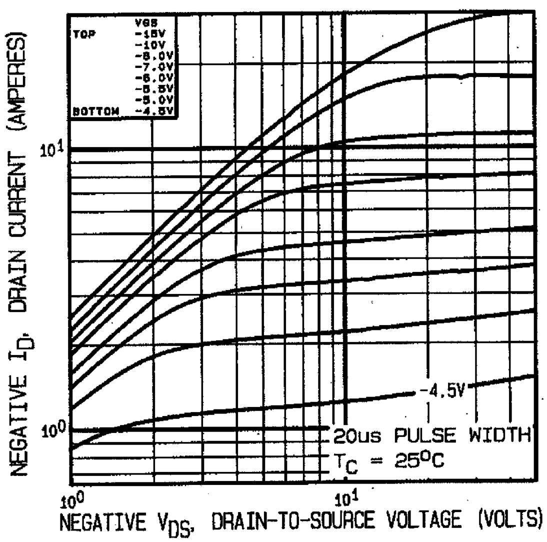


Fig 14. Typical Output Characteristics

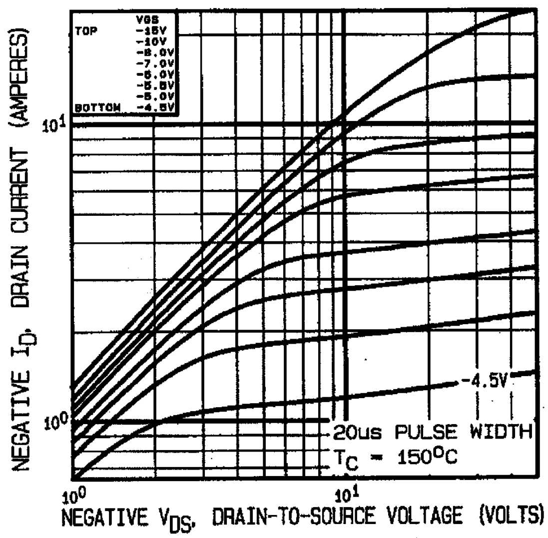


Fig 15. Typical Output Characteristics

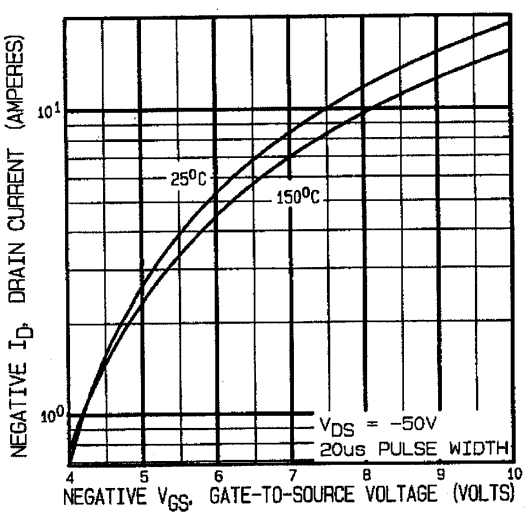


Fig 16. Typical Transfer Characteristics

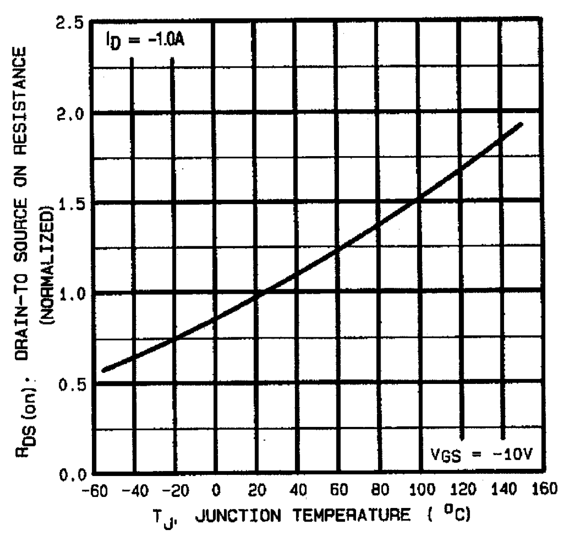


Fig 17. Normalized On-Resistance Vs. Temperature

P-Channel
Q2,Q4

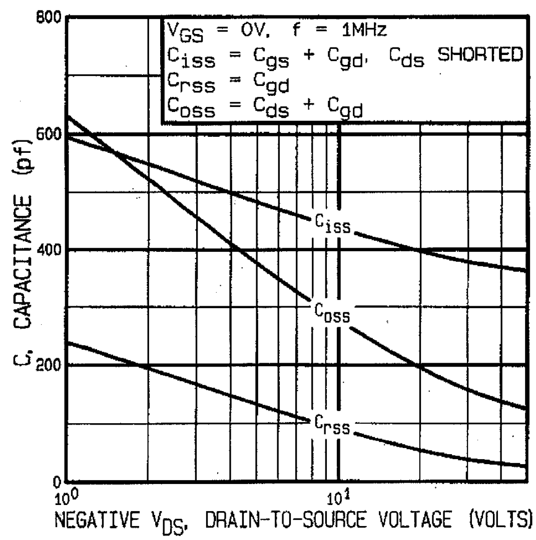


Fig 18. Typical Capacitance Vs. Drain-to-Source Voltage

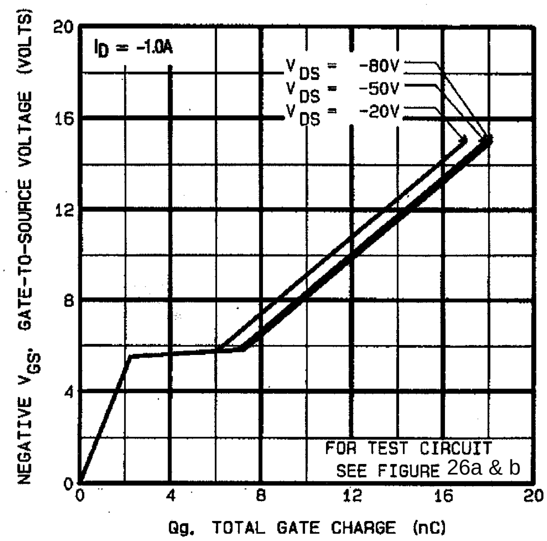


Fig 19. Typical Gate Charge Vs. Gate-to-Source Voltage

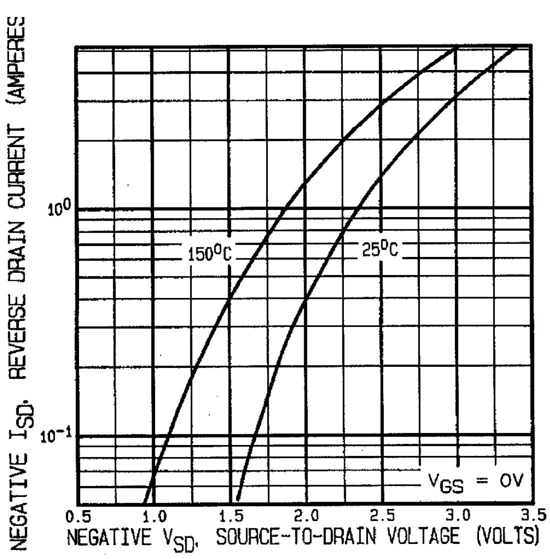


Fig20. Typical Source-Drain Diode Forward Voltage

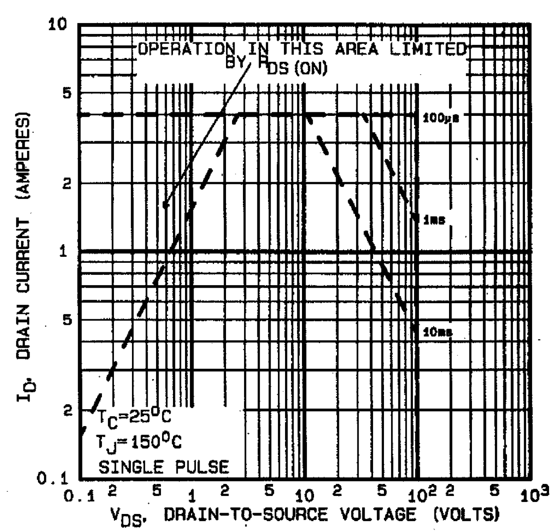


Fig 21. Maximum Safe Operating Area

P-Channel
Q2,Q4

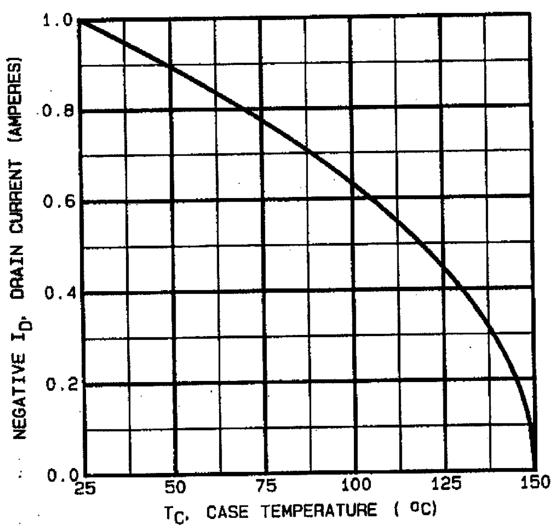


Fig 22. Maximum Drain Current Vs. Case Temperature

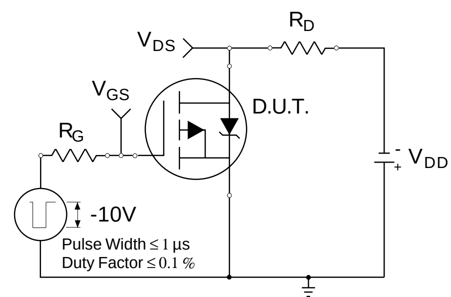


Fig 23a. Switching Time Test Circuit

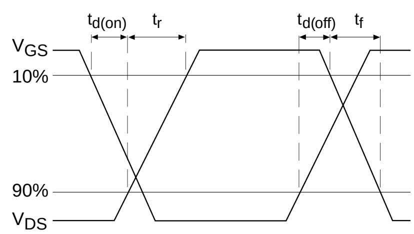


Fig 23b. Switching Time Waveforms

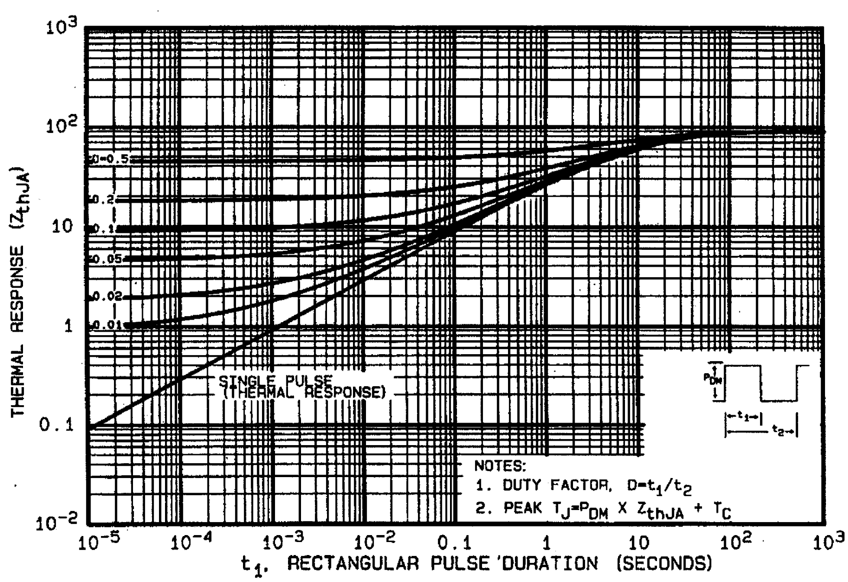


Fig 24. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

P-Channel
Q2,Q4

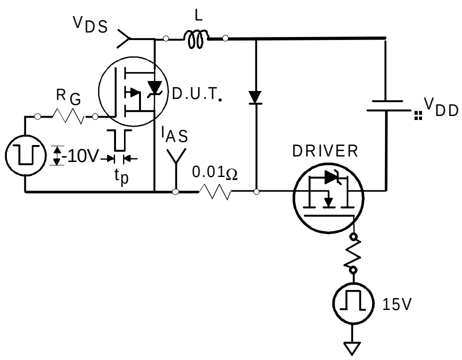


Fig 25a. Unclamped Inductive Test Circuit

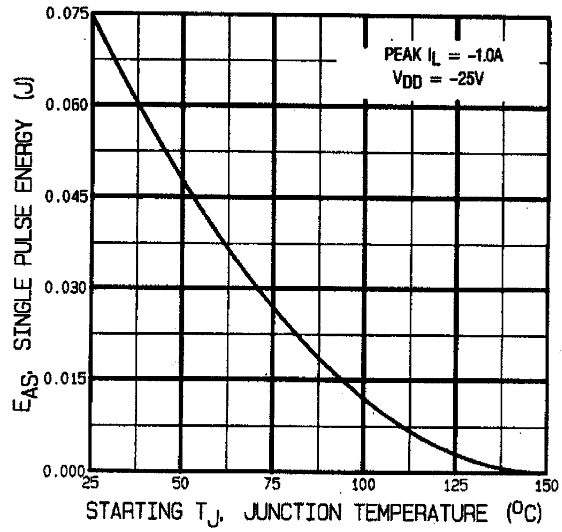


Fig 25c. Maximum Avalanche Energy Vs. Drain Current

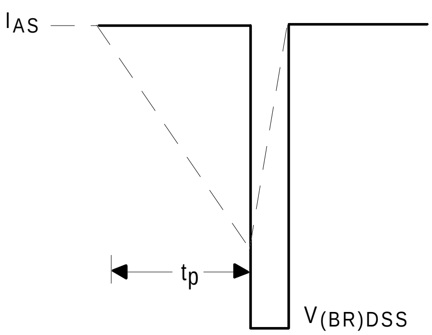


Fig 25b. Unclamped Inductive Waveforms

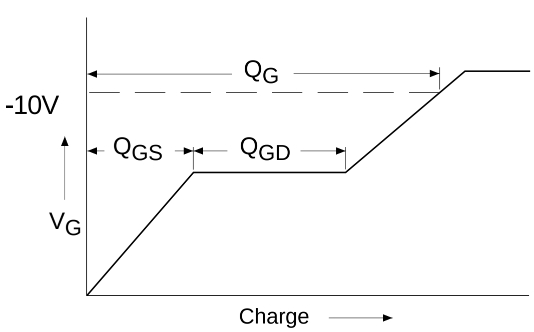


Fig 26a. Basic Gate Charge Waveform

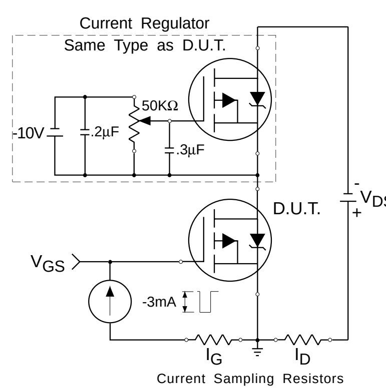


Fig 26b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L= 150mH, Peak I_L = 1.0A, V_{GS} = 10V

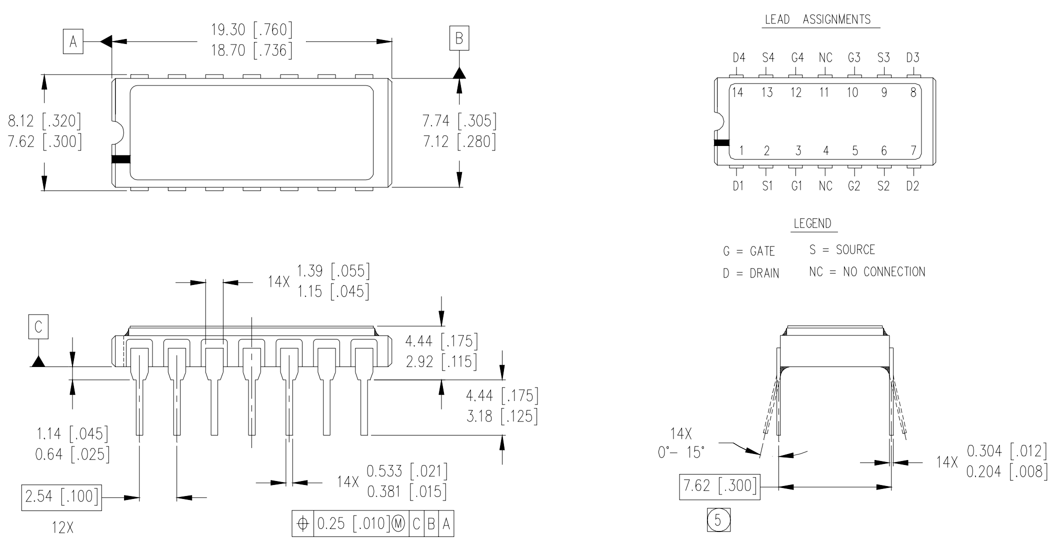
③ $I_{SD} \leq$ 1.0A, di/dt ≤ 75A/µs, $V_{DD} \leq$ 100V, $T_J \leq$ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ V_{DD} = - 25V, starting T_J = 25°C, L= 150mH, Peak I_L = - 1.0A, V_{GS} = -10V

⑥ $I_{SD} \leq$ - 1.0A, di/dt ≤ - 110A/µs, $V_{DD} \leq$ -100V, $T_J \leq$ 150°C

Case Outline and Dimensions — MO-036AB



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
5. MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International
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Data and specifications subject to change without notice.04/02

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon Technologies(英飞凌)]