

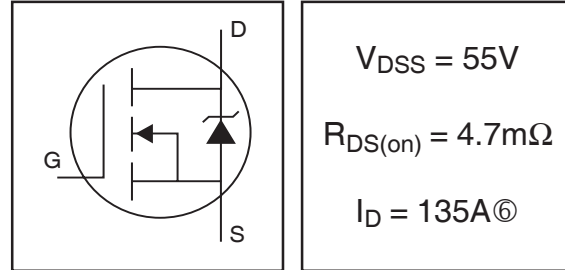
**Typical Applications**

- Industrial Motor Drive

HEXFET® Power MOSFET

**Features**

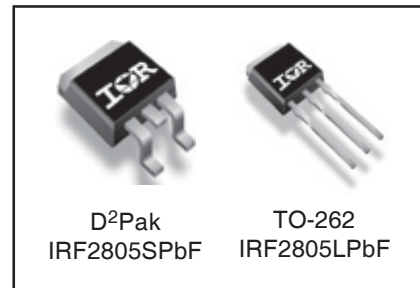
- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free



$V_{DS} = 55V$   
 $R_{DS(on)} = 4.7m\Omega$   
 $I_D = 135A\text{⑥}$

**Description**

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this product are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



D²Pak TO-262  
IRF2805SPbF IRF2805LPbF

**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	135⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	96⑥	
$I_{DM}$	Pulsed Drain Current ①	700	
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②	380	mJ
$E_{AS} (6 \text{ sigma})$	Single Pulse Avalanche Energy Tested Value⑧	1220	
$I_{AR}$	Avalanche Current⑩	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy⑦		mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ ③	2.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient(PCB Mounted, steady state)**	—	40	

HEXFET(R) is a registered trademark of International Rectifier.

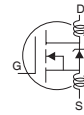
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International  
 Rectifier

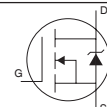
## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.06	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.9	4.7	mΩ	$V_{GS} = 10V, I_D = 104A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	91	—	—	S	$V_{DS} = 25V, I_D = 104A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	150	230	nC	$I_D = 104A$
$Q_{gs}$	Gate-to-Source Charge	—	38	57		$V_{DS} = 44V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	52	78		$V_{GS} = 10V$ ④
$t_{d(on)}$	Turn-On Delay Time	—	14	—	ns	$V_{DD} = 28V$
$t_r$	Rise Time	—	120	—		$I_D = 104A$
$t_{d(off)}$	Turn-Off Delay Time	—	68	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	110	—		$V_{GS} = 10V$ ④
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	5110	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	1190	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	210	—		$f = 1.0\text{MHz}$ , See Fig. 5
$C_{oss}$	Output Capacitance	—	6470	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	860	—		$V_{GS} = 0V, V_{DS} = 44V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance ⑤	—	1600	—		$V_{GS} = 0V, V_{DS} = 0V$ to $44V$



## Source-Drain Ratings and Characteristics

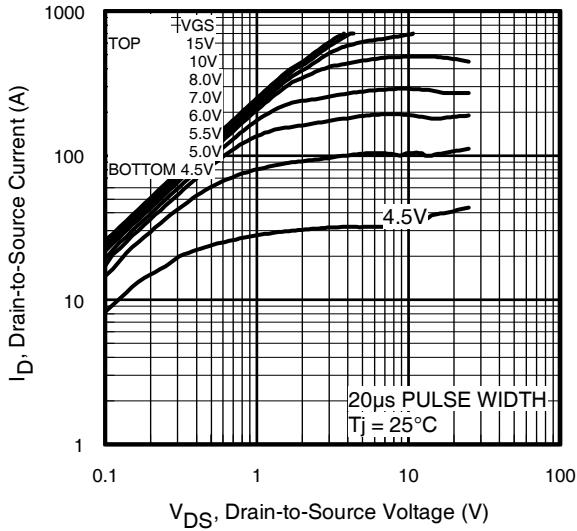
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	175	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	700		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 104A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	80	120	ns	$T_J = 25^\circ\text{C}, I_F = 104A$
$Q_{rr}$	Reverse Recovery Charge	—	290	430	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				



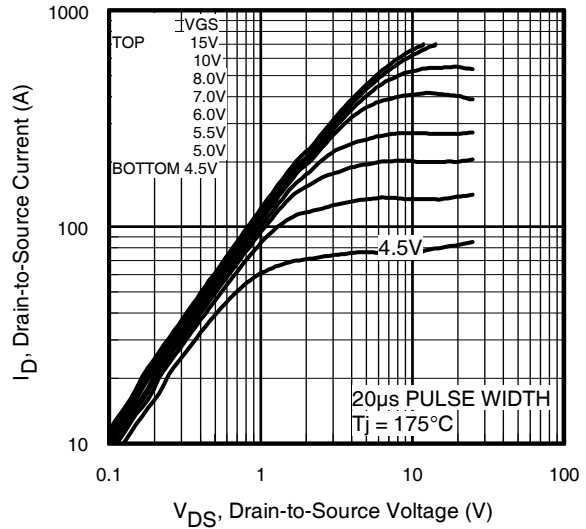
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Starting  $T_J = 25^\circ\text{C}, L = 0.08\text{mH}$   
 $R_G = 25\Omega, I_{AS} = 104A$ . (See Figure 12).
- ③  $I_{SD} \leq 104A, di/dt \leq 240A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .

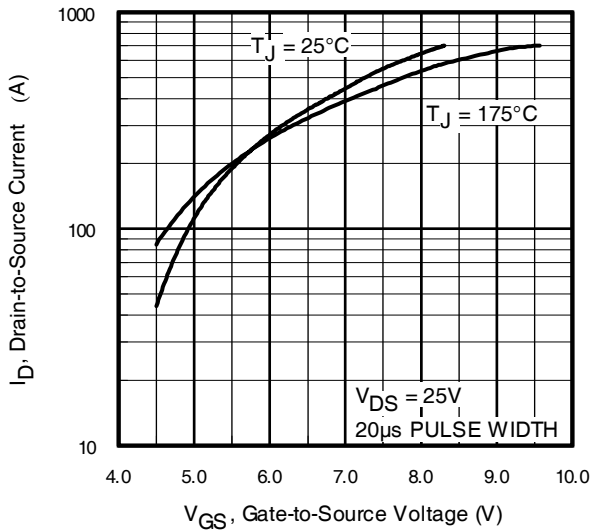
- ⑤  $C_{oss\ eff.}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑧ This value determined from sample failure population. 100% tested to this value in production.



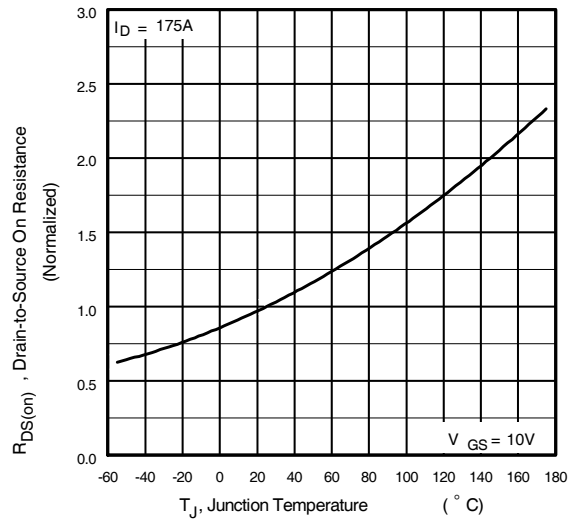
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

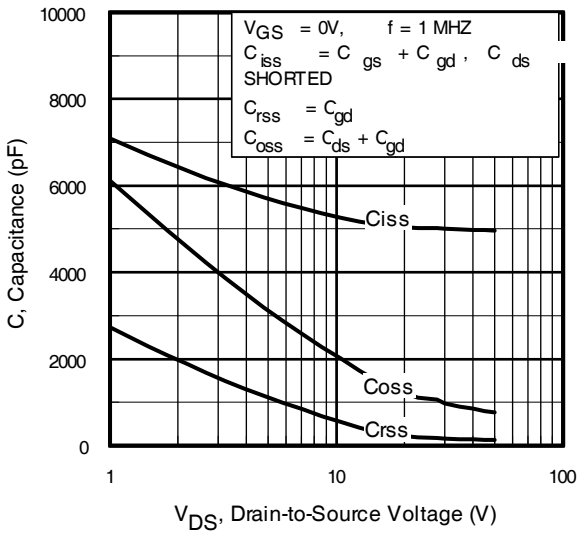


**Fig 3.** Typical Transfer Characteristics

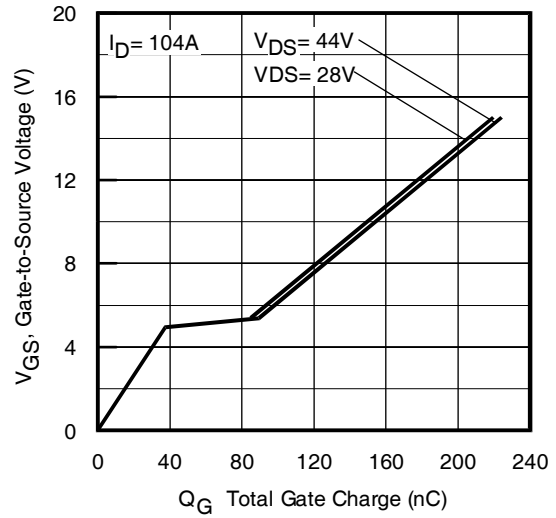


**Fig 4.** Normalized On-Resistance Vs. Temperature

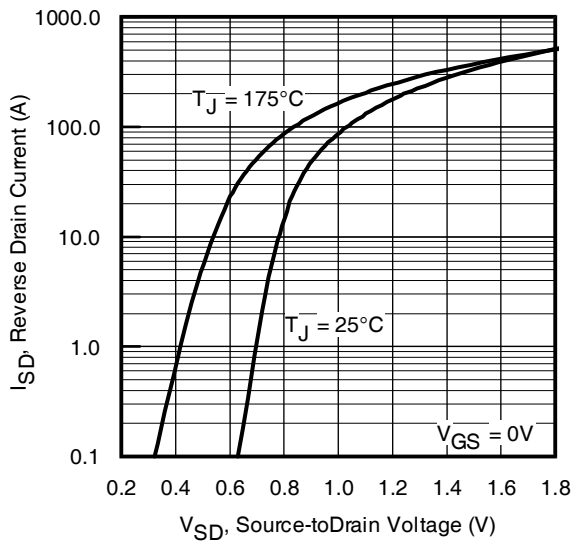
# IRF2805S/LPbF



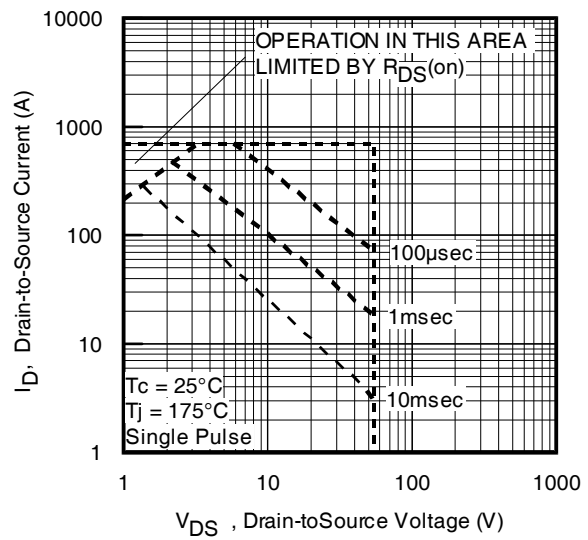
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



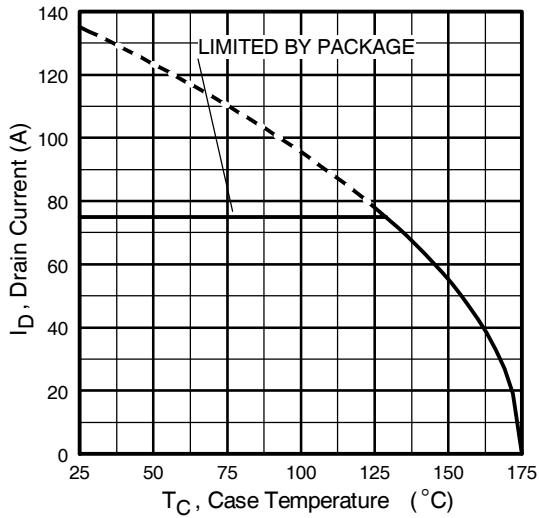
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



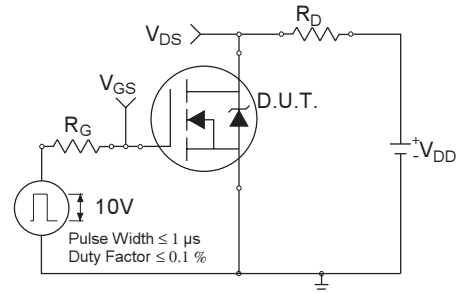
**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



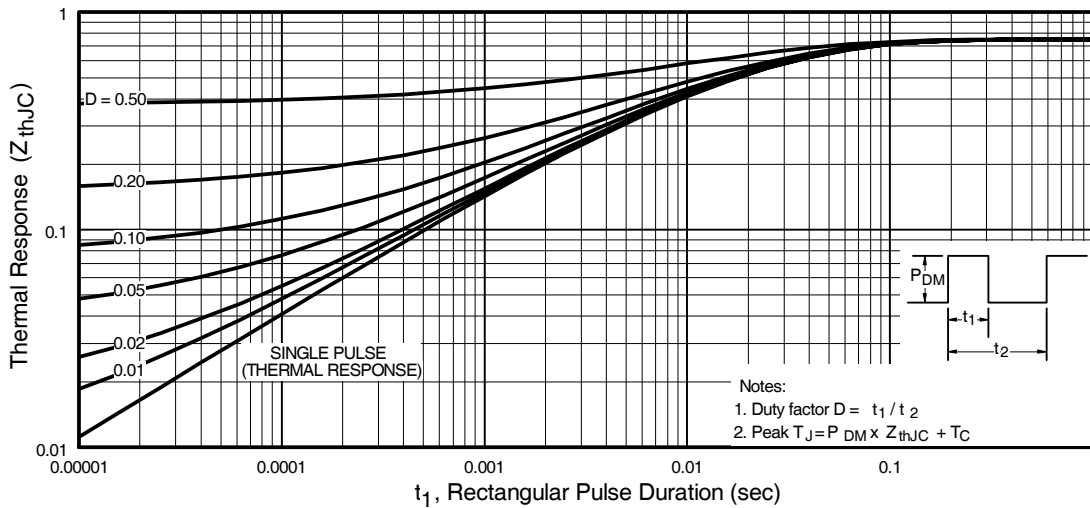
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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**Fig 12a.** Unclamped Inductive Test Circuit



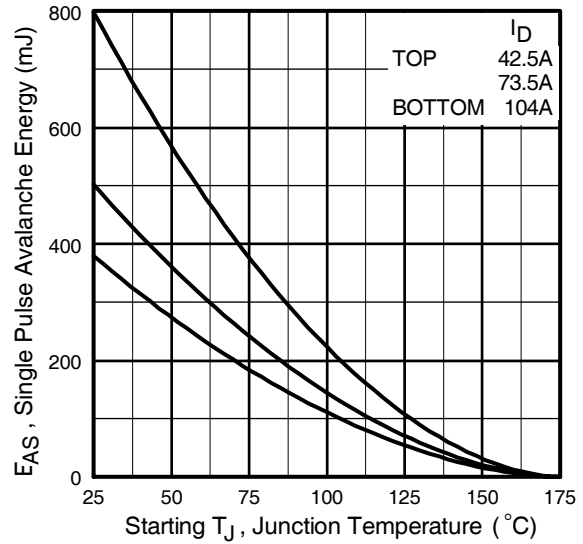
**Fig 12b.** Unclamped Inductive Waveforms



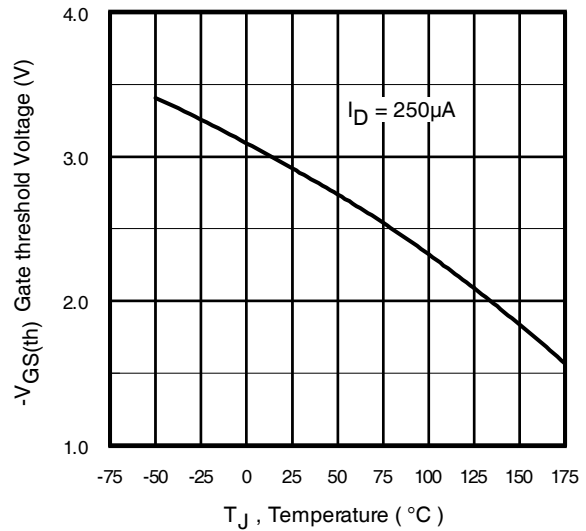
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature

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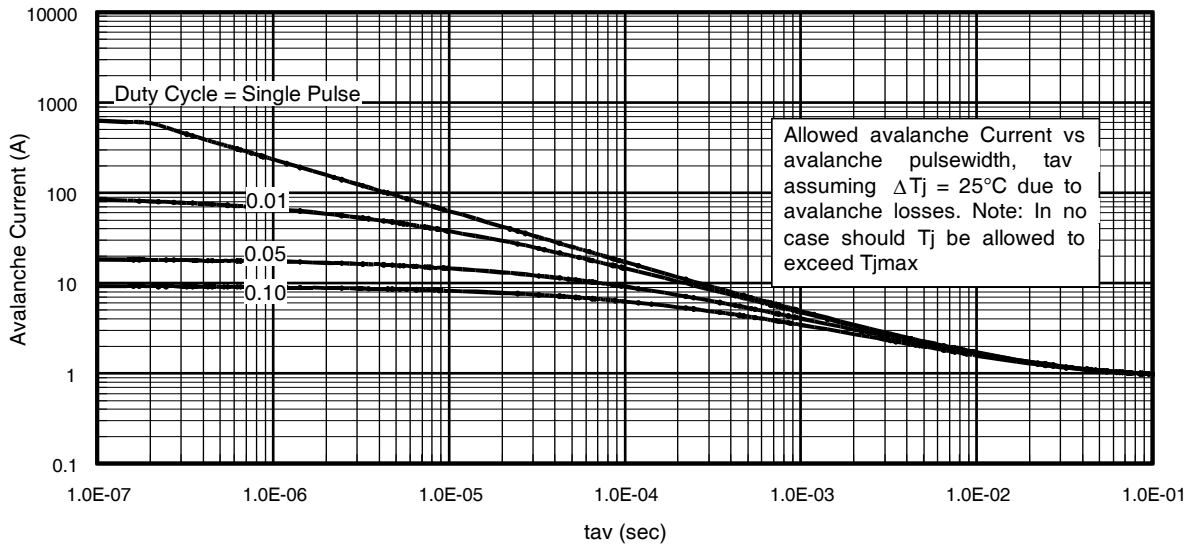


Fig 15. Typical Avalanche Current Vs.Pulsewidth

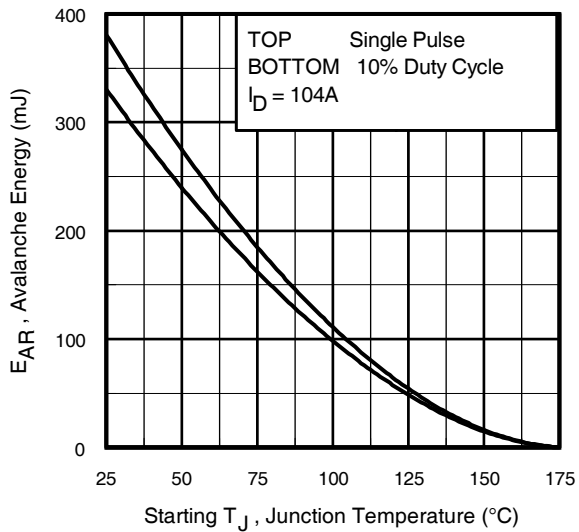


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

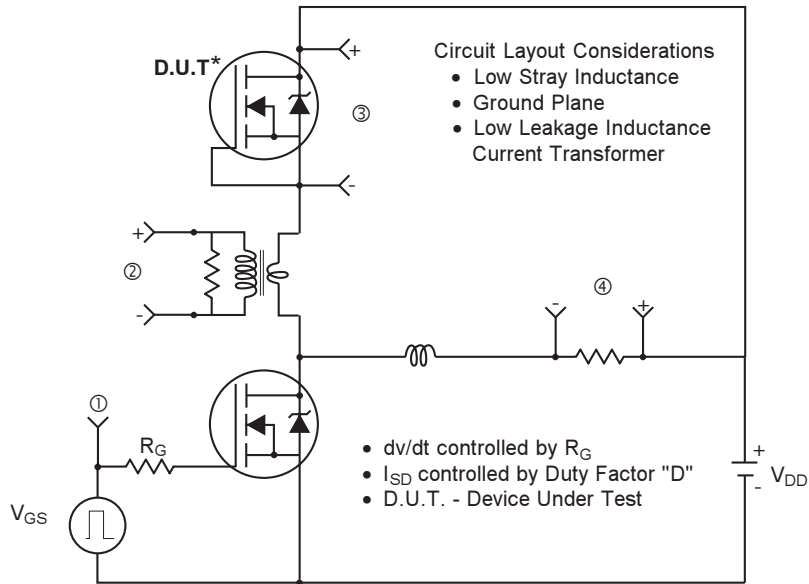
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
D = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

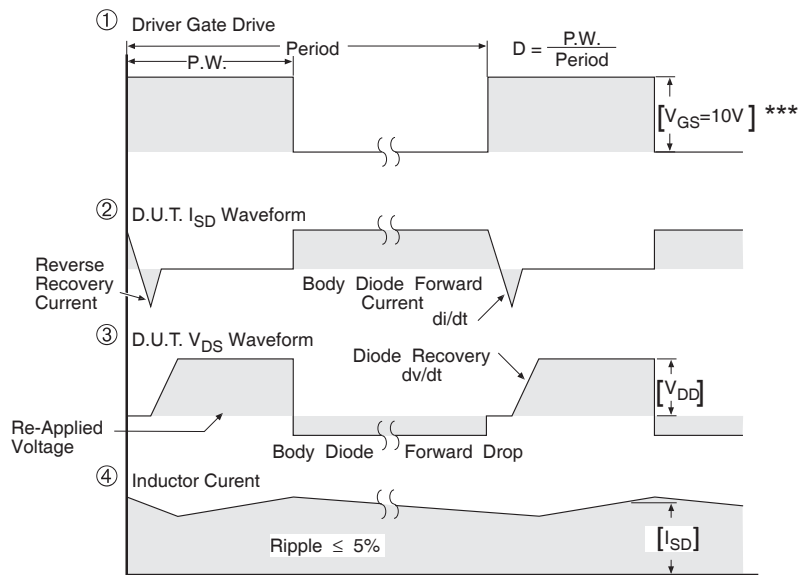
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



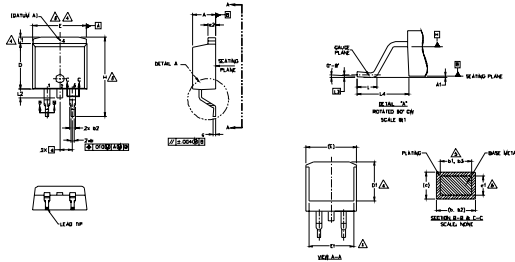
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 17.** For N-channel HEXFET® power MOSFETs



## D<sup>2</sup>Pak (TO-263AB) Package Outline

Dimensions are shown in millimeters (inches)



**LEAD ASSIGNMENTS**

**DIODES**

- 1.- ANODE (TWO DIE) / OPEN (ONE DIE)
- 2, 4.- CATHODE
- 3.- ANODE

**HEXFET**

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	-	1.65	-	.066	4
L2	-	1.78	-	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

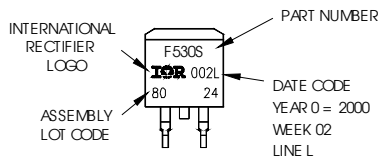
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

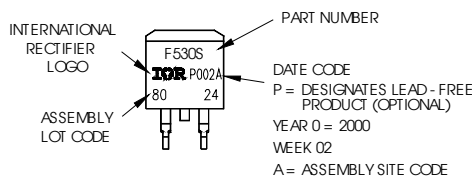
## D<sup>2</sup>Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position  
indicates "Lead - Free"



OR



**Notes:**

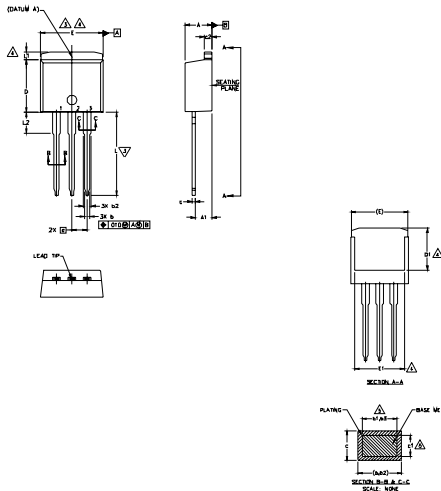
1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

# IRF2805S/LPbF

International  
**IR** Rectifier

## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
7. OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		4
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	
L2	3.56	3.71	.140	.146	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

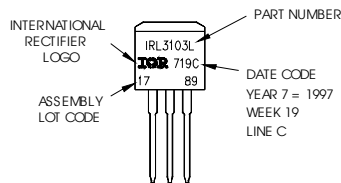
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

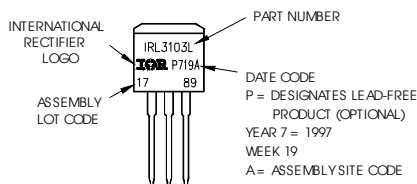
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



OR

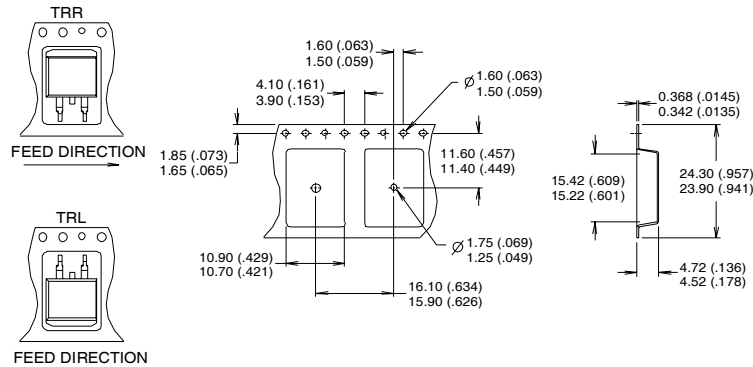


**Notes:**

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION MEASURED @ HUB.
  4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon Technologies\(英飞凌\)](#)