IFX1763 V50

Wide Input Range Low Noise 500mA 5V LDO

IFX1763XEJV50
IFX1763LDV50

Data Sheet

Rev. 1.11, 2015-01-30

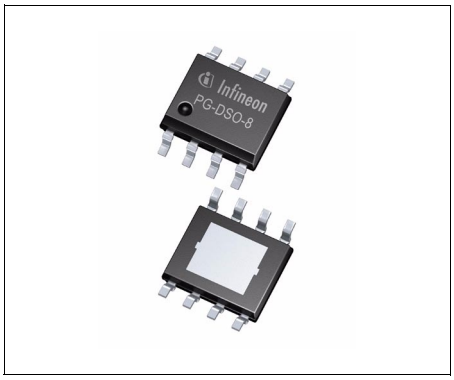
Standard Power

Wide Input Range Low Noise 500mA 5V LDO

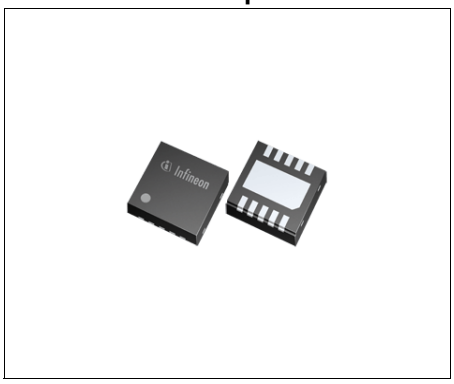
IFX1763XEJV50
IFX1763LDV50

RoHS

1 Overview



PG-DSO-8 Exposed Pad



PG-TSON-10

Features

- Low Noise down to 42 µV_{RMS} (BW = 10 Hz to 100 kHz)
- 500mA Current Capability
- Low Quiescent Current: 30 µA
- Wide Input Voltage Range up to 20 V
- Internal circuitry working down to 1.8 V
- 2.5% Output Voltage Accuracy (over full temperature and load range)
- Low Dropout Voltage: 350 mV
- Very low Shutdown Current: < 1 µA
- No Protection Diodes Needed
- Fixed Output Voltage: 5.0 V
- Stable with ≥ 3.3 µF Output Capacitor
- Stable with Aluminium, Tantalum or Ceramic Capacitors
- Reverse Battery Protection
- No Reverse Current
- Overcurrent and Overtemperature Protected
- PG-DSO-8 Exposed Pad and TSON-10 Exposed Pad Packages
- Green Product (RoHS compliant)

Applications

- Microcontroller Supply
- Battery-Powered Systems
- Noise Sensitive Instruments
- Radar Applications
- Image Sensors

The IFX1763 V50 is not qualified and manufactured according to the requirements of Infineon Technologies with regards to automotive and/or transportation applications. For automotive applications please refer to the Infineon TLx (TLE, TLS, TLF.....) voltage regulator products.

Type	Package	Marking
IFX1763XEJV50	PG-DSO-8 Exposed Pad	1763EV50
IFX1763LDV50	PG-TSON-10	176LV50

The IFX1763 V50 is a micropower, low noise, low dropout 5 V voltage regulator. The device is capable of supplying an output current of 500 mA with a dropout voltage of 350 mV. Designed for use in battery-powered systems, the low quiescent current of 30 µA makes it an ideal choice.

One feature of the IFX1763 V50 is its low output noise: by adding an external 0.01 µF bypass capacitor output noise values down to 42 μV_{RMS} over a 10 Hz to 100 kHz bandwidth can be reached. The IFX1763 V50 voltage regulator is stable with output capacitors as small as 3.3 µF. Small ceramic capacitors can be used without the series resistance required by many other regulators. Its internal protection circuitry includes reverse battery protection, current limiting and reverse current protection. The IFX1763 V50 is available in a PG-DSO-8 Exposed Pad and as well as in a TSON10 exposed pad package.

2 Block Diagram

Note: Pin numbers in the block diagram refer to the DSO-8 EP package type.

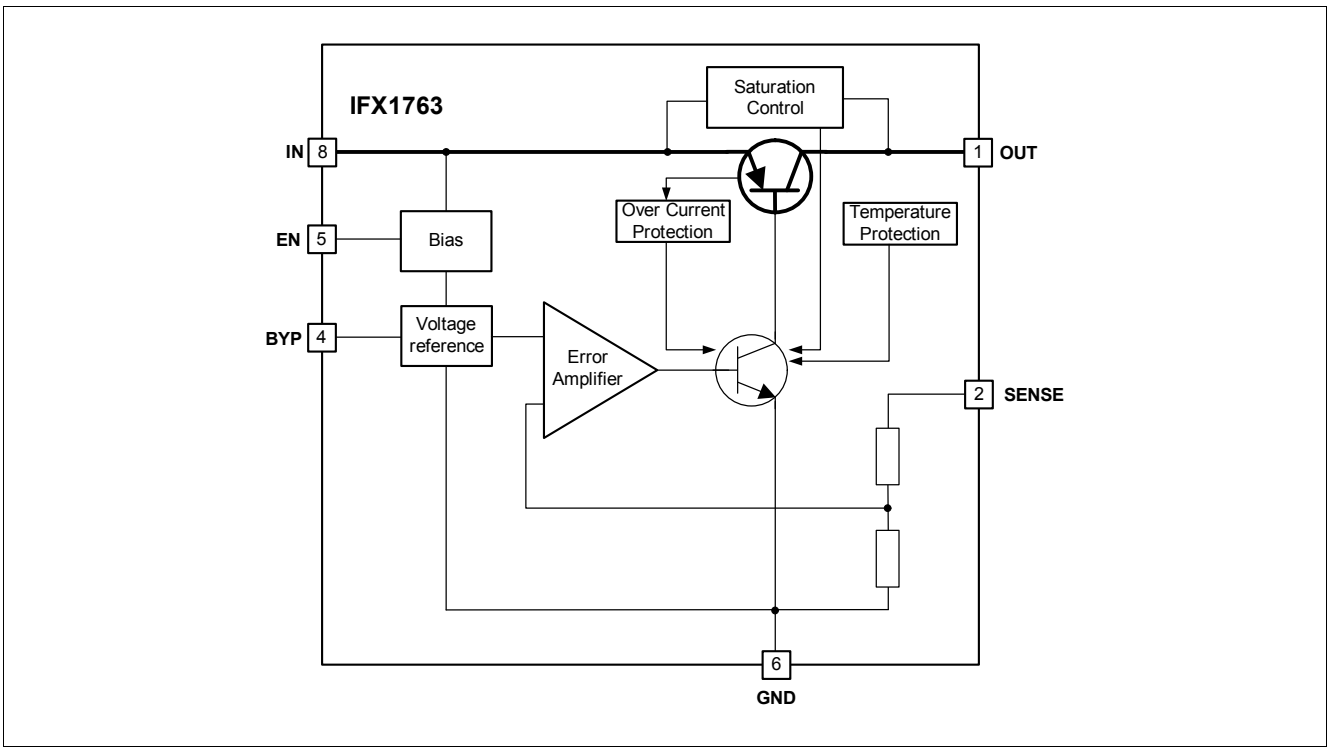


Figure 1 Block Diagram IFX1763 V50

3 Pin Configuration

3.1 Pin Assignment

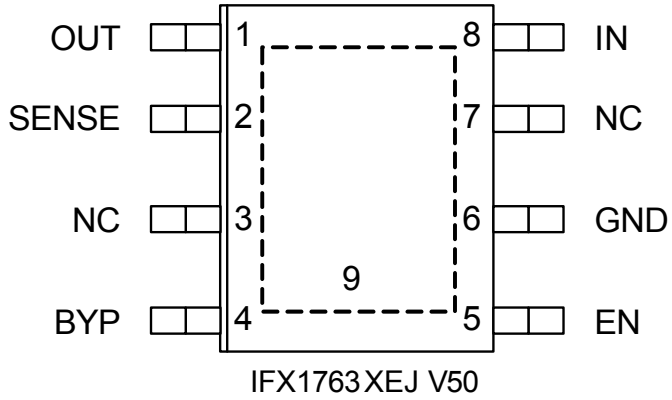


Figure 2 Pin Configuration of IFX1763XEJV50 in PG-DSO-8 Exposed Pad

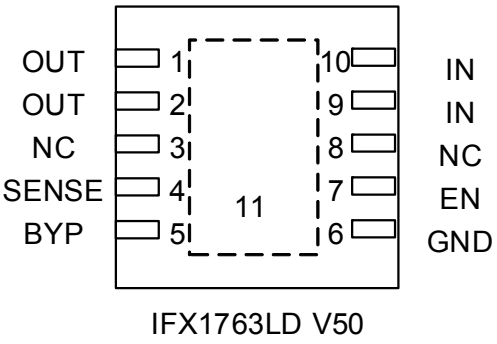


Figure 3 Pin Configuration of IFX1763LDV50 in PG-TSON10

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1 (DSO-8 EP) 1,2 (TSON-10)	OUT	**Output**. Supplies power to the load. For this pin a minimum output capacitor of 3.3 µF is required to prevent oscillations. Larger output capacitors may be required for applications with large transient loads in order to limit peak voltage transients or when the regulator is applied in conjunction with a bypass capacitor. For more details please refer to the section **"Application Information" on Page 19**.
2 (DSO-8 EP) 4 (TSON-10)	SENSE	**Output Sense.** The SENSE pin is the input to the error amplifier. This allows to achieve an optimized regulation performance in case of small voltage drops R_p that occur between regulator and load. In applications where such drops are relevant they can be eliminated by connecting the SENSE pin directly at the load. In standard configurations the SENSE pin can be connected directly to the OUT pin. For further details please refer to the section **"Kelvin Sense Connection" on Page 19**.
3, 7 (DSO-8 EP) 3, 8 (TSON-10)	NC	**No Connect.** The NC Pins have no connection to any internal circuitry. Connect either to GND or leave open.
4 (DSO-8) 5 (TSON-10)	BYP	**Bypass.** The BYP pin is used to bypass the reference of the IFX1763 V50 to achieve low noise performance. The BYP-pin is clamped internally to ±0.6 V (i.e. one V_{BE}). A small capacitor from the output to the BYP pin will bypass the reference to lower the output voltage noise[1]. If not used this pin must be left unconnected.
5 (DSO-8 EP) 7 (TSON-10)	EN	**Enable.** With the EN pin the IFX1763 V50 can be put into a low power shutdown state. The output will be off when the EN is pulled low. The EN pin can be driven by 5V logic or open-collector logic with pull-up resistor. The pull-up resistor is required to supply the pull-up current of the open-collector gate[2] and the EN pin current[3]. Please note that if the EN pin is not used it must be connected to V_{IN}. It must not be left floating.
6 (DSO-8 EP) 6,(TSON-10)	GND	**Ground.**
8 (DSO-8 EP) 9, 10 (TSON-10)	IN	**Input.** Via the input pin IN the power is supplied to the device. A capacitor at the input pin is required if the device is more than 6 inches away from the main input filter capacitor or if bigger inductance is present at the IN pin[4]. The IFX1763 V50 is designed to withstand reverse voltages on the Input pin with respect to GND and Output. In the case of reverse input (e.g. due to a wrongly attached battery) the device will act as if there is a diode in series with its input. In this way there will be no reverse current flowing into the regulator and no reverse voltage will appear at the load. Hence, the device will protect both - the device itself and the load.
9 (DSO-8 EP) 11 (TSON-10)	Tab	**Exposed Pad.** To ensure proper thermal performance, solder Pin 11 (exposed pad) of TSON10 to the PCB ground and tie directly to Pin 6. In the case of DSO-8 EP as well solder Pin 9 (exposed pad) to the PCB ground and tie directly to Pin 6.

1) A maximum value of 10 nF can be used for reducing output voltage noise over the bandwidth from 10 Hz to 100 kHz.
2) Normally several microamperes.
3) Typical value is 1 µA.
4) In general the output impedance of a battery rises with frequency, so it is advisable to include a bypass capacitor in battery-powered circuits. Depending on actual conditions an input capacitor in the range of 1 to 10 µF is sufficient.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Table 1 Absolute Maximum Ratings[1)]

T_j = -40 °C to +150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage							
Voltage	V_{IN}	-20	–	20	V	–	P_4.1.1
Output Voltage							
Voltage	V_{OUT}	-20	–	20	V	–	P_4.1.2
Input to Output Differential Voltage	V_{IN} - V_{OUT}	-20	–	20	V	–	P_4.1.3
Sense Pin							
Voltage	V_{SENSE}	-20	–	20	V	–	P_4.1.4
BYP Pin							
Voltage	V_{BYP}	-0.6	–	0.6	V		P_4.1.5
Enable Pin							
Voltage	V_{EN}	-20	–	20	V	–	P_4.1.6
Temperatures							
Junction Temperature	T_j	-40	–	150	°C	–	P_4.1.7
Storage Temperature	T_{stg}	-55	–	150	°C	–	P_4.1.8
ESD Susceptibility							
All Pins	V_{ESD}	-2	–	2	kV	HBM[2)]	P_4.1.9
All Pins	V_{ESD}	-1	–	1	kV	CDM[3)]	P_4.1.10

1) Not subject to production test, specified by design.
2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k Ω, 100 pF)
3) ESD susceptibility, Charged Device Model “CDM” according JEDEC JESD22-C101

Notes

1. *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
2. *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

4.2 Functional Range

Table 2 Functional Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Input Voltage Range	V_{IN}	5.5	–	20	V	–	P_4.2.1
Operating Junction Temperature	T_j	-40	–	125	°C	–	P_4.2.2

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Table 3 Thermal Resistance[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
IFX1763X EJ (PG-DSO-8 Exposed Pad)							
Junction to Case	R_{thJC}	–	7.0	–	K/W	–	P_4.3.1
Junction to Ambient	R_{thJA}	–	39	–	K/W	–[2)]	P_4.3.2
Junction to Ambient	R_{thJA}	–	155	–	K/W	Footprint only[3)]	P_4.3.3
Junction to Ambient	R_{thJA}	–	66	–	K/W	300 mm² heatsink area on PCB[3)]	P_4.3.4
Junction to Ambient	R_{thJA}	–	52	–	K/W	600 mm² heatsink area on PCB[3)]	P_4.3.5
IFX1763 LD (PG-TSON10)							
Junction to Case	R_{thJC}	–	6.4	–	K/W	–	P_4.3.6
Junction to Ambient	R_{thJA}	–	53	–	K/W	–[2)]	P_4.3.7
Junction to Ambient	R_{thJA}	–	183	–	K/W	Footprint only[3)]	P_4.3.8
Junction to Ambient	R_{thJA}	–	69	–	K/W	300 mm² heatsink area on PCB[3)]	P_4.3.9
Junction to Ambient	R_{thJA}	–	57	–	K/W	600 mm² heatsink area on PCB[3)]	P_4.3.10

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

5 Electrical Characteristics

5.1 Electrical Characteristics Table

Table 4 Electrical Characteristics

-40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Minimum Operating Voltage[1)]							
Minimum Operating Voltage	$V_{IN,min}$	–	1.8	2.3	V	I_{OUT} = 500 mA	P_5.1.1
Output Voltage[2)]							
Output Voltage	V_{OUT}	4.875	5.00	5.125	V	1 mA < I_{OUT} < 500 mA; 6 V < V_{IN} < 20 V	P_5.1.2
Line Regulation							
Line Regulation	ΔV_{OUT}	–	1	25	mV	ΔV_{IN} = 5.5 V to 20 V; I_{OUT} = 1 mA	P_5.1.3
Load Regulation							
Load Regulation	ΔV_{OUT}	–	16	32	mV	T_J = 25°C; V_{IN}= 6.0 V; ΔI_{OUT} = 1 to 500 mA	P_5.1.4
Load Regulation	ΔV_{OUT}	–	–	57	mV	V_{IN} = 6.0V; ΔI_{OUT} = 1 to 500 mA	P_5.1.5
Dropout Voltage[3)]							
Dropout Voltage	V_{DR}	–	110	140	mV	I_{OUT} = 10 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.6
Dropout Voltage	V_{DR}	–	–	190	mV	I_{OUT} = 10 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.7
Dropout Voltage	V_{DR}	–	170	200	mV	I_{OUT} = 50 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.8
Dropout Voltage	V_{DR}	–	–	250	mV	I_{OUT} = 50 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.9
Dropout Voltage	V_{DR}	–	200	230	mV	I_{OUT} = 100 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.10
Dropout Voltage	V_{DR}	–	–	300	mV	I_{OUT} = 100 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.11
Dropout Voltage	V_{DR}	–	350	380	mV	I_{OUT} = 500 mA; V_{IN} = $V_{OUT,nom}$; T_J = 25°C	P_5.1.12
Dropout Voltage	V_{DR}	–	–	480	mV	I_{OUT} = 500 mA; V_{IN} = $V_{OUT,nom}$	P_5.1.13
GND Pin Current[4)]							
GND Pin Current	I_{GND}	–	30	60	µA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 0 mA	P_5.1.14
GND Pin Current	I_{GND}	–	50	100	µA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 1 mA	P_5.1.15

Table 4 Electrical Characteristics (cont'd)

-40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
GND Pin Current	I_{GND}	–	300	850	µA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 50 mA	P_5.1.16
GND Pin Current	I_{GND}	–	0.7	2.2	mA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 100 mA	P_5.1.17
GND Pin Current	I_{GND}	–	3	8	mA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 250 mA	P_5.1.18
GND Pin Current	I_{GND}	–	11	22	mA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 500 mA; T_J ≥ 25°C	P_5.1.19
GND Pin Current	I_{GND}	–	11	31	mA	V_{IN} = $V_{OUT,nom}$; I_{OUT} = 500 mA; T_J < 25°C	P_5.1.20
Quiescent Current in Shutdown							
Quiescent Current in Off-Mode (EN-pin low)	I_q	–	0.1	1	µA	V_{IN} = 6 V; V_{EN} = 0 V; T_J = 25°C	P_5.1.21
Enable							
Enable Threshold High	$V_{th,EN}$	–	0.8	2.0	V	V_{OUT} = Off to On	P_5.1.22
Enable Threshold Low	$V_{tl,EN}$	0.25	0.65	–	V	V_{OUT} = On to Off	P_5.1.23
EN Pin Current[5)]	I_{EN}	–	0.01	–	µA	V_{EN} = 0 V; T_J = 25°C	P_5.1.24
EN Pin Current[5)]	I_{EN}	–	1	–	µA	V_{EN} = 20 V; T_J = 25°C	P_5.1.25
Output Voltage Noise[6)]							
Output Voltage Noise	e_{no}	–	55	–	μV_{RMS}	C_{OUT} = 10 µF ceramic; C_{BYP} = 10 nF; I_{OUT} = 500 mA; (BW = 10 Hz to100 kHz)	P_5.1.26
Output Voltage Noise	e_{no}	–	44	–	μV_{RMS}	C_{OUT} = 10µF ceramic +250mΩ resistor in series; C_{BYP} = 10 nF; I_{OUT} = 500 mA; (BW = 10 Hz to100 kHz)	P_5.1.27
Output Voltage Noise	e_{no}	–	42	–	μV_{RMS}	C_{OUT} = 22 µF ceramic; C_{BYP} = 10 nF; I_{OUT} = 500 mA; (BW = 10 Hz to100 kHz)	P_5.1.28
Output Voltage Noise	e_{no}	–	42	–	μV_{RMS}	C_{OUT} = 22 µF ceramic +250mΩ resistor in series; C_{BYP} = 10 nF; I_{OUT} = 500 mA; (BW = 10 Hz to100 kHz)	P_5.1.29
Power Supply Ripple Rejection[6)]							
Power Supply Ripple Rejection	$PSRR$	50	65	–	dB	V_{IN} - V_{OUT} = 1.5 V (avg); V_{RIPPLE} = 0.5 Vpp; f_r = 120 Hz; I_{OUT} = 500mA	P_5.1.30

Table 4 Electrical Characteristics (cont'd)

-40 °C < T_j < 125 °C; all voltages with respect to ground; positive current defined flowing out of pin; unless otherwise specified.

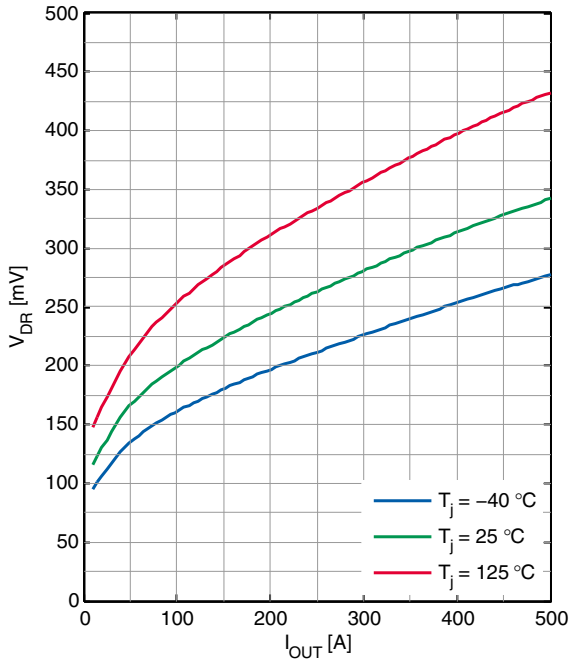
Parameter	Symbol	Values			Unit	Note / Test Condition	Number
		Min.	Typ.	Max.			
Output Current Limitation							
Output Current Limit	$I_{OUT,limit}$	520	–	–	mA	V_{IN} = 7 V; V_{OUT} = 0 V	P_5.1.31
Output Current Limit	$I_{OUT,limit}$	520	–	–	mA	V_{IN} = $V_{OUT,nom}$ + 1 V ΔV_{OUT} = -0.1 V	P_5.1.32
Input Reverse Leakage Current							
Input Reverse Leakage	$I_{leak,rev}$	–	–	1	mA	V_{IN} = -20 V; V_{OUT} = 0 V	P_5.1.33
Reverse Output Current[7]							
Reverse Output Current	$I_{Reverse}$	–	10	20	µA	V_{OUT} = $V_{OUT,nom}$; V_{IN} < $V_{OUT,nom}$; T_J = 25°C	P_5.1.34
Output Capacitor[6]							
Output Capacitance	C_{OUT}	3.3	–	–	µF	C_{BYP} = 0 nF	P_5.1.35
ESR	ESR	–[8]	–	3	Ω	–	P_5.1.36

1) This parameter defines the minimum input voltage for which the device is powered up and provides the maximum nominal output current of 500 mA. Under this minimum input voltage condition the IFX1763 V50 starts to be in tracking mode and the output voltage will typically be in the range of around 1 V while providing the 500 mA.
2) The operation conditions are limited by the maximum junction temperature. The regulated output voltage specification will only apply for conditions where the limit of the maximum junction temperature is fulfilled. It will therefore not apply for all possible combinations of input voltage and output current. When operating at maximum input voltage, the output current must be limited for thermal reasons. The same holds true when operating at maximum output current where the input voltage range must be limited for thermal reasons.
3) The dropout voltage is the minimum input to output voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage will be equal to V_{IN} - V_{DR}.
4) GND-pin current is tested with V_{IN} = $V_{OUT,nom}$ and a current source load. This means that this parameter is tested while being in dropout condition and thus reflects a worst case condition. The GND-pin current will in most cases decrease slightly at higher input voltages - please also refer to the corresponding typical performance graphs.
5) The EN pin current flows into EN pin.
6) Not subject to production test, specified by design.
7) Reverse output current is tested with the IN pin grounded and the OUT pin forced to the rated output voltage. This current flows into the OUT pin and out of the GND pin.
8) C_{BYP} = 0 nF, C_{OUT} ≥ 3.3 µF; please note that for cases where a bypass capacitor at BYP is used - depending on the actual applied capacitance of C_{OUT} and C_{BYP} - a minimum requirement for ESR may apply. For further details please also refer to the corresponding typical performance graph.

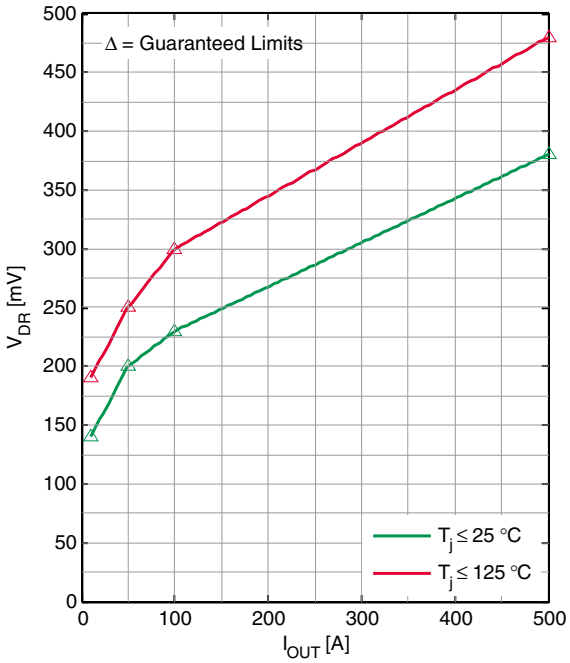
Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specified mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

6 Typical Performance Characteristics

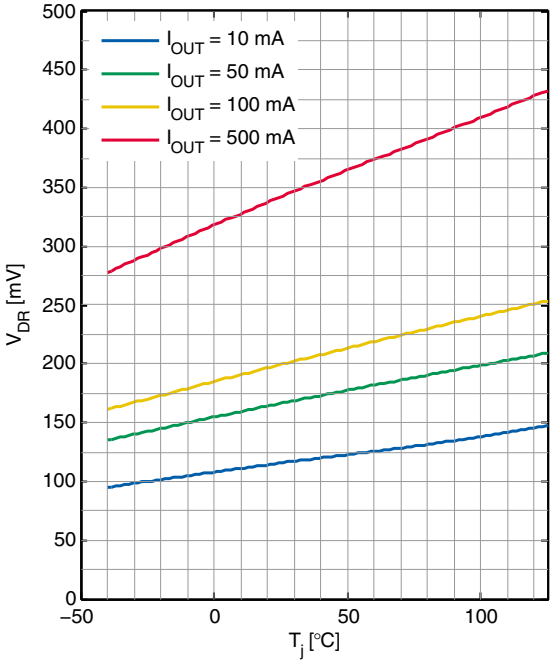
Dropout Voltage V_{DR} versus Output Current I_{OUT}



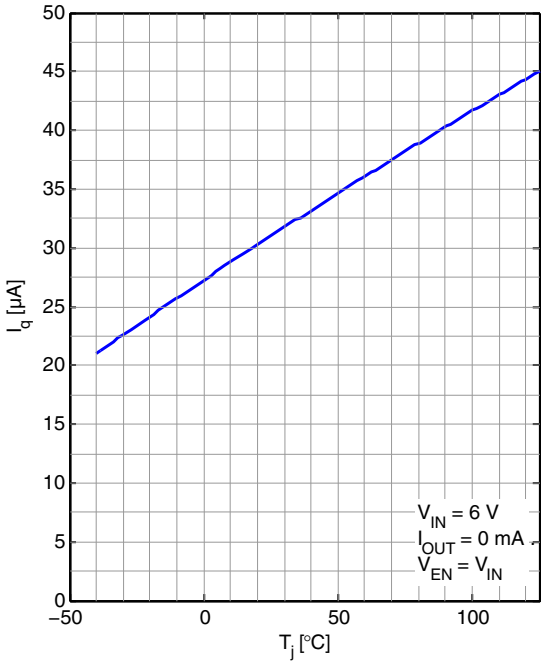
Guaranteed Dropout Voltage V_{DR} versus Output Current I_{OUT}



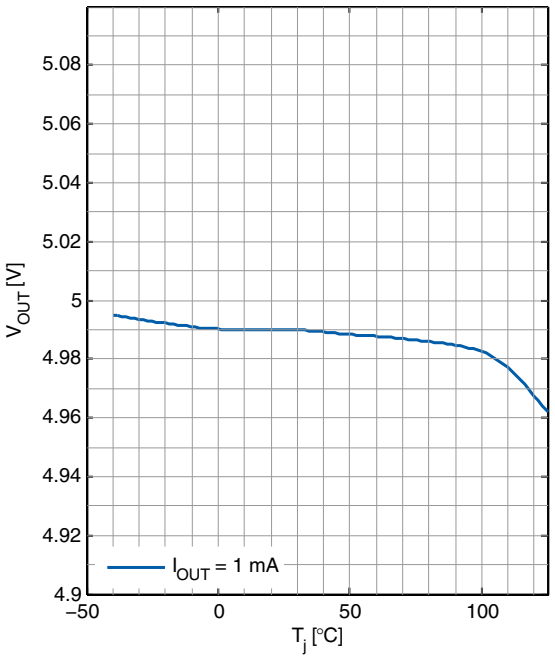
Dropout Voltage V_{DR} versus Junction Temperature T_J



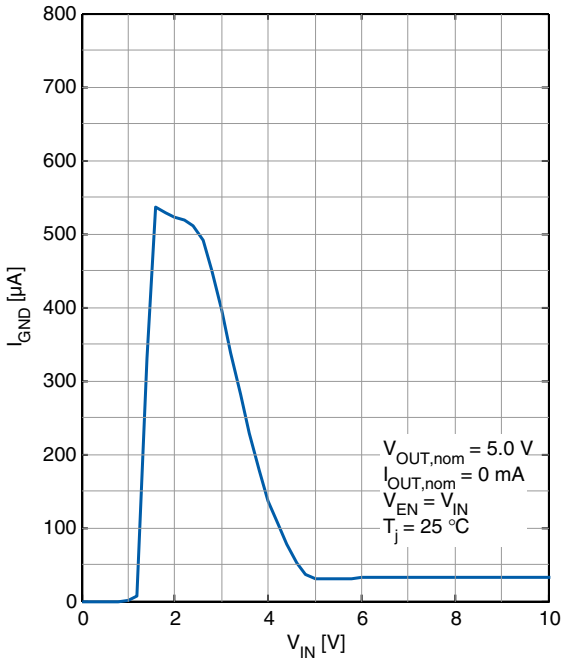
Quiescent Current versus Junction Temperature T_J



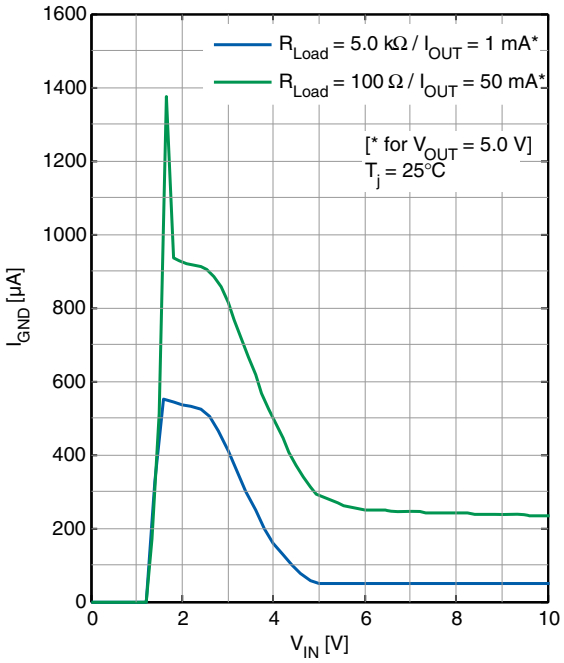
Output Voltage V_{OUT} versus Junction Temperature T_J



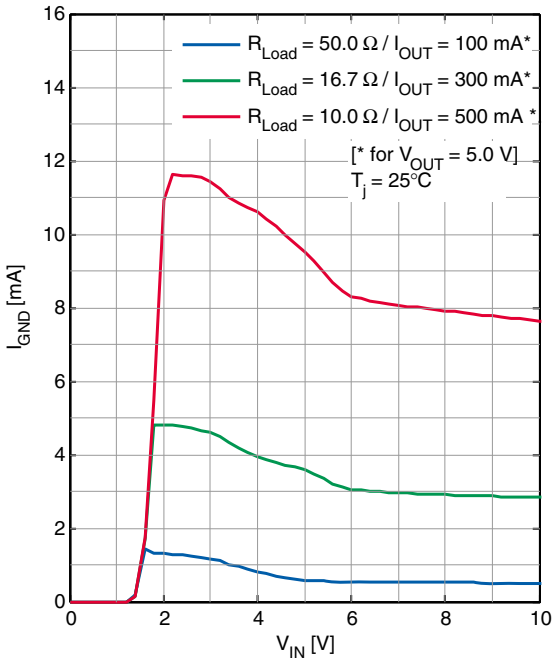
Quiescent Current I_q versus Input Voltage V_{IN}



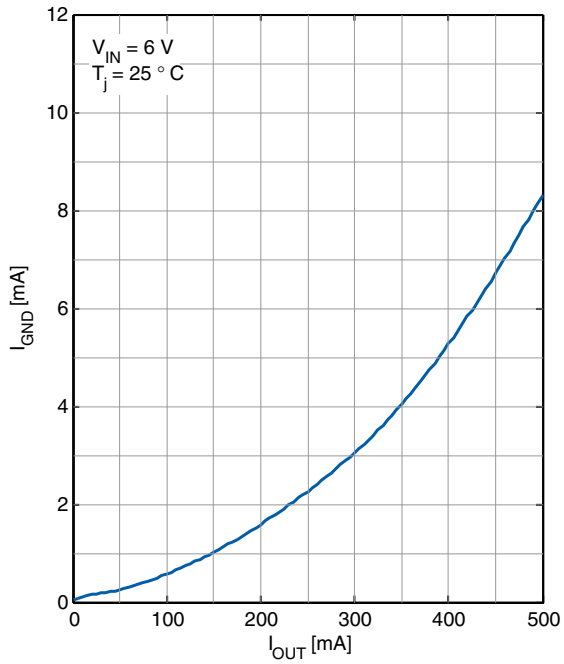
GND Current I_{GND} versus Input Voltage V_{IN}



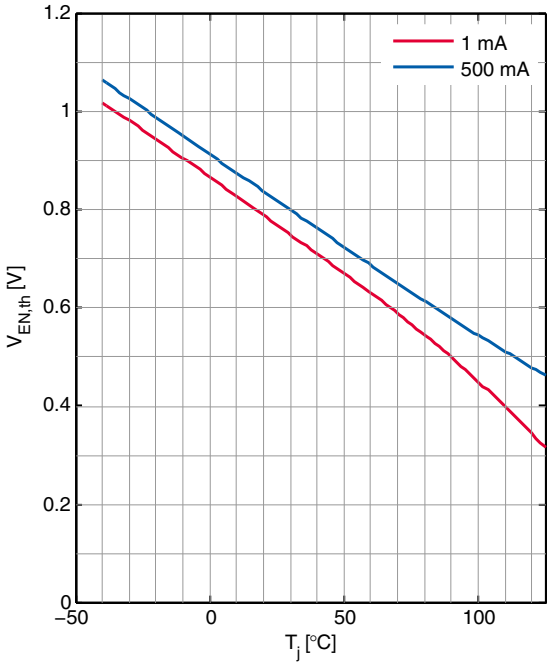
GND Current I_{GND} versus Input Voltage V_{IN}



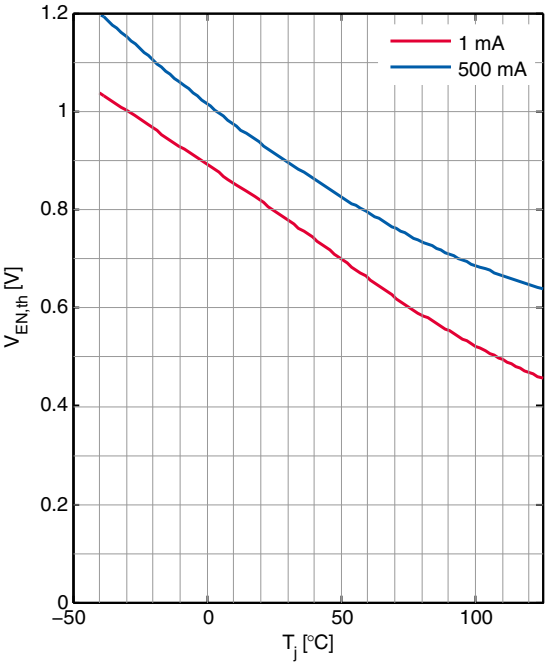
GND Current I_{GND} versus Output Current I_{OUT}



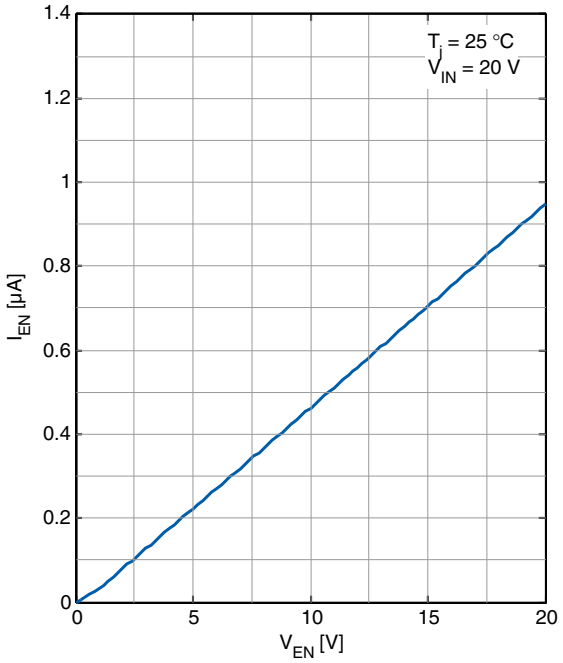
EN Pin Threshold (On-to-Off) versus Junction Temperature T_J



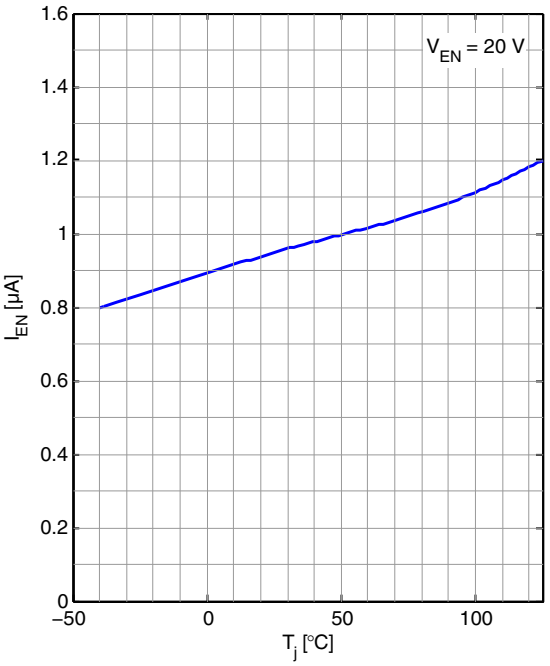
EN Pin Threshold (Off-to-On) versus Junction Temperature T_J



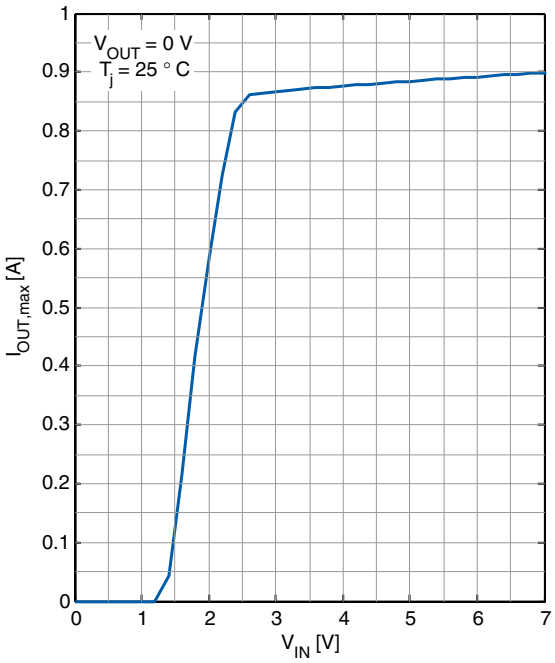
EN Pin Current I_{EN} versus EN Pin Voltage V_{EN}



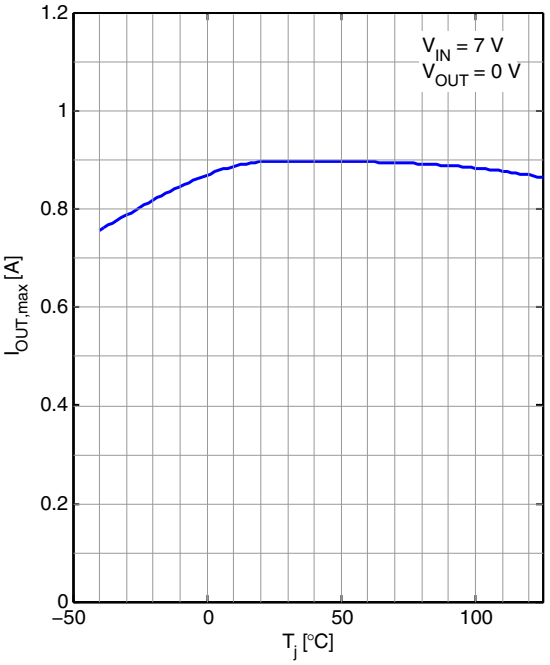
EN Pin Current versus Junction Temperature T_J



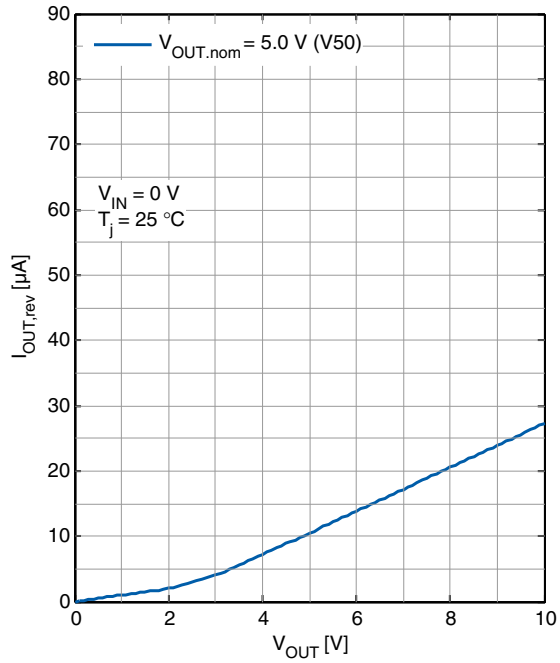
Current Limit versus Input Voltage V_{IN}



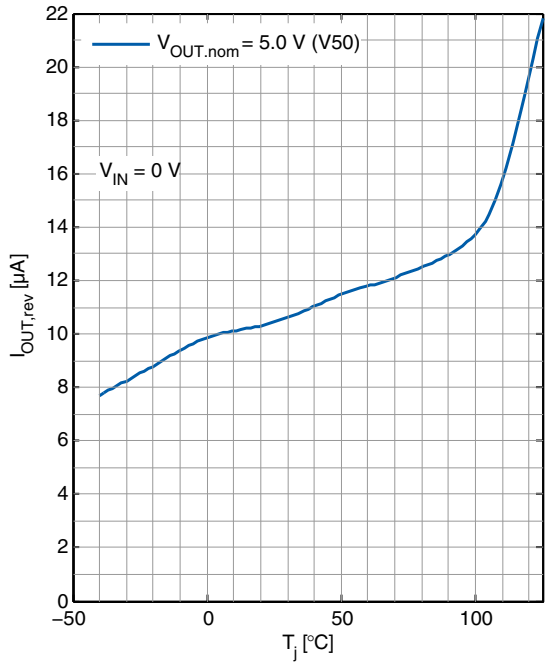
Current Limit versus Junction Temperature T_J



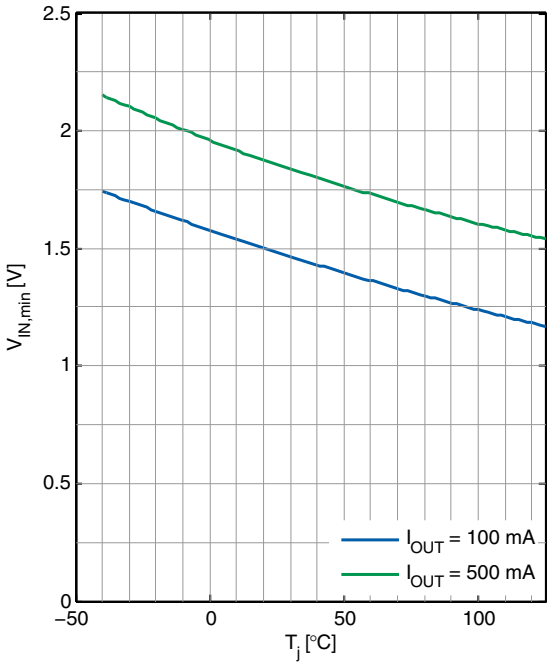
Reverse Output Current versus Output Voltage V_{OUT}



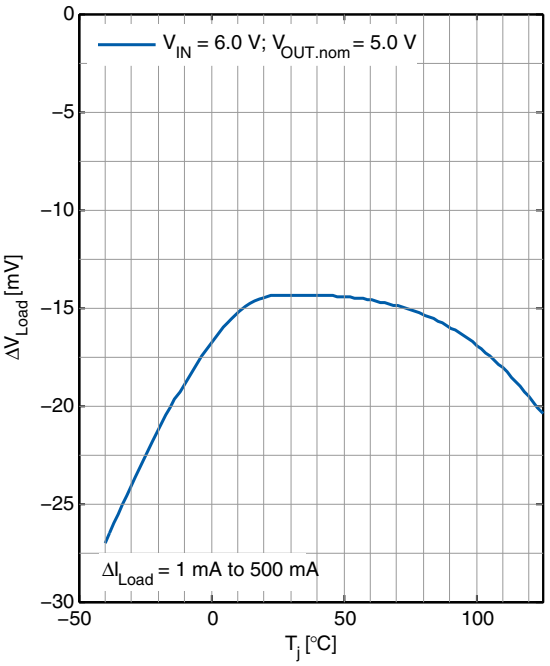
Reverse Output Current versus Junction Temperature T_J



Minimum Input Voltage[1] versus Junction Temperature T_J

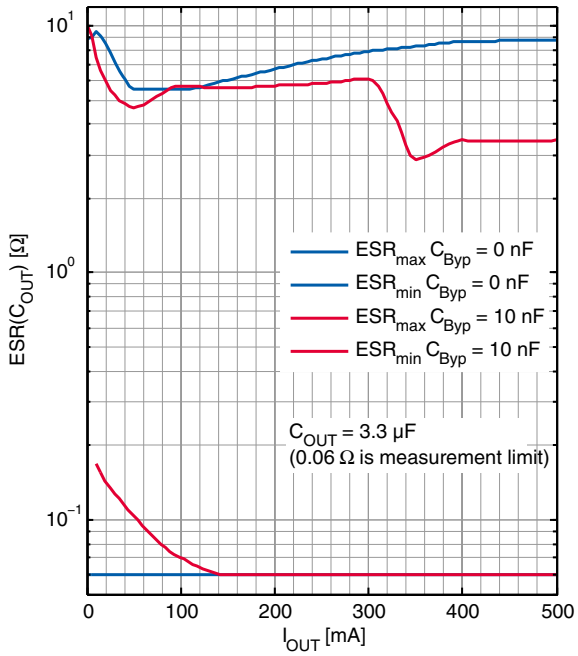


Load Regulation versus Junction Temperature T_J

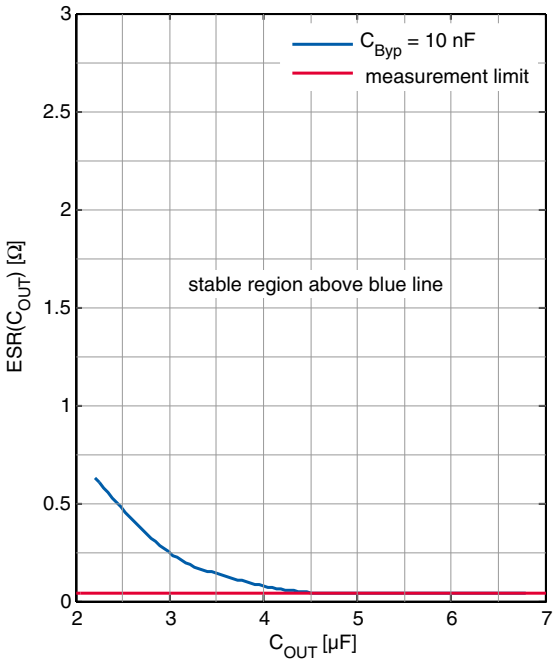


1) V_{IN},min is referred here as the minimum input voltage for which the requested current is provided and V_{OUT} reaches 1 V.

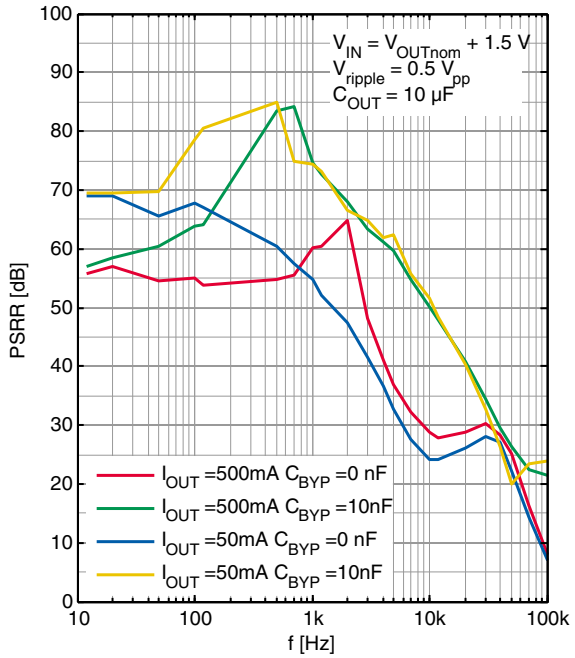
ESR Stability versus Output Current I_{OUT} (for C_{OUT} = 3.3µF)



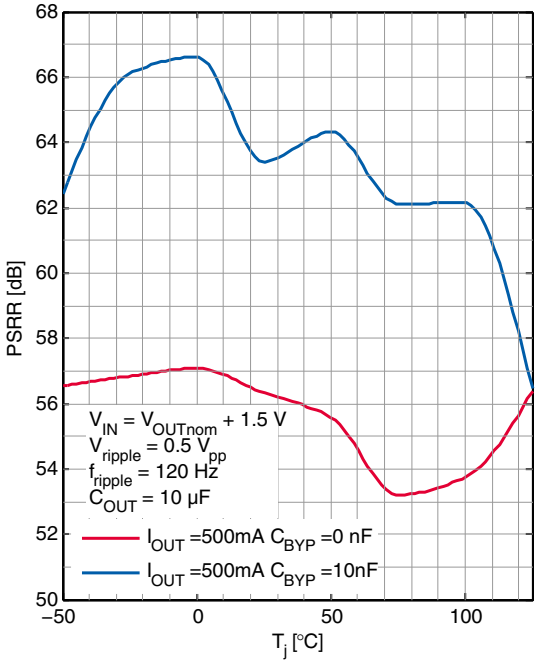
ESR(C_{OUT}) with C_{BYP} = 10 nF versus Output Capacitance C_{OUT}



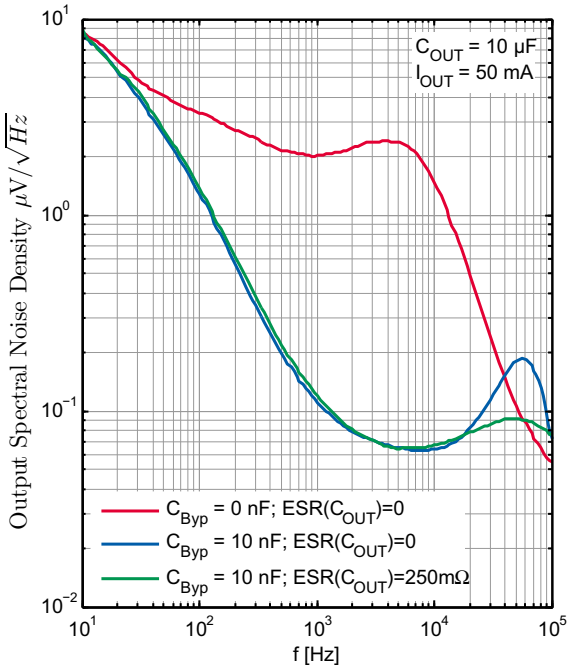
Input Ripple Rejection PSRR versus Frequency f



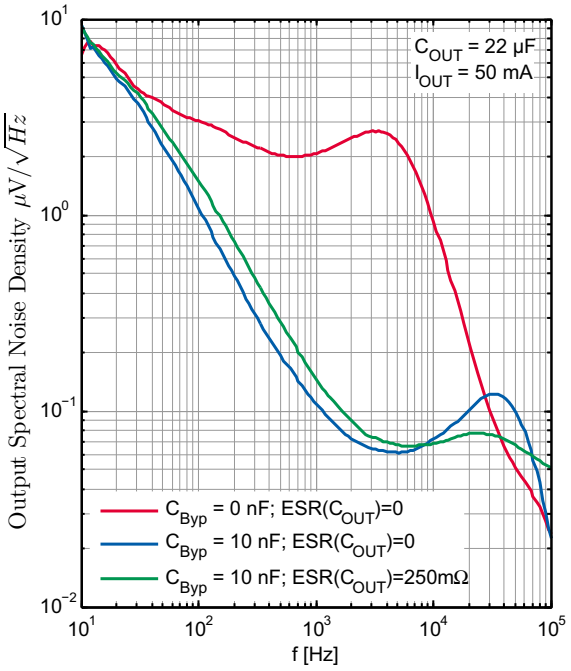
Input Ripple Rejection PSRR versus Junction Temperature T_J



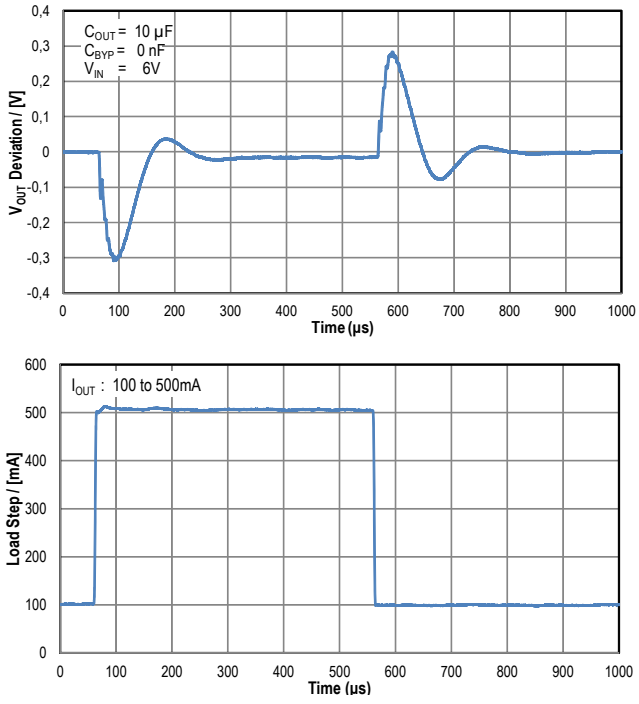
Output Noise Spectral Density versus Frequency (C_{OUT} = 10µF, I_{OUT} = 50mA[1])



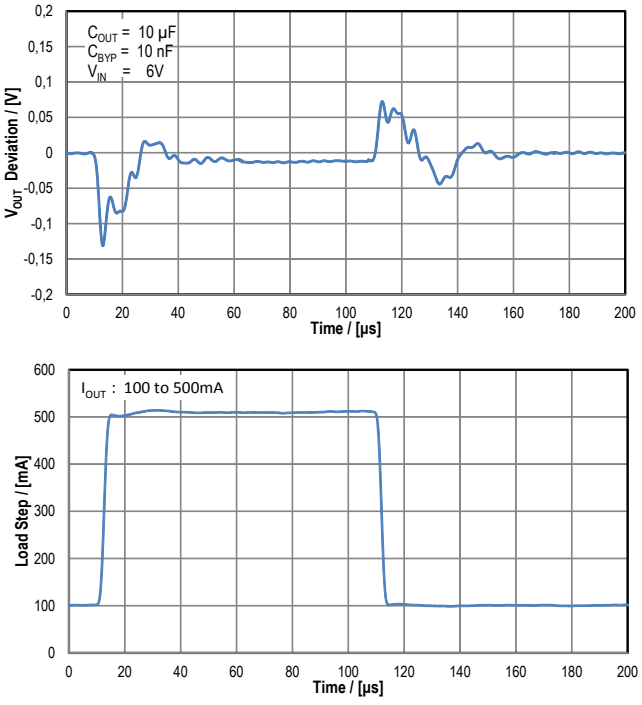
Output Noise Spectral Density versus Frequency (C_{OUT} = 22µF, I_{OUT} = 50mA[1])



Transient Response C_{BYP} = 0nF



Transient Response C_{BYP} = 10nF



1) Load condition 50mA is representing a worst case condition with regard to output voltage noise performance.

7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

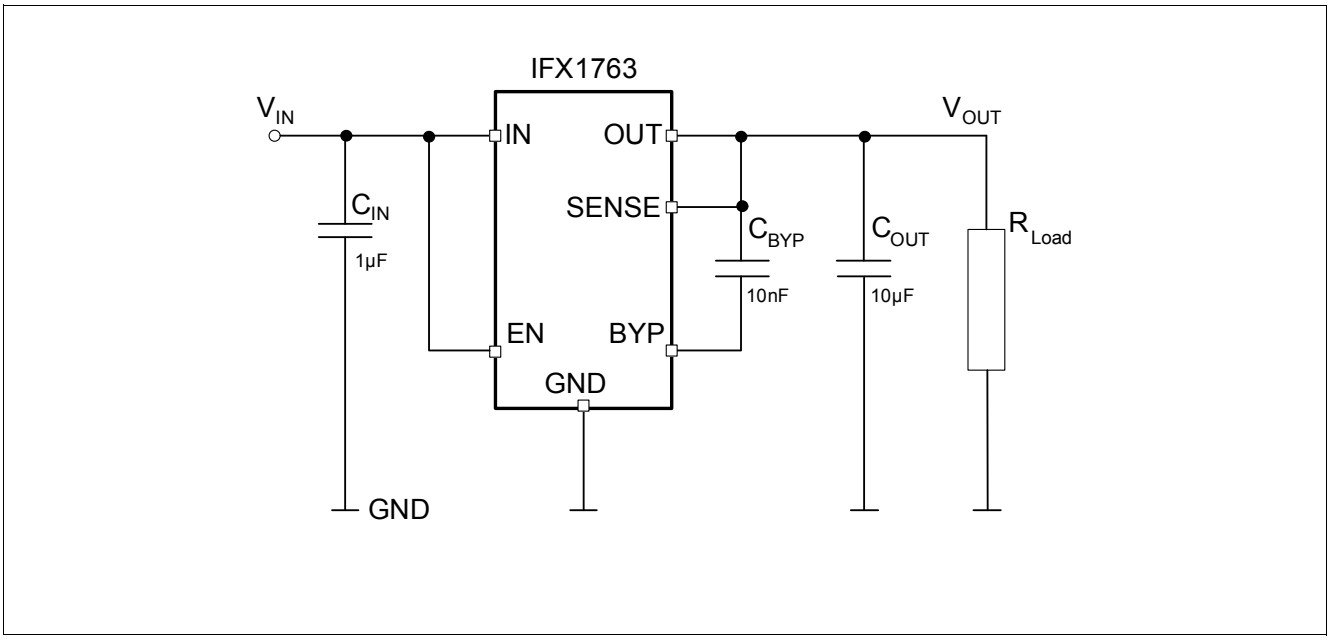


Figure 4 Typical Application Circuit IFX1763 V50

Note: This is a very simplified example of an application circuit. The function must be verified in the real application[1)2)].

The IFX1763 V50 is a 500 mA low dropout regulator with very low quiescent current and Enable-functionality. The device is capable of supplying 500 mA at a dropout voltage of 350 mV. Output voltage noise numbers down to 42 μV_{RMS} can be achieved over a 10 Hz to 100 kHz bandwidth with the addition of a 10 nF reference bypass capacitor. The usage of a reference bypass capacitor will additionally improve transient response of the regulator, lowering the settling time for transient load conditions. The device has a low operating quiescent current of typical 30 µA that drops to less than 1 µA in shutdown (EN-pin pulled to low level). The device also incorporates several protection features which makes it ideal for battery-powered systems. It is protected against both reverse input and reverse output voltages. In battery backup applications where the output can be held up by a backup battery when the input is pulled to ground the device behaves like it has a diode in series with its output and prevents reverse current flow.

7.1 Kelvin Sense Connection

The SENSE pin of the IFX1763 V50 is the input to the error amplifier. An optimum regulation will be obtained at the point where the SENSE pin is connected to the OUT pin of the regulator. In critical applications however small voltage drops can be caused by the resistance R_p of the PC-traces and thus may lower the resulting voltage at the load. This effect may be eliminated by connecting the SENSE pin to the output as close as possible at the load

1) Please note that in case a non-negligible inductance at IN pin is present, e.g. due to long cables, traces, parasitics, etc, a bigger input capacitor C_{IN} may be required to filter its influence. As a rule of thumb if the IN pin is more than six inches away from the main input filter capacitor an input capacitor value of C_{IN} = 10 µF is recommended.

2) For specific needs a small optional resistor may be placed in series to very low ESR output capacitors C_{OUT} for enhanced noise performance (for details please see **“Bypass Capacitance and Low Noise Performance” on Page 20**).

(see **Figure 5**). Please note that the voltage drop across the external PC trace will add up to the dropout voltage of the regulator.

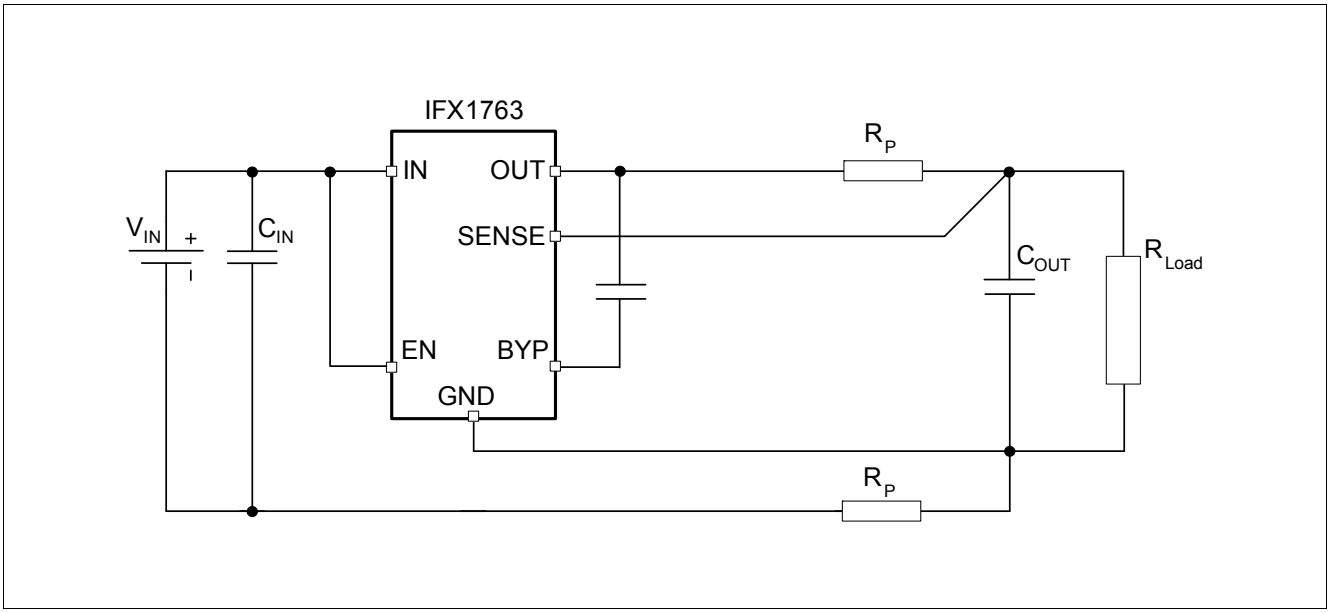


Figure 5 Kelvin Sense Connection

7.2 Bypass Capacitance and Low Noise Performance

The IFX1763 V50 regulator may be used in combination with a bypass capacitor connecting the OUT pin to the BYP pin in order to minimize output voltage noise[1].This capacitor will bypass the reference of the regulator, providing a low frequency noise pole. The noise pole provided by such a bypass capacitor will lower the output voltage noise in the considered bandwidth. For a given output voltage actual numbers of the output voltage noise will - next to the bypass capacitor itself - be dependent on the capacitance of the applied output capacitor and its ESR: In case of applying the IFX1763 V50 with a bypass capacitor of 10 nF in combination with a (low ESR) ceramic C_{OUT} of 10 µF will result in output voltage noise numbers of typical 55 μV_{RMS}. This Output Noise level can be reduced to typical 44 μV_{RMS} under the same conditions by adding a small resistance of ~250 mΩ in series to the 10 µF ceramic output capacitor acting as additional ESR. A reduction of the output voltage noise can also be achieved by increasing capacitance of the output capacitor. For C_{OUT} = 22 µF (ceramic low ESR) the output voltage noise will be typical 42 μV_{RMS}. For output capacitor values of 22 µF or bigger adding resistance in series to C_{OUT} does not further lower output noise numbers significantly anymore. For further details please also see **"Output Voltage Noise6)" on Page 10**,, of the Electrical Characteristics. Please note that next to reducing the output voltage noise level the usage of a bypass capacitor has the additional benefit of improving transient response which will be also explained in the next chapter. However one needs to take into consideration that on the other hand the regulator start-up time is proportional to the size of the bypass capacitor and slows down to values around 15 ms when using a 10 nF bypass capacitor in combination with a 10 µF C_{OUT} output capacitor.

7.3 Output Capacitance Requirements and Transient Response

The IFX1763 V50 is designed to be stable with a wide range of output capacitors. The ESR of the output capacitor is an essential parameter with regard to stability, most notably with small capacitors. A minimum output capacitor of 3.3 µF with an ESR of 3 Ω or less is recommended to prevent oscillations. Like in general for LDO's the output transient response of the IFX1763 V50 will be a function of the output capacitance. Larger values of output capacitance decrease peak deviations and thus improve transient response for larger load current changes.

1) a good quality low leakage capacitor is recommended.

Bypass capacitors, used to decouple individual components powered by the IFX1763 V50 will increase the effective output capacitor value. Please note that with the usage of larger bypass capacitors for low noise operation either larger values of output capacitors are needed or a minimum ESR requirement of C_{OUT} may have to be considered (see also **Figure "ESR(COUT) with CBYP = 10 nF versus Output Capacitance COUT" on Page 17** as example). In conjunction with the usage of a 10 nF bypass capacitor an output capacitor C_{OUT} ≥ 6.8 µF is recommended. The benefit of a bypass capacitor to the transient response performance is impressive and illustrated as one example in **Figure 6** where the transient response of the IFX1763 V50 to one and the same load step from 100 mA to 500 mA is shown with and without a 10 nF bypass capacitor: for the given configuration of C_{OUT} = 10 µF with no bypass capacitor the load step will settle in the range of less than 200 µs while for C_{OUT} = 10 µF in conjunction with a 10 nF bypass capacitor the same load step will settle in the range of 20 µs. Due to the shorter reaction time of the regulator by adding the bypass capacitor not only the settling time improves but also output voltage deviations due to load steps are sharply reduced.

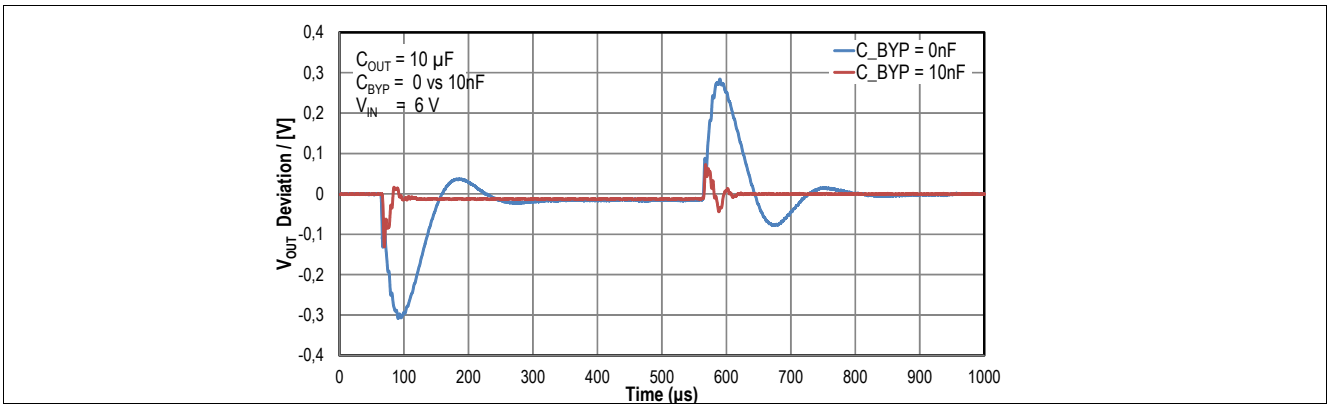


Figure 6 Influence of C_{BYP}: example of transient response to one and the same load step with and without C_{BYP} of 10 nF (I_{OUT} 100 mA to 500 mA)

7.4 Protection Features

The IFX1763 V50 regulators incorporate several protection features which make them ideal for usage in battery-powered circuits. In addition to normal protection features associated with monolithic regulators like current limiting and thermal limiting the device is protected against reverse input voltage, reverse output voltage and reverse voltages from output to input.

Current limit protection and thermal overload protection are intended to protect the device against current overload conditions at the output of the device. For normal operation the junction temperature must not exceed 125°C.

The input of the device will withstand reverse voltages of 20 V. Current flowing into the device will be limited to less than 1 mA (typically less than 100 µA) and no negative voltage will appear at the output. The device will protect both itself and the load. This provides protection against batteries being plugged backwards.

The output of the IFX1763 V50 can be pulled below ground without damaging the device. If the input is left open-circuit or grounded, the output can be pulled below ground by 20 V. Under such conditions the OUT pin by itself will act like an open circuit with practically no current flowing out of the pin[1)]. In more application relevant cases where the output pin OUT is connected to the SENSE pin there will be a small current of typically less than 100 µA present from this origin. If the input is powered by a voltage source the output will source the short-circuit current of the device and will protect itself by thermal limiting. In this case grounding the EN pin will turn off the device and stop the output from sourcing the short-circuit current.

In circuits where a backup battery is required, several different input/output conditions can occur. The output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is left open-circuit. Current flow back into the output will follow the curve as shown in **Figure 7** below.

1) typically < 1 µA for the mentioned conditions, V_{OUT} being pulled below ground with other pins either grounded or open.

When the IN pin of the IFX1763 V50 is forced below the OUT pin, or the OUT pin is pulled above the IN pin, the input current will typically drop to less than 2 µA. This can happen if the input of the device is connected to a discharged battery and the output is held up by either a backup battery or a second regulator circuit. The state of the EN pin will have no effect on the reverse output current when the output is pulled above the input.

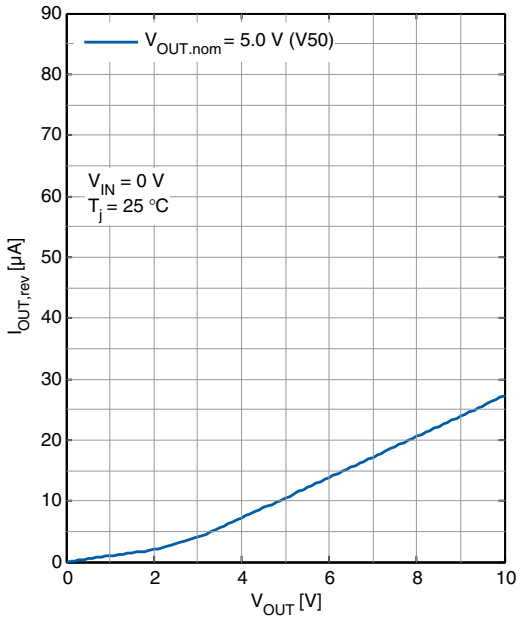


Figure 7 Reverse Output Current

8 Package Outlines

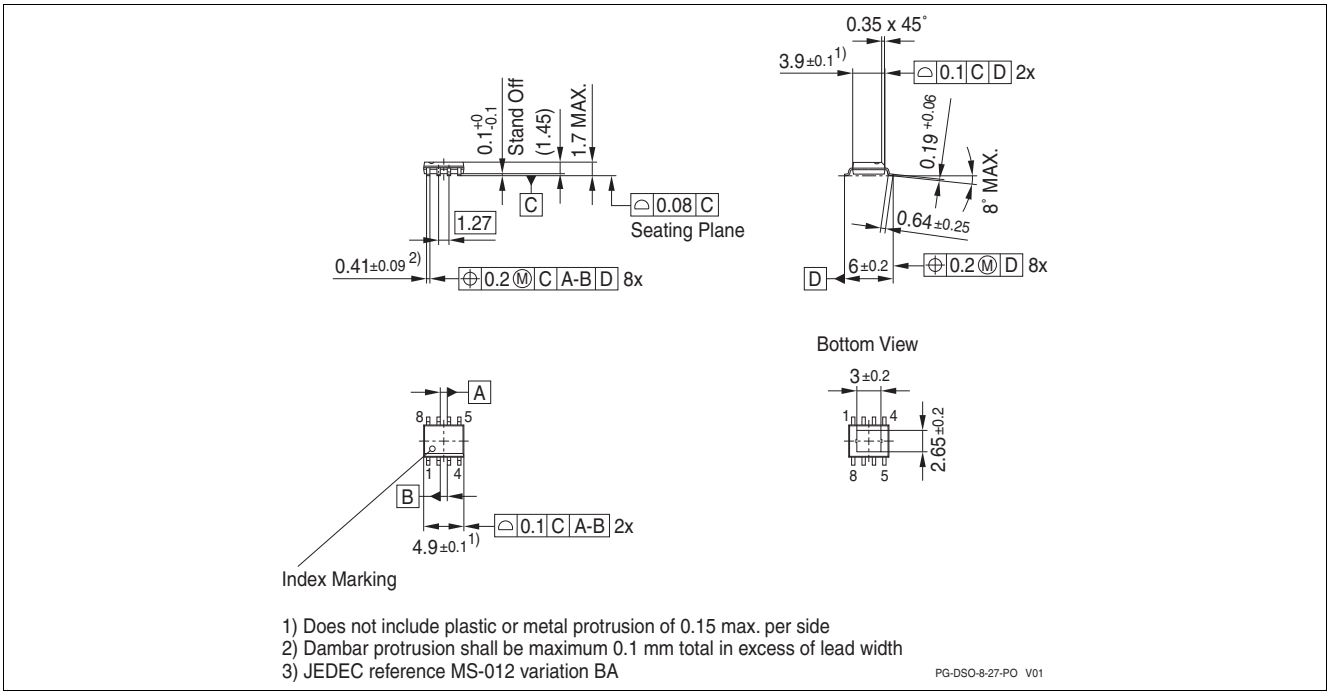


Figure 8 **PG-DSO-8 Exposed Pad** package outlines

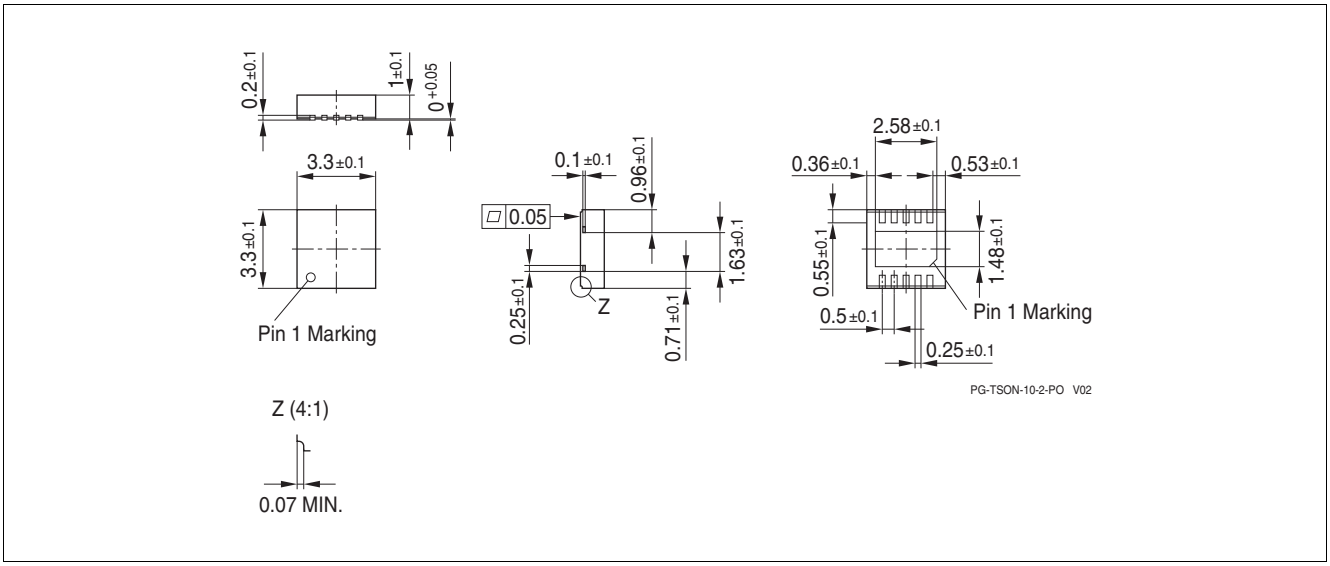


Figure 9 **PG-TSON-10** Package Outlines

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
1.11	2015-01-30	• Editorial changes - figure title of TSON-10 package figure in Product Overview corrected.
1.1	2014-10-30	Updated Data Sheet including additional package type PG-TSON-10: • PG-TSON-10 package variants added: Product Overview, Pin Configuration Thermal Resistance, Wording, etc added / updated accordingly. • Editorial changes throughout the document.
1.0	2014-05-16	Data Sheet - Initial Release

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