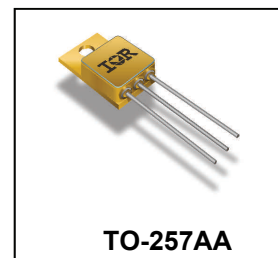


**RADIATION HARDENED  
POWER MOSFET  
THRU-HOLE(TO-257AA)**

**100V, N-CHANNEL**  
**REF: MIL-PRF-19500/614**  
**RAD-Hard HEXFET TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	I <sub>D</sub>	QPL Part Number
IRHY7130CM	100 kRads(Si)	0.18Ω	14.4A	JANSR2N7380
IRHY3130CM	300 kRads(Si)	0.18Ω	14.4A	JANSF2N7380
IRHY5130CM	500 kRads(Si)	0.18Ω	14.4A	JANSG2N7380
IRHY8130CM	1000 kRads(Si)	0.18Ω	14.4A	JANSH2N7380



**Description**

IR HiRel RAD-Hard HEXFET technology provides high performance power MOSFETs for space applications. This technology has over a decade of proven performance and reliability in satellite applications. These devices have been characterized for both Total Dose and Single Event Effects (SEE). The combination of low R<sub>ds(on)</sub> and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching and temperature stability of electrical parameters.

**Features**

- Single Event Effect (SEE) Hardened
- Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Hermetically Sealed
- Ceramic Eyelets
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

**Absolute Maximum Ratings**

**Pre-Irradiation**

Symbol	Parameter	Value	Units
I <sub>D1</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 25°C	Continuous Drain Current	14.4	A
I <sub>D2</sub> @ V <sub>GS</sub> = 12V, T <sub>C</sub> = 100°C	Continuous Drain Current	9.1	
I <sub>DM</sub> @ T <sub>C</sub> = 25°C	Pulsed Drain Current ①	57.6	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	150	mJ
I <sub>AR</sub>	Avalanche Current ①	14.4	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	6.0	V/ns
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in.(1.6mm) from case for 10s)	
	Weight	7.0 (Typical)	

For Footnotes, refer to the page 2.

**Electrical Characteristics @ T<sub>J</sub> = 25°C (Unless Otherwise Specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	0.18	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 9.1A ④
		—	—	0.20		V <sub>GS</sub> = 12V, I <sub>D1</sub> = 14.4A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	—	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
G <sub>fs</sub>	Forward Transconductance	2.5	—	—	S	V <sub>DS</sub> = 15V, I <sub>D2</sub> = 9.1A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	25	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V <sub>GS</sub> = -20V
Q <sub>G</sub>	Total Gate Charge	—	—	40	nC	I <sub>D1</sub> = 14.4A
Q <sub>GS</sub>	Gate-to-Source Charge	—	—	10		V <sub>DS</sub> = 50V
Q <sub>GD</sub>	Gate-to-Drain ('Miller') Charge	—	—	20		V <sub>GS</sub> = 12V
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	25	ns	V <sub>DD</sub> = 50V
t <sub>r</sub>	Rise Time	—	—	60		I <sub>D1</sub> = 14.4A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	40		R <sub>G</sub> = 7.5Ω
t <sub>f</sub>	Fall Time	—	—	30		V <sub>GS</sub> = 12V
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	7.0	—	nH	Measured from drain lead (6mm/0.25in. from package) to source lead (6mm/0.25in. from package)
C <sub>iss</sub>	Input Capacitance	—	960	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	340	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	85	—		f = 1.0MHz

**Source-Drain Diode Ratings and Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	14.4	A	
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	57.6		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.8	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 14.4A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	275	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 14.4A, V <sub>DD</sub> ≤ 50V
Q <sub>rr</sub>	Reverse Recovery Charge	—	—	2.5	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

**Thermal Resistance**

Symbol	Parameter	Min.	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	—	1.67	°C/W
R <sub>θJA</sub>	Junction-to-Ambient	—	—	80	

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② V<sub>DD</sub> = 25V, starting T<sub>J</sub> = 25°C, L = 1.45mH, Peak I<sub>L</sub> = 14.4A, V<sub>GS</sub> = 12V
- ③ I<sub>SD</sub> ≤ 14.4A, di/dt ≤ 395A/μs, V<sub>DD</sub> ≤ 100V, T<sub>J</sub> ≤ 150°C
- ④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%
- ⑤ Total Dose Irradiation with V<sub>GS</sub> Bias. 12 volt V<sub>GS</sub> applied and V<sub>DS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.
- ⑥ Total Dose Irradiation with V<sub>DS</sub> Bias. 80 volt V<sub>DS</sub> applied and V<sub>GS</sub> = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

**Radiation Characteristics**

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR HiRel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

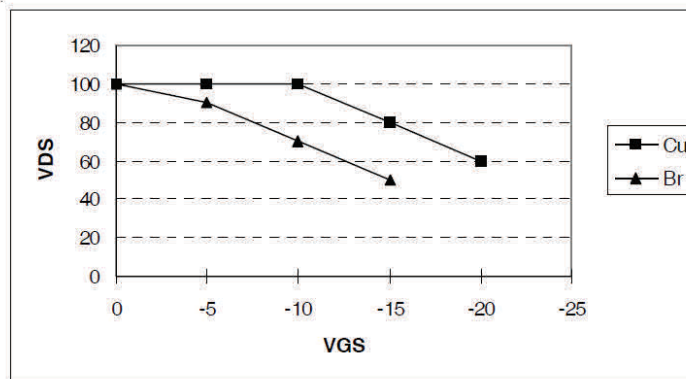
Symbol	Parameter	100 kRads (Si) <sup>1</sup>		Up to 300 k - 1000 kRads (Si) <sup>2</sup>		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	100	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	4.0	1.25	4.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	100	—	100	nA	V <sub>GS</sub> = 20V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	-100	—	-100	nA	V <sub>GS</sub> = -20V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	25	—	50	μA	V <sub>DS</sub> = 80V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.18	—	0.24	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 9.1A
R <sub>DS(on)</sub>	Static Drain-to-Source ④ On-State Resistance (TO-257AA)	—	0.18	—	0.24	Ω	V <sub>GS</sub> = 12V, I <sub>D2</sub> = 9.1A
V <sub>SD</sub>	Diode Forward Voltage ④	—	1.8	—	1.8	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 14.4A

1. Part number IRHY7130CM (JANSR2N7380)
2. Part numbers IRHY3130CM (JANSF2N7380), IRHY5130CM (JANSR2N7380), IRHY8130CM (JANSH2N7380)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

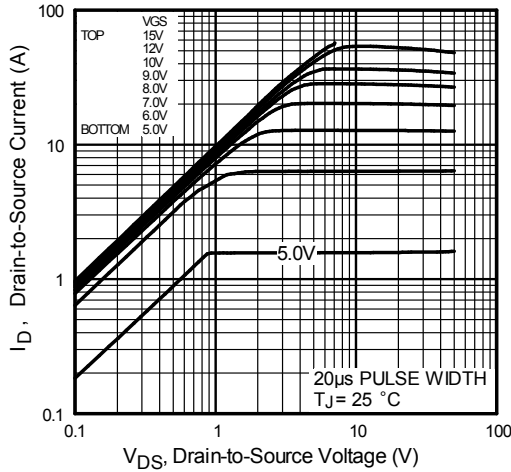
**Table 2. Typical Single Event Effect Safe Operating Area**

Ion	LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)				
				@VGS = 0V	@VGS = -5V	@VGS = -10V	@VGS = -15V	@VGS = -20V
Cu	28	285	43	100	100	100	80	60
Br	36.8	305	39	100	90	70	50	-

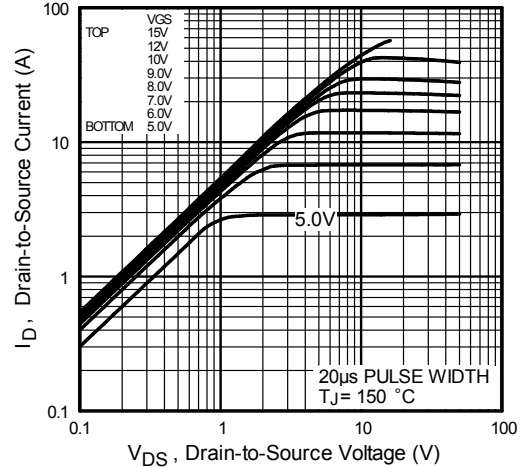


**Fig a.** Typical Single Event Effect, Safe Operating Area

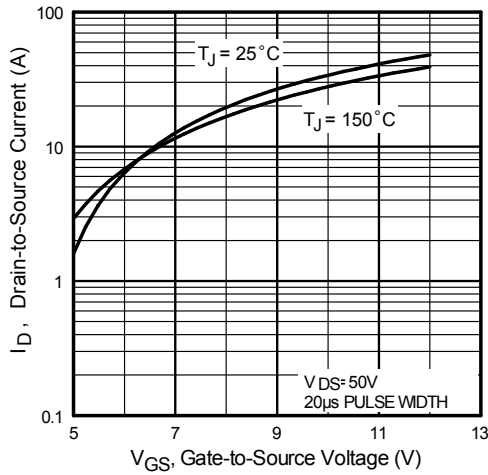
For Footnotes, refer to the page 2.



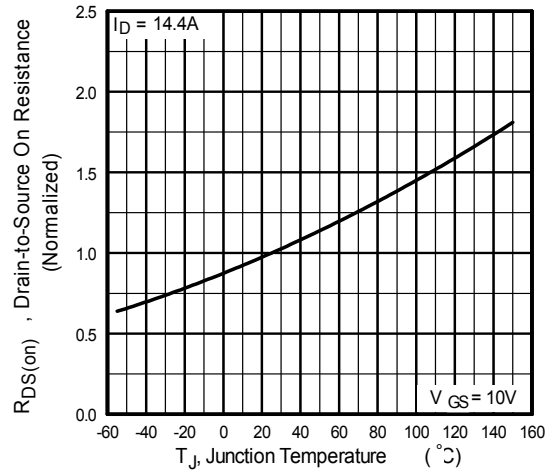
**Fig 1.** Typical Output Characteristics



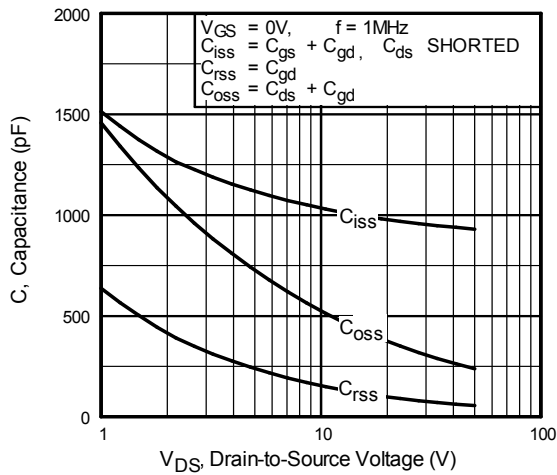
**Fig 2.** Typical Output Characteristics



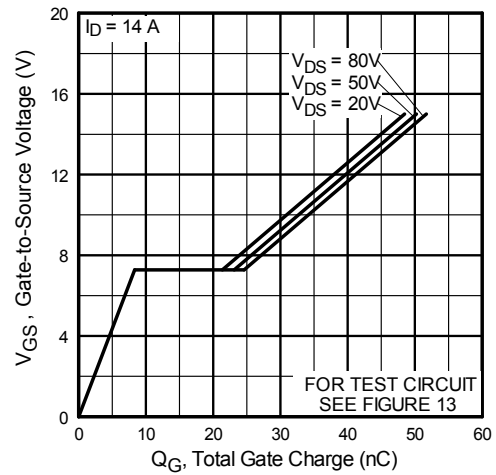
**Fig 3.** Typical Transfer Characteristics



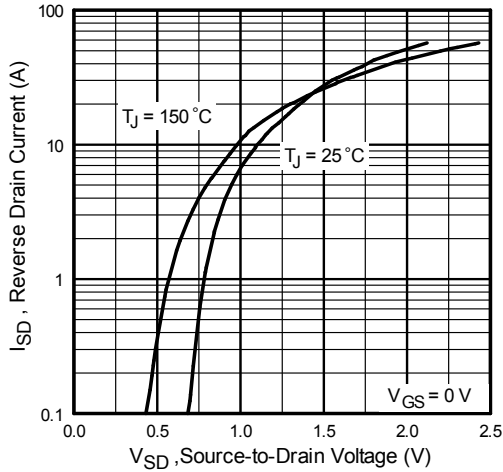
**Fig 4.** Normalized On-Resistance Vs. Temperature



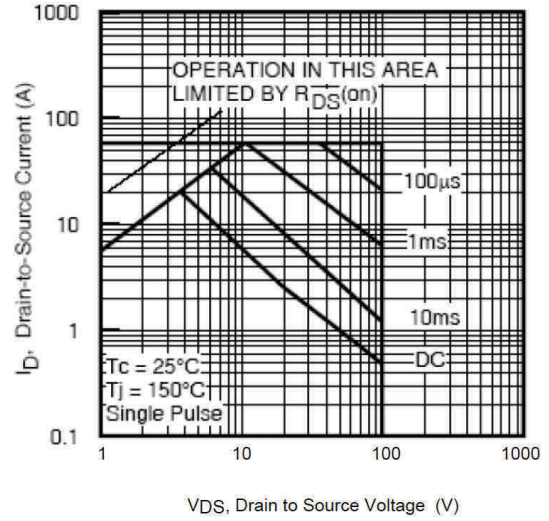
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



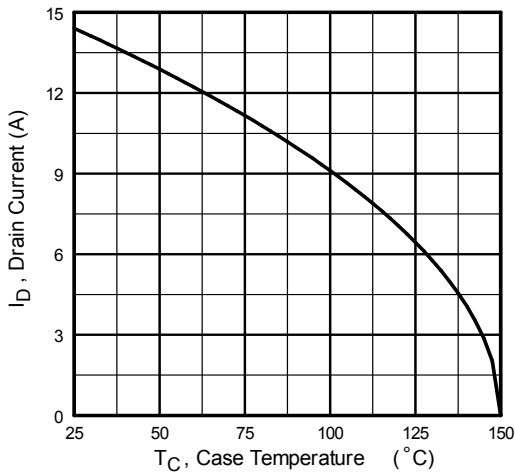
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



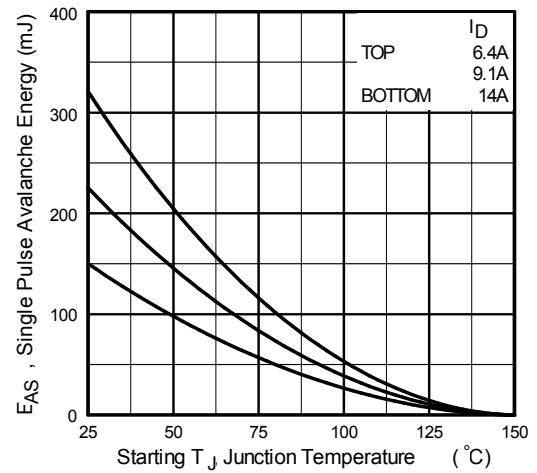
**Fig 7.** Typical Source-Drain Diode Forward Voltage



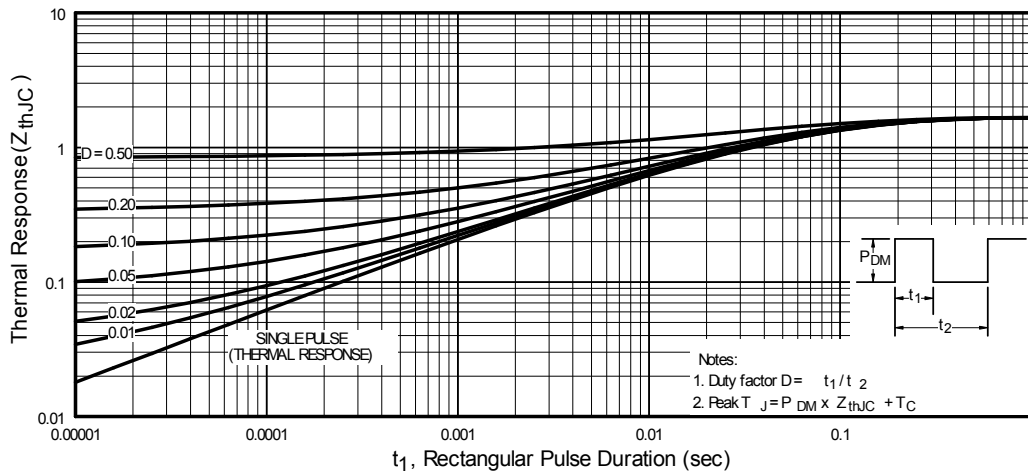
**Fig 8.** Maximum Safe Operating Area



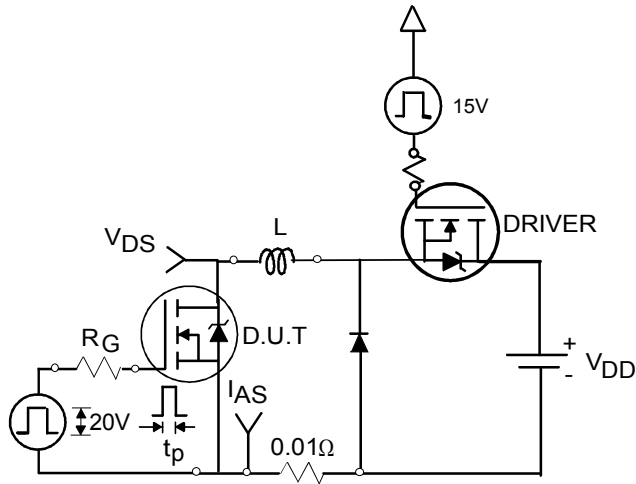
**Fig 9.** Maximum Drain Current Vs. Case Temperature



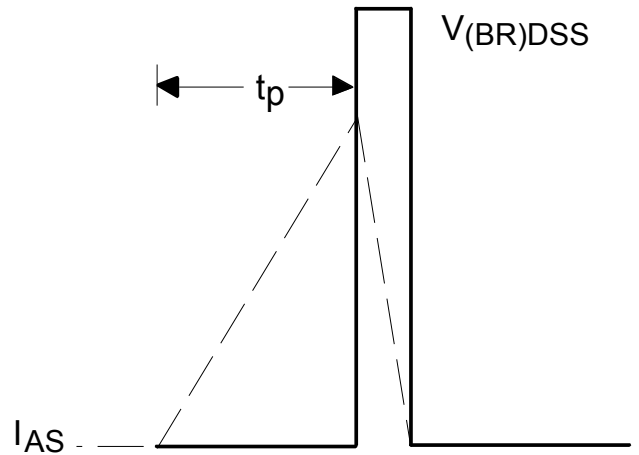
**Fig 10.** Maximum Avalanche Energy Vs. Drain Current



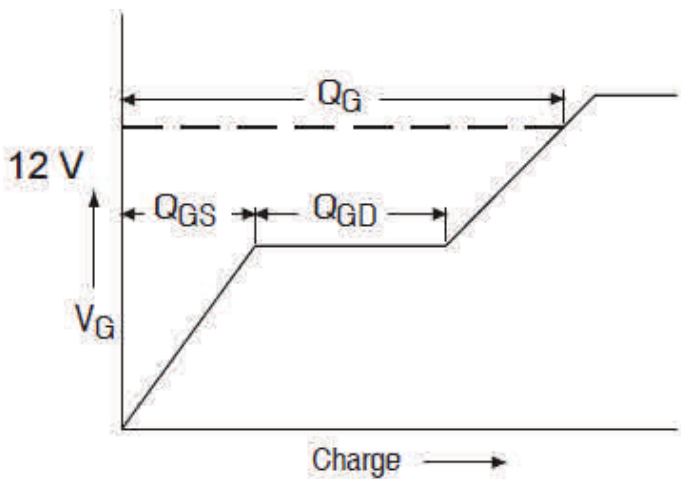
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case



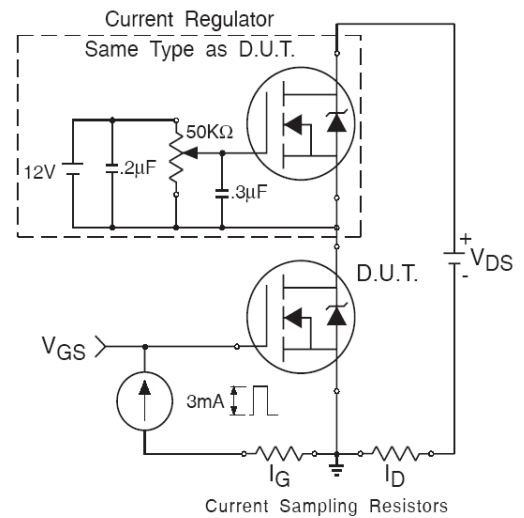
**Fig 12a.** Unclamped Inductive Test Circuit



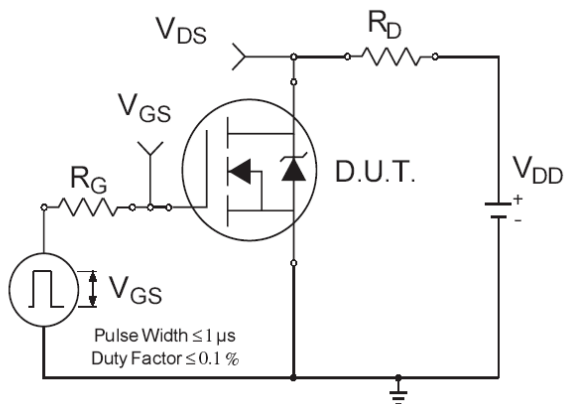
**Fig 12b.** Unclamped Inductive Waveforms



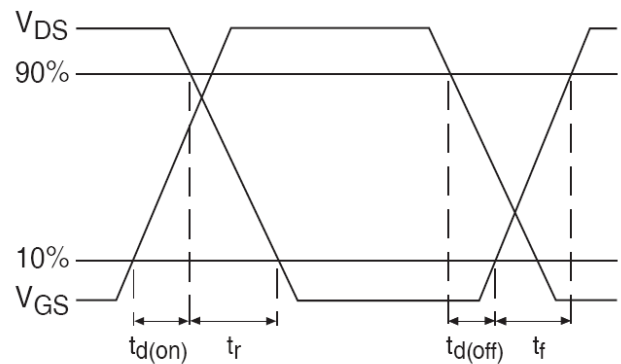
**Fig 13a.** Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

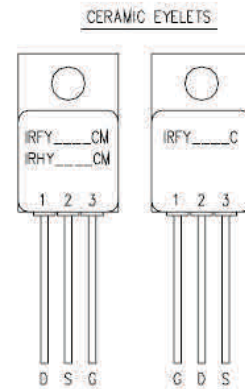
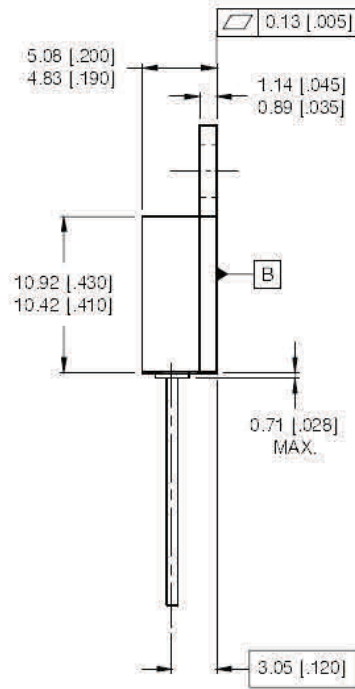
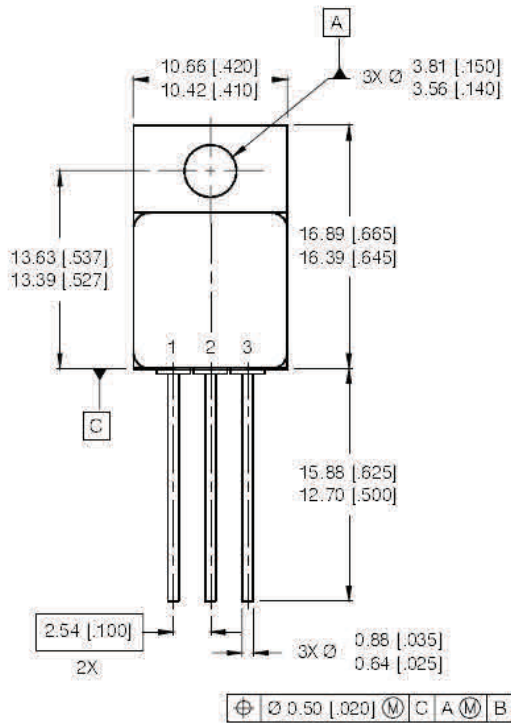


**Fig 14a.** Switching Time Test Circuit



**Fig 14b.** Switching Time Waveforms

**Case Outline and Dimensions — TO-257AA**



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

**PIN ASSIGNMENTS**

- 1 = DRAIN
- 2 = SOURCE
- 3 = GATE

### **IMPORTANT NOTICE**

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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