

IGBT

TRENCHSTOP™ IGBT3 Chip  
SIGC15T60E

Data Sheet

Industrial Power Control



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## TRENCHSTOP™ IGBT3 Chip

### Features:

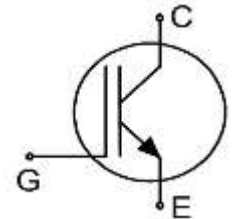
- 600V trench & field stop technology
- Low  $V_{CEsat}$
- Low turn-off losses
- Short tail current
- Positive temperature coefficient
- Easy paralleling

### Recommended for:

- Power modules
- Discrete components

### Applications:

- Drives
- White goods
- Resonant applications



Chip Type	$V_{CE}$	$I_{Cn}$	Die Size	Package
SIGC15T60E	600V	30A	3.92mm x 3.88mm	Sawn on foil

### Mechanical Parameters

Die size	3.92 x 3.88	mm <sup>2</sup>
Emitter pad size	See chip drawing	
Gate pad size	0.61 x 1.08	
Area total	15.21	
Silicon thickness	70	μm
Wafer size	200	mm
Maximum possible chips per wafer	1806	
Passivation frontside	Photoimide	
Pad metal	3200nm AlSiCu	
Backside metal	Ni Ag – system To achieve a reliable solder connection it is strongly recommended not to consume the Ni layer completely during production process	
Die bond	Electrically conductive epoxy glue and soft solder	
Wire bond	Al, ≤500μm	
Reject ink dot size	∅ 0.65mm; max. 1.2mm	
Storage environment (<6 months)	for original and sealed MBB bags	Ambient atmosphere air, temperature 17°C – 25°C
	for open MBB bags	Acc. IEC 62258-3; Section 9.4 Storage Environment.

## Maximum Ratings

In general, from reliability and lifetime point of view, the lower the operation junction temperature and/or the applied voltage, the greater the expected lifetime of any semiconductor device.

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_{vj}=25^{\circ}\text{C}$	$V_{CE}$	600	V
DC collector current, limited by $T_{vj\text{ max}}^1$	$I_C$	-	A
Pulsed collector current, $t_p$ limited by $T_{vj\text{ max}}^2$	$I_{C,puls}$	90	A
Gate-emitter voltage	$V_{GE}$	$\pm 20$	V
Virtual junction temperature	$T_{vj}$	-40 ... +175	$^{\circ}\text{C}$
Short circuit data <sup>1/2/3</sup> $V_{GE}=15\text{V}$ , $V_{CC}=360\text{V}$ , $T_{vj}=150^{\circ}\text{C}$	$t_{sc}$	6	$\mu\text{s}$
Reverse bias safe operating area (RBSOA) <sup>2</sup>	$I_{C,max} = 60\text{A}$ , $V_{CE,max} = 600\text{V}$ , $T_{vj} \leq 150^{\circ}\text{C}$		

## Static Characteristics (tested on wafer), $T_{vj}=25^{\circ}\text{C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0\text{V}$ , $I_C=2\text{mA}$	600	-	-	V
Collector-emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15\text{V}$ , $I_C=30\text{A}$	1.1	1.5	1.9	
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C=430\mu\text{A}$ , $V_{GE}=V_{CE}$	5.0	5.8	6.5	
Zero gate voltage collector current	$I_{CES}$	$V_{CE}=600\text{V}$ , $V_{GE}=0\text{V}$	-	-	1.6	$\mu\text{A}$
Gate-emitter leakage current	$I_{GES}$	$V_{CE}=0\text{V}$ , $V_{GE}=20\text{V}$	-	-	300	nA
Integrated gate resistor	$r_G$		none			$\Omega$

## Electrical Characteristics <sup>2</sup>

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	$C_{ies}$	$V_{CE}=25\text{V}$ , $V_{GE}=0\text{V}$ , $f=1\text{MHz}$ $T_{vj}=25^{\circ}\text{C}$	-	1630	-	pF
Output capacitance	$C_{oes}$		-	108	-	
Reverse transfer capacitance	$C_{res}$		-	50	-	

<sup>1</sup> Depending on thermal properties of assembly.

<sup>2</sup> Not subject to production test - verified by design/characterization.

<sup>3</sup> Allowed number of short circuits: <1000; time between short circuits: >1s.



# SIGC15T60E

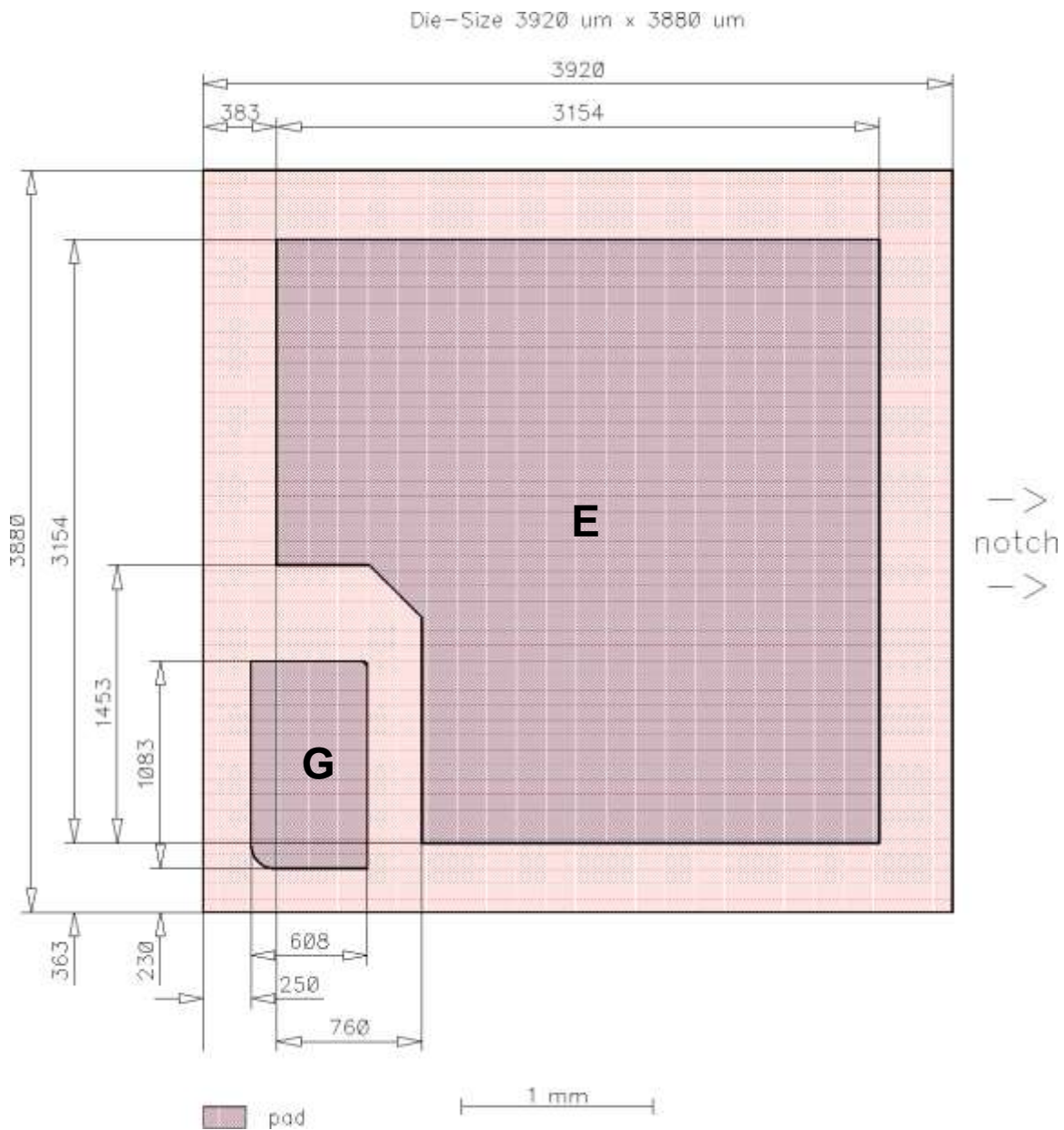
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## Further Electrical Characteristics

Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

Application example	-	-
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## Chip Drawing



**E** = Emitter

**G** = Gate



# SIGC15T60E

## Bare Die Product Specifics

Test coverage at wafer level cannot cover all application conditions. Therefore it is recommended to test all characteristics which are relevant for the application at package level, including RBSOA and SCSOA.

## Description

AQL 0.65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

## Revision History

Revision	Subjects (major changes since last revision)	Date
2.1	Wafer diameter changed to 200 mm	06.07.2010
2.2	Additional Basic Type, editorial changes, maximum possible chips per wafer corrected	19.07.2017

## Relevant Application Notes

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