IRHY57130CM
JANSR2N7484T3

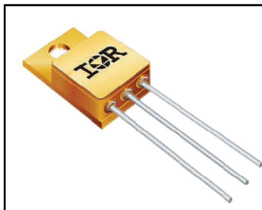
An Infineon Technologies Company

RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-257AA)

100V, N-CHANNEL
REF: MIL-PRF-19500/702
R5 TECHNOLOGY

Product Summary

Part Number	Radiation Level	RDS(on)	I_D	QPL Part Number
IRHY57130CM	100 kRads(Si)	0.07Ω	18A*	JANSR2N7484T3
IRHY53130CM	300 kRads(Si)	0.07Ω	18A*	JANSF2N7484T3
IRHY55130CM	500 kRads(Si)	0.07Ω	18A*	JANSG2N7484T3
IRHY58130CM	1000 kRads(Si)	0.085Ω	18A*	JANSH2N7484T3



TO-257AA

Description

IRHY57130CM is part of the International Rectifier HiRel family of products. IR HiRel R5 technology provides high performance power MOSFETs for space applications. These devices have been characterized for both Total Dose and Single Event Effect (SEE) with useful performance up to LET of 80 (MeV/(mg/cm^2)). The combination of low RDS(on) and low gate charge reduces the power losses in switching applications such as DC-DC converters and motor controllers. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features

- Single Event Effect (SEE) Hardened
- Ultra Low RDS(on)
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Electrically Isolated
- Ceramic Eyelets
- Light Weight
- ESD Rating: Class 1C per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	18*	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	14	
I_{DM}	Pulsed Drain Current ①	72	
P_D @T_C = 25°C	Maximum Power Dissipation	75	W
	Linear Derating Factor	0.6	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy ②	87	mJ
I_{AR}	Avalanche Current ①	18	A
E_{AR}	Repetitive Avalanche Energy ①	7.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	1.4	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	4.3 (Typical)	g

* Current is limited by package

For Footnotes, refer to the page 2.

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.11	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.07	Ω	V_{GS} = 12V, I_D = 14A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
Gfs	Forward Transconductance	13	—	—	S	V_{DS} = 15V, I_D = 14A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS} = 80V, V_{GS} = 0V
		—	—	25		V_{DS} = 80V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_G	Total Gate Charge	—	—	50	nC	I_D = 18A
Q_{GS}	Gate-to-Source Charge	—	—	7.4		V_{DS} = 50V
Q_{GD}	Gate-to-Drain ('Miller') Charge	—	—	20		V_{GS} = 12V
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 50V
tr	Rise Time	—	—	100		I_D = 18A
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		R_G = 7.5Ω
t_f	Fall Time	—	—	30		V_{GS} = 12V
Ls + L_D	Total Inductance	—	6.8		nH	Measured from Drain lead (6mm /0.25in from package) to Source lead (6mm/0.25in from package) with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	1005	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	365	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	50	—		f = 1.0MHz

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	18*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	72		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_J = 25°C, I_S = 18A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	250	ns	T_J = 25°C, I_F = 18A, V_{DD} ≤ 25V
Q_{rr}	Reverse Recovery Charge	—	—	850	nC	di/dt = 100A/µs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	1.67	°C/W
$R_{\theta JA}$	Junction-to-Ambient (Typical socket mount)	—	—	80	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L = 0.53mH, Peak I_L = 18A, V_{GS} = 12V

③ I_{SD} ≤ 18A, di/dt ≤ 155A/µs, V_{DD} ≤ 100V, T_J ≤ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 80 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel radiation hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at IR Hirel is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 500 kRads (Si)[1]		1000 kRads (Si)[2]		Units	Test Conditions
		Min.	Max.	Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	——	100	——	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.0	1.5	4.0	V	V_{DS} = V_{GS}, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	——	100	——	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	——	-100	——	-100	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	——	10	——	25	µA	V_{DS} = 80V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State ④ Resistance (TO-3)	——	0.07	——	0.085	Ω	V_{GS} = 12V, I_D = 14A
$R_{DS(on)}$	Static Drain-to-Source On-State ④ Resistance (TO-257AA)	——	0.07	——	0.085	Ω	V_{GS} = 12V, I_D = 14A
V_{SD}	Diode Forward Voltage ④	——	1.2	——	1.2	V	V_{GS} = 0V, I_D = 18A

1. Part numbers IRHY57130CM (JANSR2N7484T3), IRHY53130CM (JANSF2N7484T3) and IRHY55130CM (JANSG2N7484T3)
2. Part number IRHY58130CM (JANSH2N7484T3)

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm^2))	Energy (MeV)	Range (µm)	VDS (V)				
			@ VGS = 0V	@ VGS=-5V	@ VGS=-10V	@ VGS =-15V	@ VGS=-20V
38 ± 5%	300 ± 7.5%	38 ± 7.5%	100	100	100	100	100
61 ± 5%	330 ± 7.5%	31 ± 10%	100	100	100	35	25
84 ± 5%	350 ± 7.5%	28 ± 7.5%	100	100	80	25	——

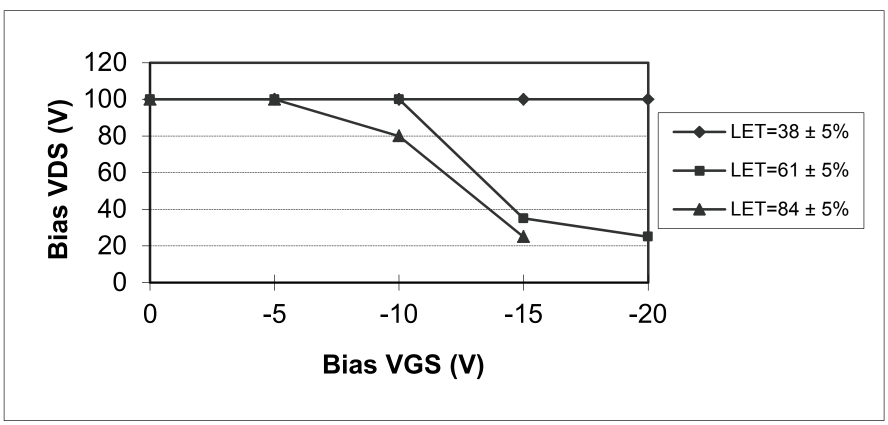


Fig a. Typical Single Event Effect, Safe Operating Area

For Footnotes, refer to the page 2.

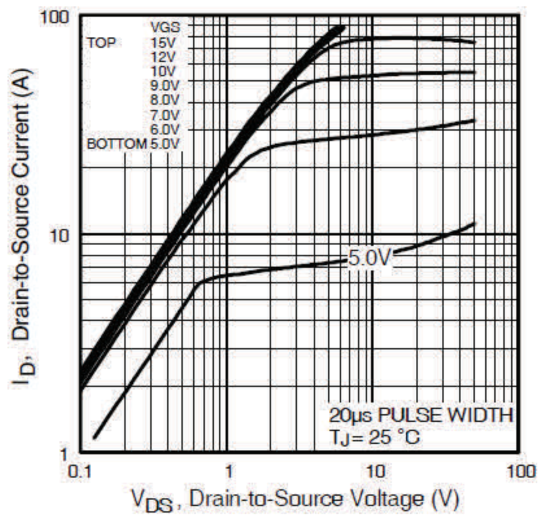


Fig 1. Typical Output Characteristics

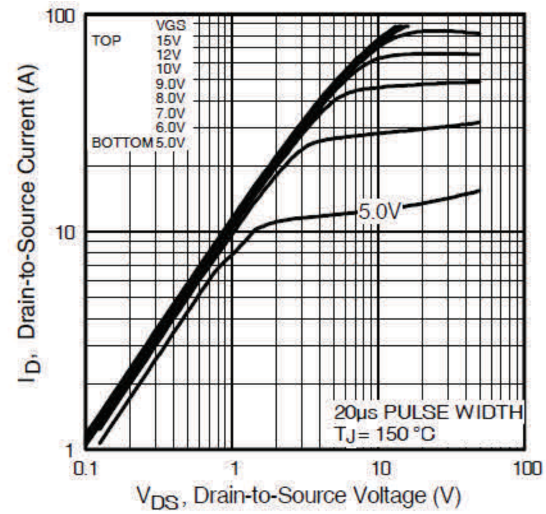


Fig 2. Typical Output Characteristics

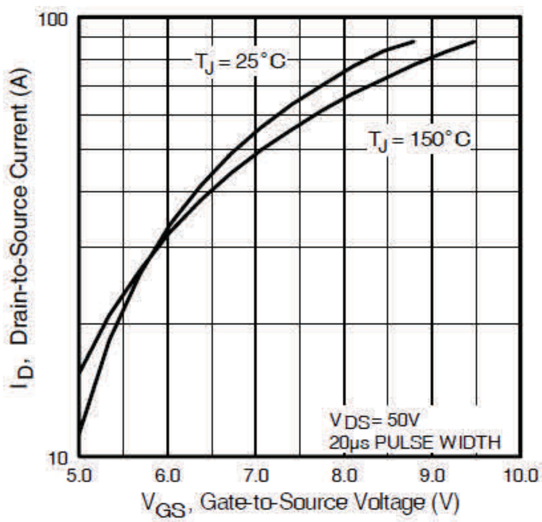


Fig 3. Typical Transfer Characteristics

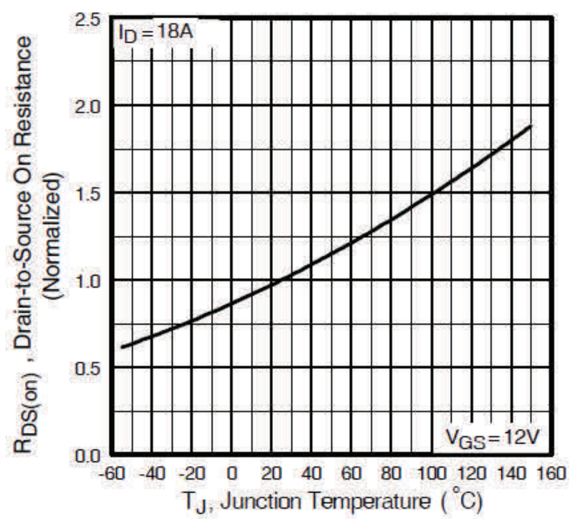


Fig 4. Normalized On-Resistance Vs. Temperature

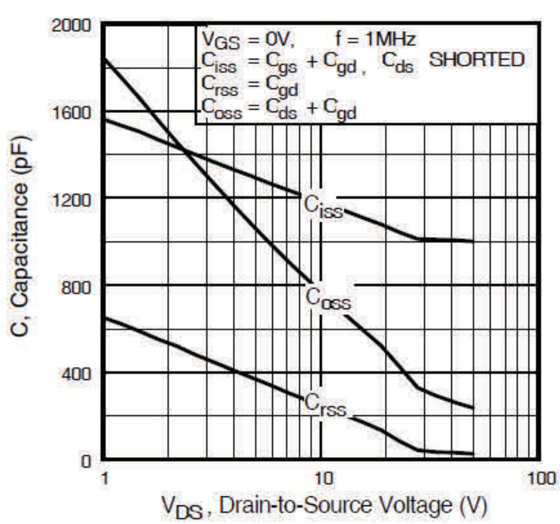


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

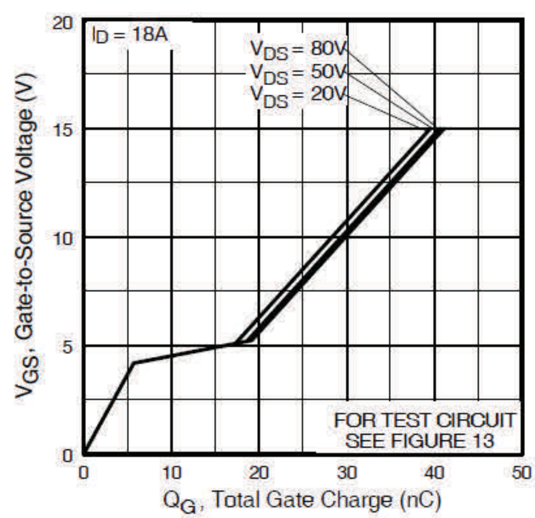


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

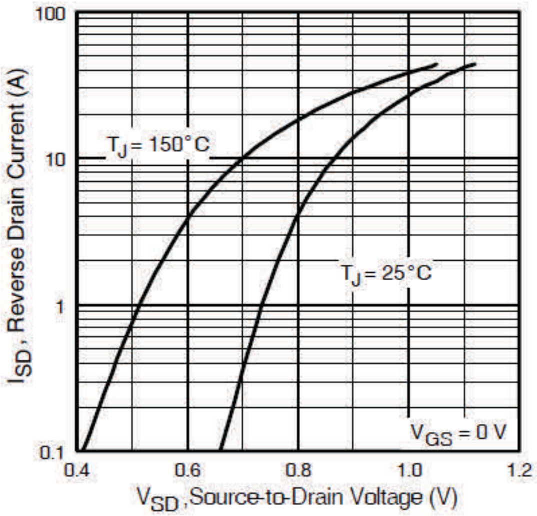


Fig 7. Typical Source-Drain Diode Forward Voltage

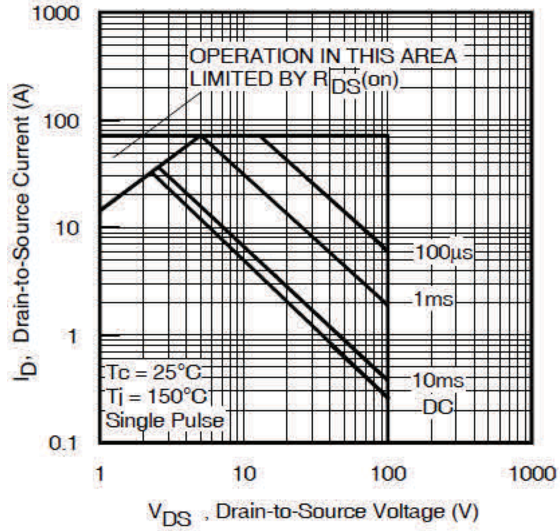


Fig 8. Maximum Safe Operating Area

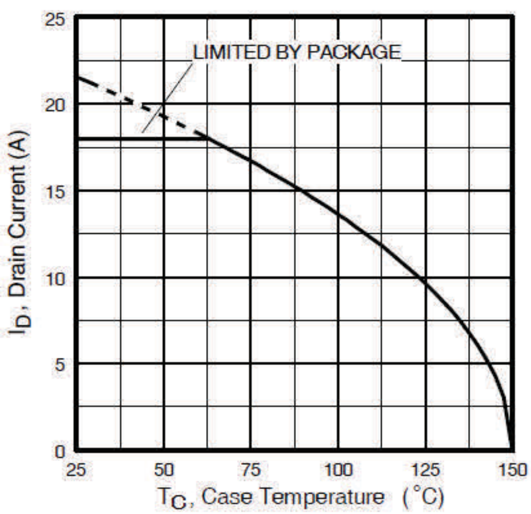


Fig 9. Maximum Drain Current Vs. Case Temperature

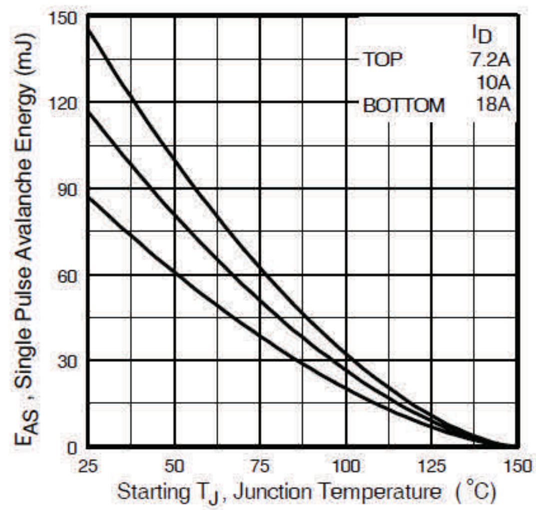


Fig 10. Maximum Avalanche Energy Vs. Drain Current

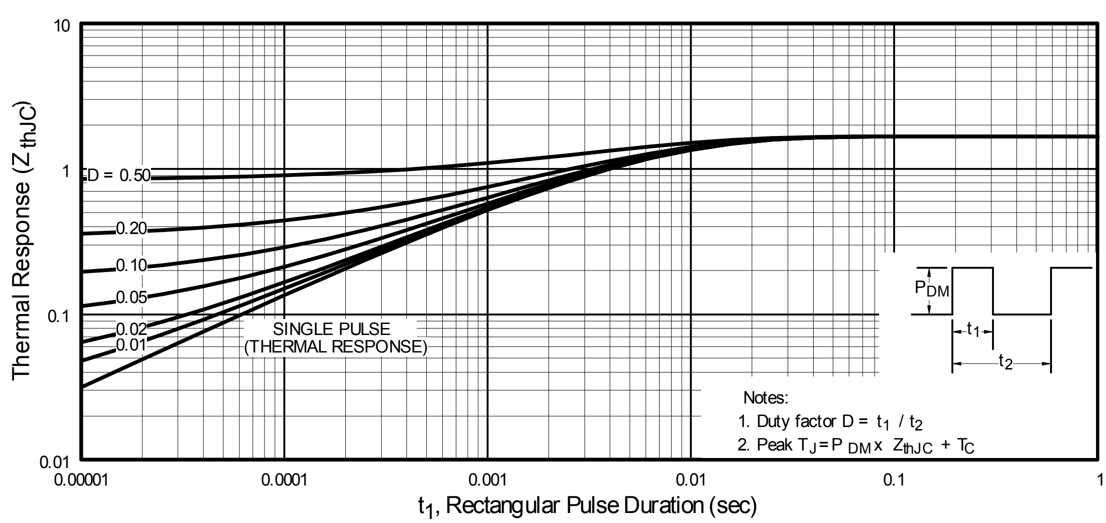


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

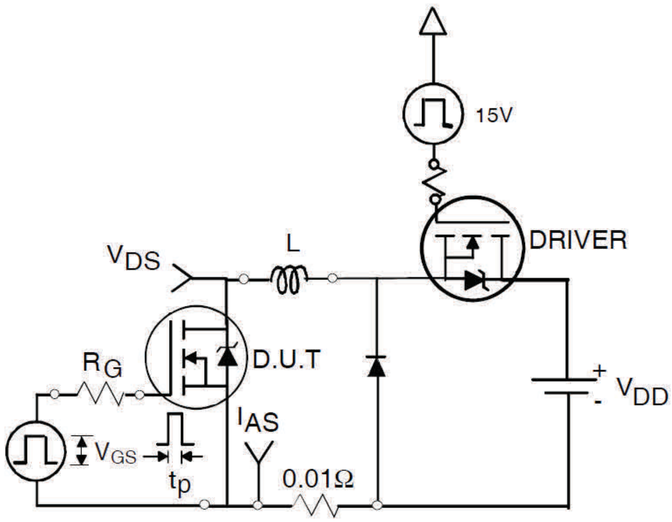


Fig 12a. Unclamped Inductive Test Circuit

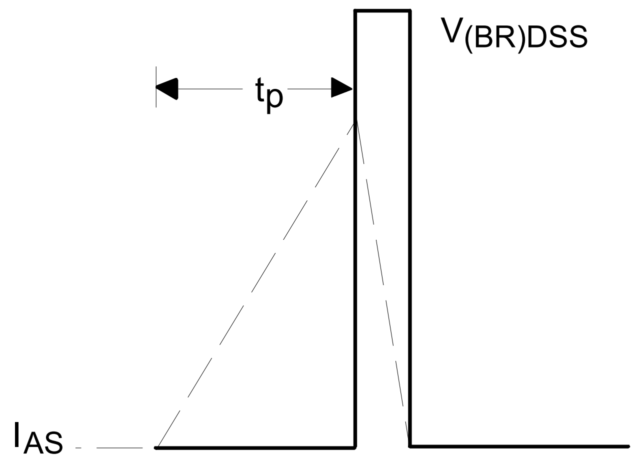


Fig 12b. Unclamped Inductive Waveforms

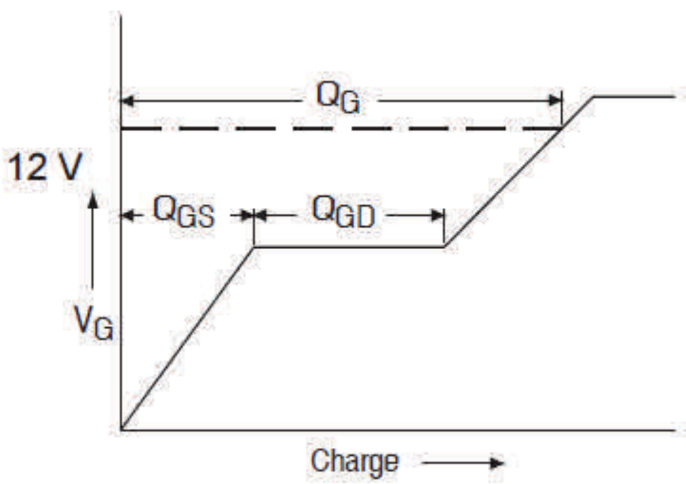


Fig 13a. Gate Charge Waveform

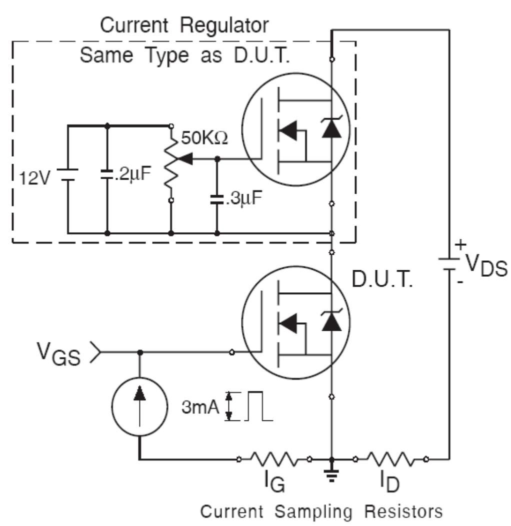


Fig 13b. Gate Charge Test Circuit

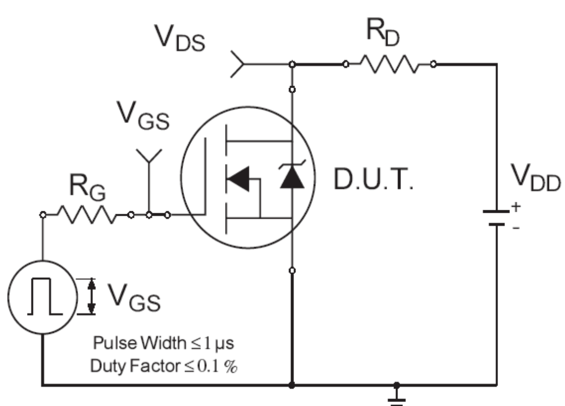


Fig 14a. Switching Time Test Circuit

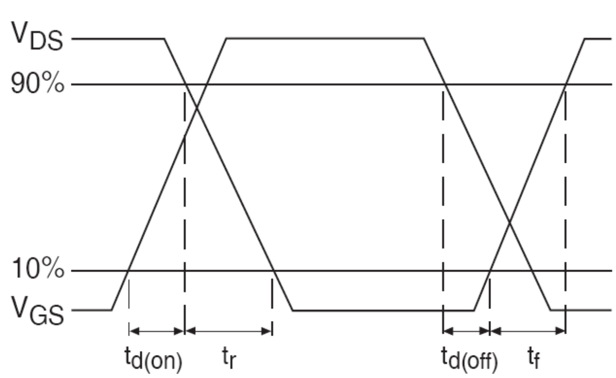
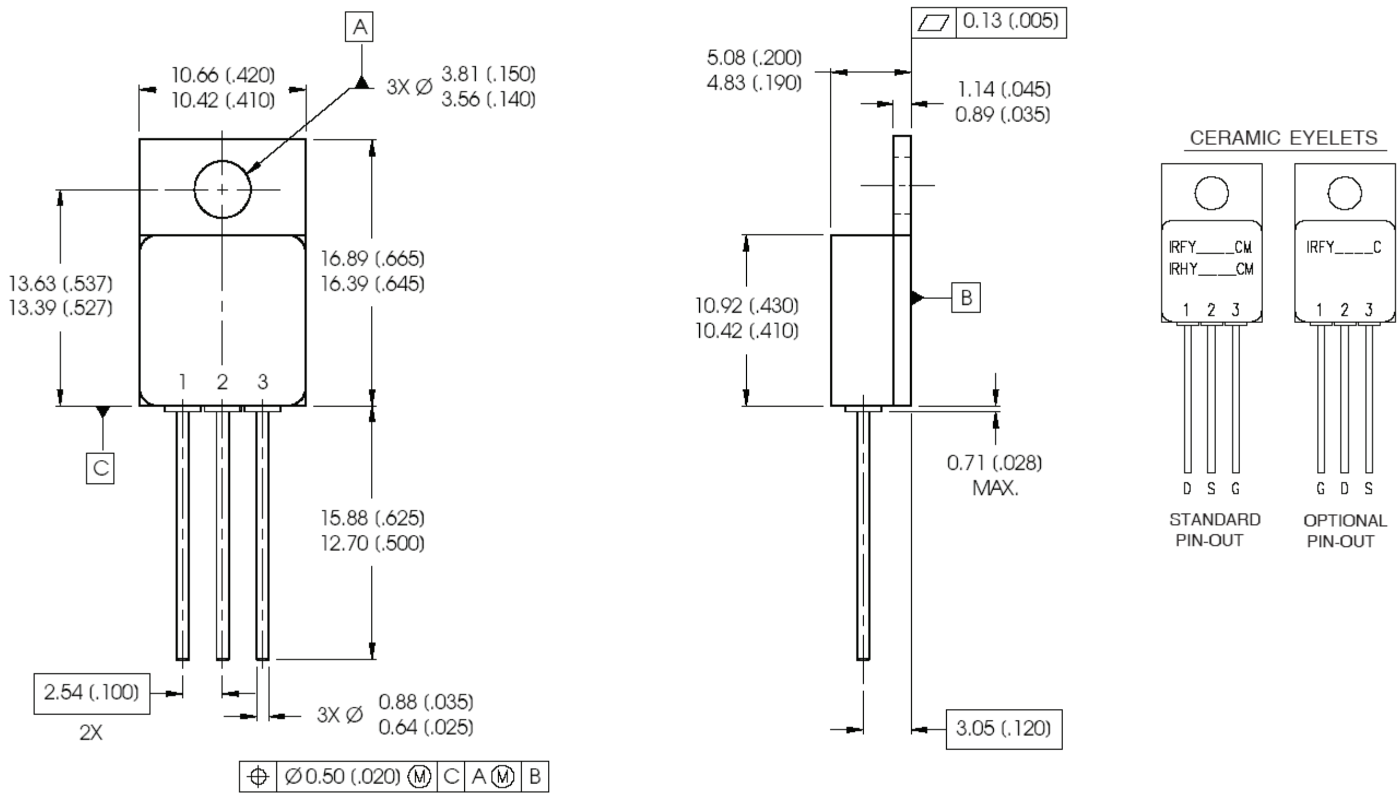


Fig 14b. Switching Time Waveforms

Case Outline and Dimensions — TO-257AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-257AA.

PIN ASSIGNMENTS

1 = DRAIN
2 = SOURCE
3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

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