

ESD233-B1-W0201

Protection Devices

TVS (Transient Voltage Suppressor)

Bi-directional, 5.5 V, 33 pF, 0201, RoHS and Halogen Free compliant

Features

- ESD / transient protection according to:
 - IEC61000-4-2 (ESD): ± 20 kV (air / contact discharge)
 - IEC61000-4-4 (EFT): ± 2 kV / ± 40 A (5/50 ns)
 - IEC61000-4-5 (surge): ± 5 A (8/20 μ s)
- Bi-directional working voltage up to: $V_{RWM} = \pm 5.5$ V
- Line capacitance: $C_L = 33$ pF (typical) at $f = 1$ MHz
- Clamping voltage: $V_{CL} = 13$ V (typical) at $I_{TLP} = 16$ A with $R_{DYN} = 0.20$ Ω (typical)
- Very low reverse current: $I_R < 1$ nA (typical)
- Small form factor SMD Size 0201 and low profile (0.58 mm x 0.28 mm x 0.15 mm)
- Bidirectional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package



Guidelines for optimized PCB design and assembly process are available in [\[2\]](#)

Applications

- ESD Protection of highly susceptible IC/ASICs in audio, headset, human digital interfaces

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

Device information

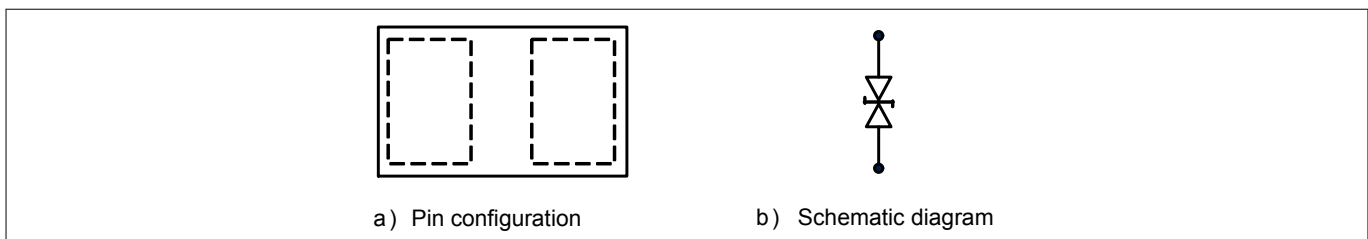


Figure 1 Pin configuration and schematic diagram

Table 1 Part information

Type	Package	Configuration	Marking code
ESD233-B1-W0201	WLL-2-1	1 line, bi-directional	WA ¹⁾

¹⁾ The device does not have any marking or date code on the device backside. The Marking code is on pad side.

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Maximum ratings

1 Maximum ratings

Note: $T_A = 25\text{ °C}$, unless otherwise specified ¹⁾

Table 2 Maximum ratings

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	±5.5	V
ESD discharge ²⁾	V_{ESD} (contact)	±20	kV
	V_{ESD} (air)	±20	
Peak pulse power ³⁾	P_{PK}	70	W
Peak pulse current ³⁾	I_{PP}	±5	A
Operating temperature range	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings. Exceeding only one of these values may cause irreversible damage to the component.

¹ Device is electrically symmetrical

² V_{ESD} according to IEC61000-4-2 (R = 330 Ω, C = 150 pF discharge network)

³ Stress pulse: 8/20µs current waveform according to IEC61000-4-5

Electrical characteristics

2 Electrical characteristics

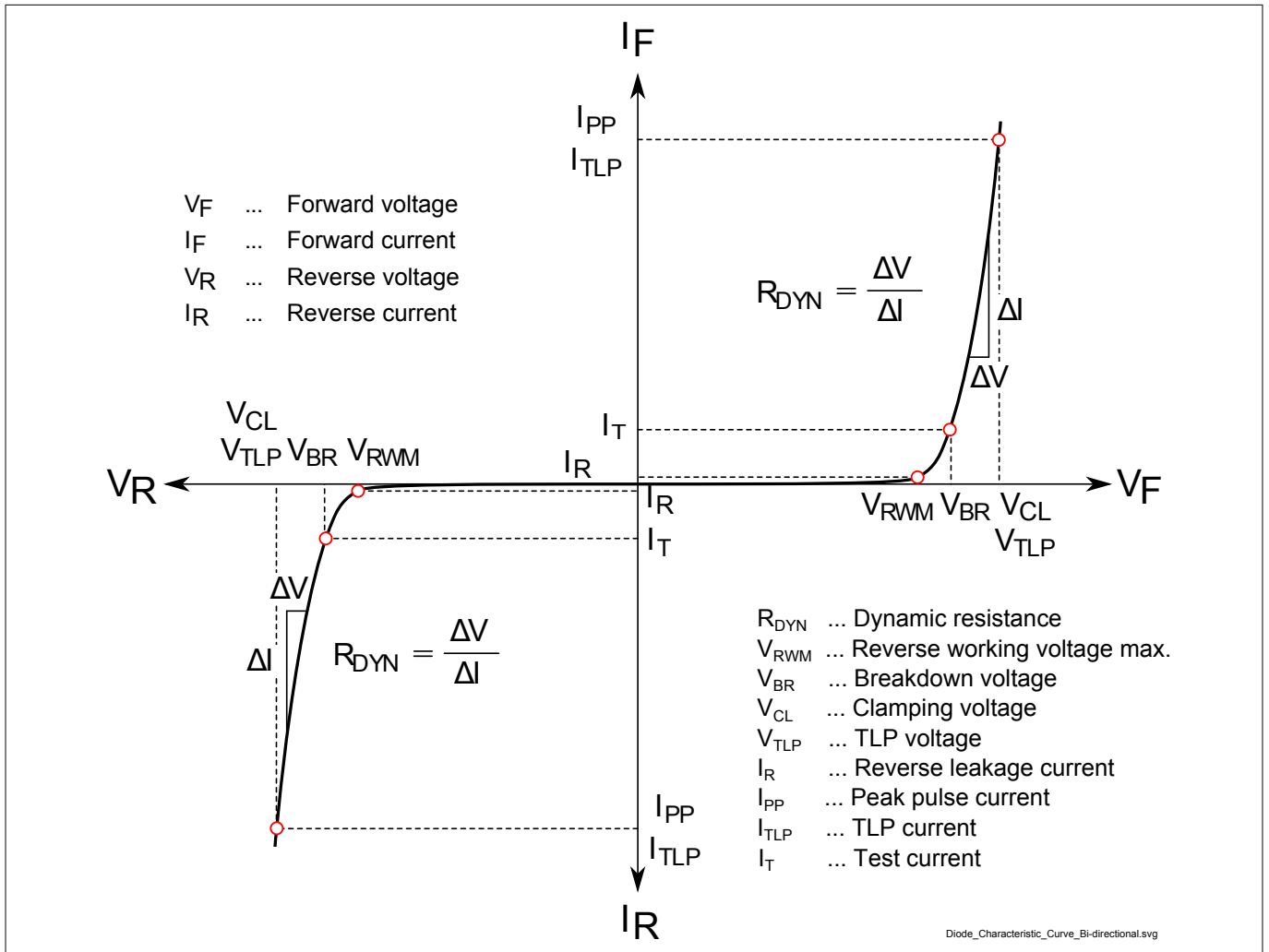


Figure 2 Definitions of electrical characteristics

Electrical characteristics

Table 3 DC characteristics ($T_A = 25\text{ °C}$, unless otherwise specified) ¹⁾

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Breakdown voltage	V_{BR}	7.5	–	9.7	V	$I_T = 1\text{ mA}$
Reverse leakage current	I_R	–	<1	100	nA	$V_R = 5.5\text{ V}$

Table 4 AC characteristics ($T_A = 25\text{ °C}$, unless otherwise specified)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	26	33	40	pF	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$ ²⁾
		–	33	–		$V_R = 0\text{ V}$, $f = 1\text{ GHz}$

Table 5 ESD and Surge characteristics ($T_A = 25\text{ °C}$, unless otherwise specified) ¹⁾

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Clamping voltage ³⁾	V_{CL}	–	10	–	V	$I_{TLP} = 1\text{ A}$, $t_p = 100\text{ ns}$
		–	13	–		$I_{TLP} = 16\text{ A}$, $t_p = 100\text{ ns}$
Clamping voltage ⁴⁾		–	10	–		$I_{PP} = 1\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$
		–	10.5	–		$I_{PP} = 3\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$
		–	11.5	–		$I_{PP} = 5\text{ A}$, $t_p = 8/20\text{ }\mu\text{s}$
Dynamic resistance ³⁾	R_{DYN}	–	0.20		Ω	$t_p = 100\text{ ns}$

¹⁾ Device is electrically symmetrical

²⁾ Verified by design

³⁾ Please refer to Application Note AN210 [1]. TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$.

⁴⁾ Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Typical characteristic diagrams

3 Typical characteristic diagrams

Note: $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

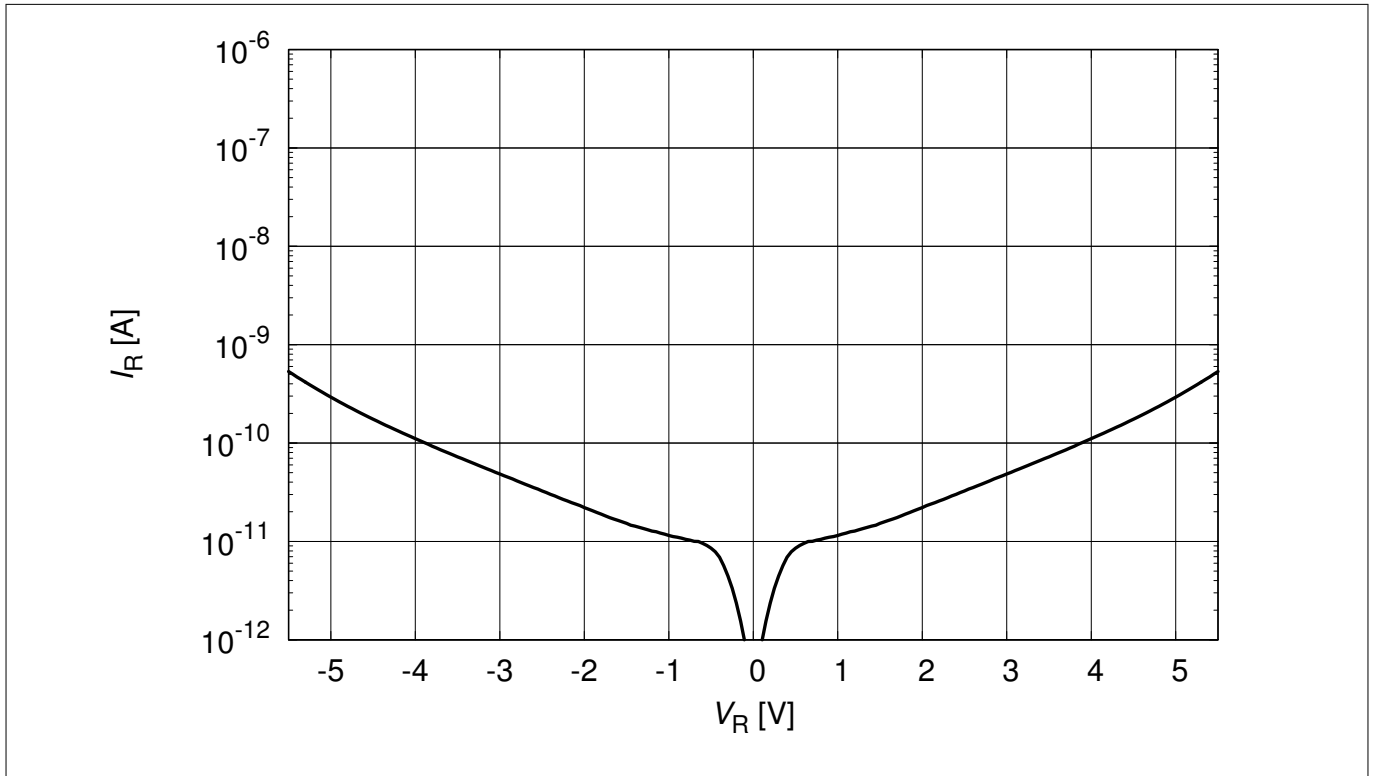


Figure 3 Reverse leakage current: $I_R = f(V_R)$

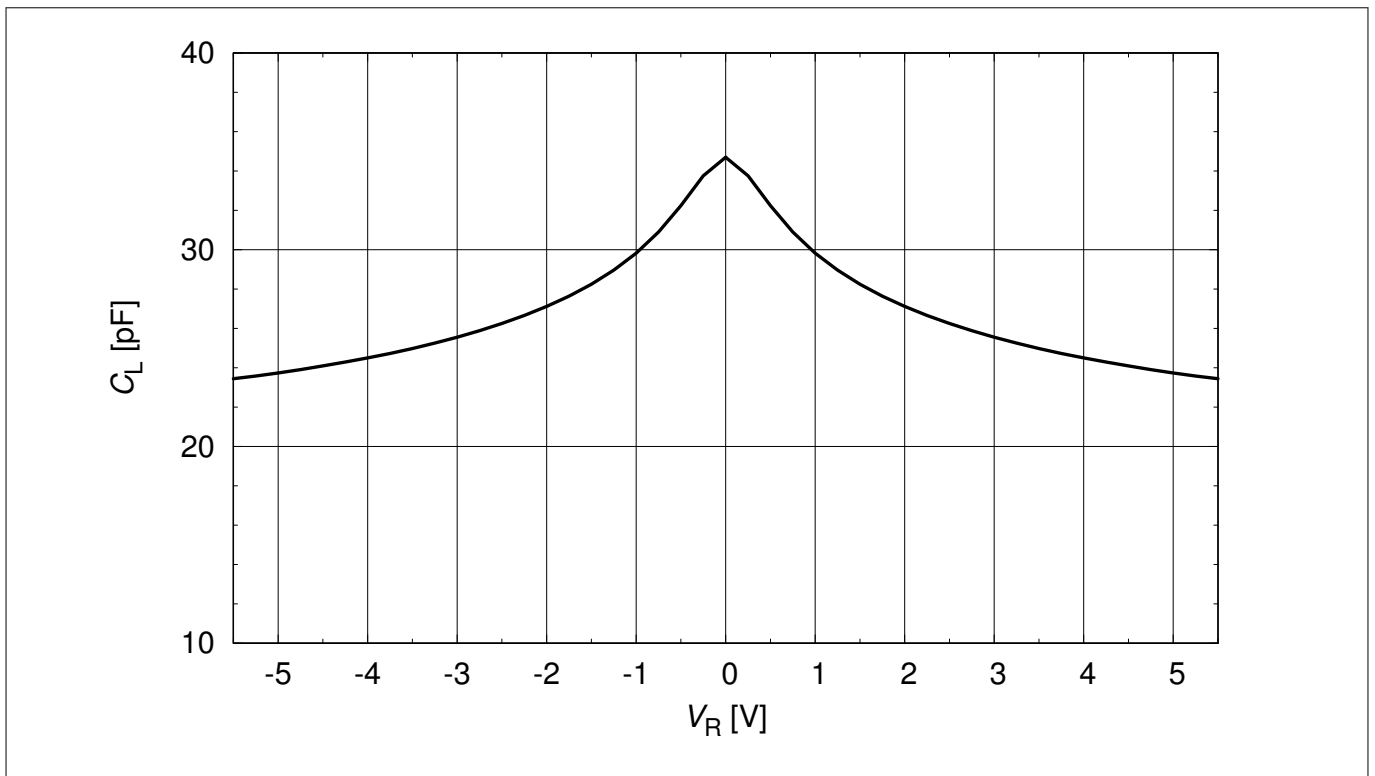


Figure 4 Line capacitance: $C_L = f(V_R)$, $f = 1\text{ MHz}$

Typical characteristic diagrams

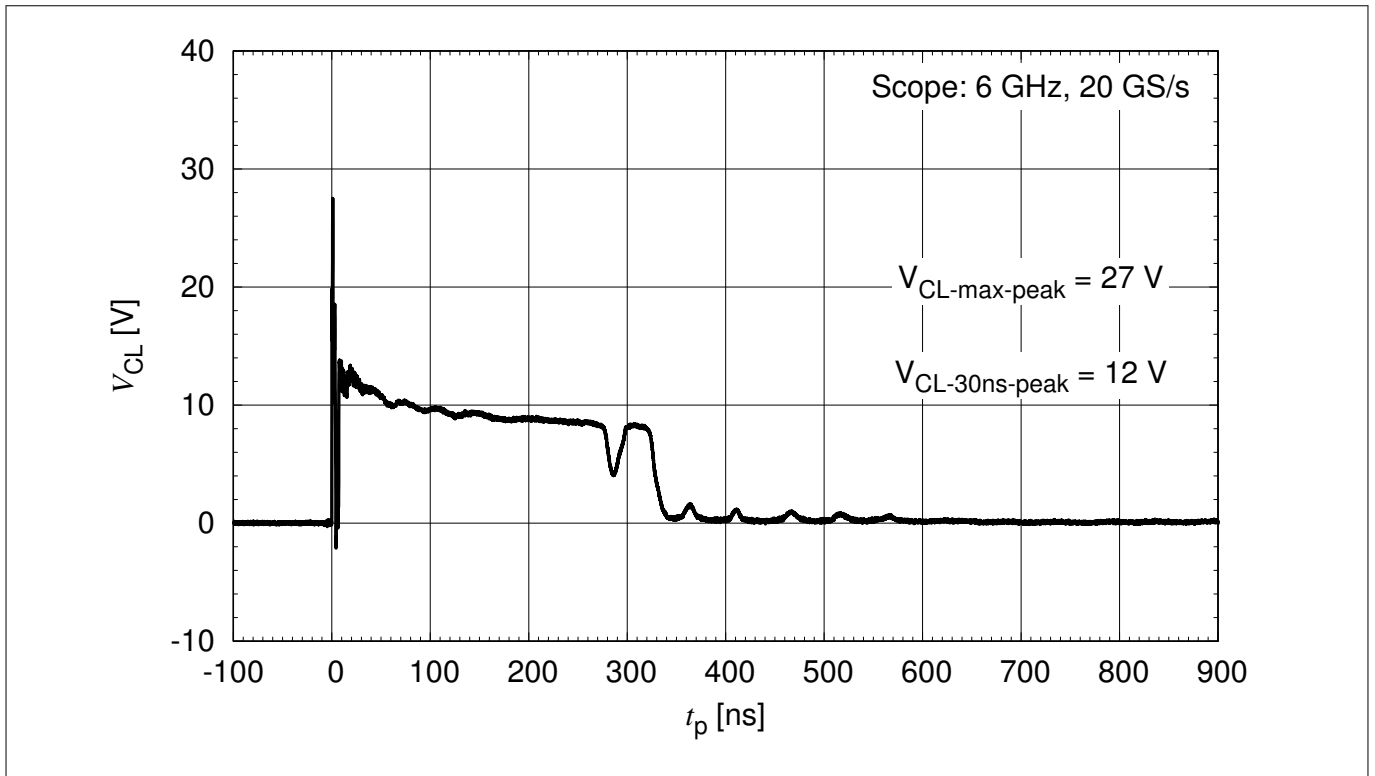


Figure 5 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positive pulse according to IEC 61000-4-2

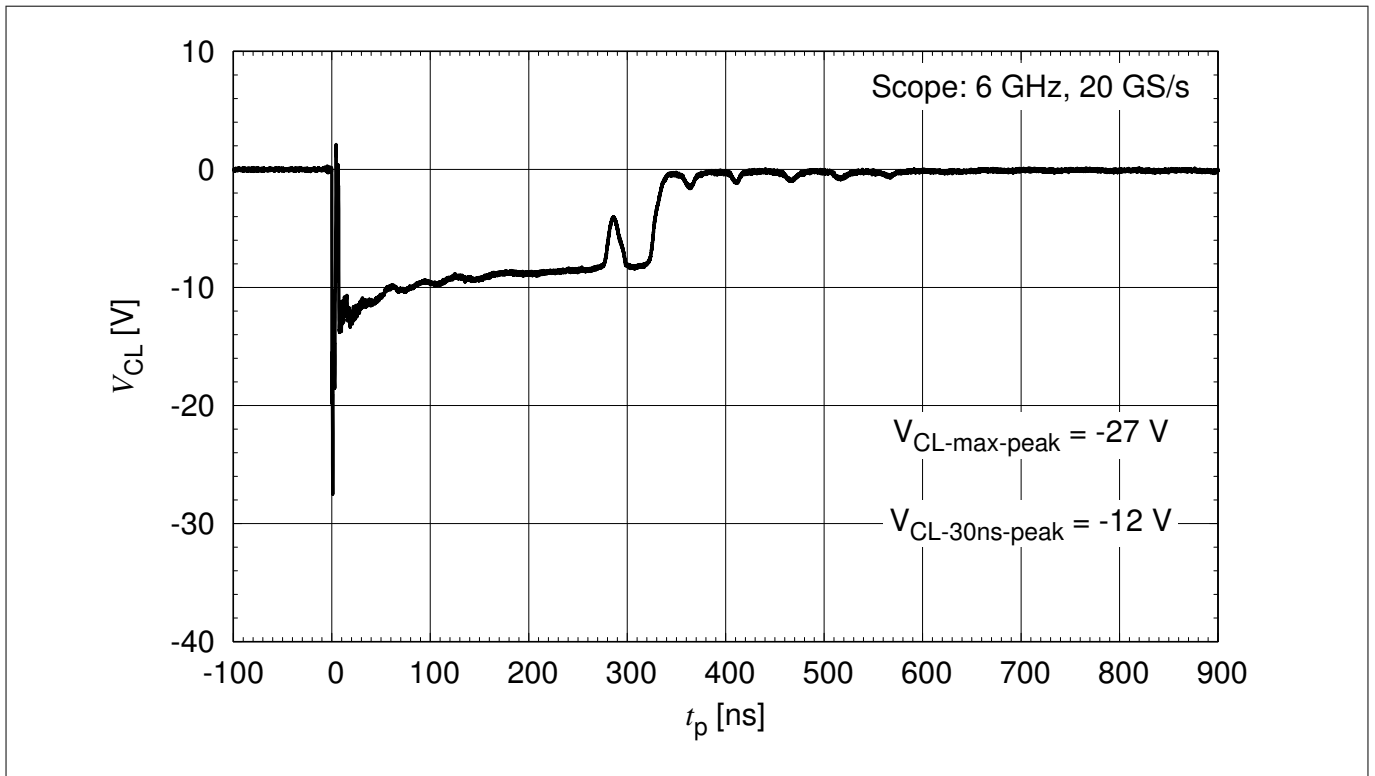


Figure 6 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negative pulse according to IEC 61000-4-2

Typical characteristic diagrams

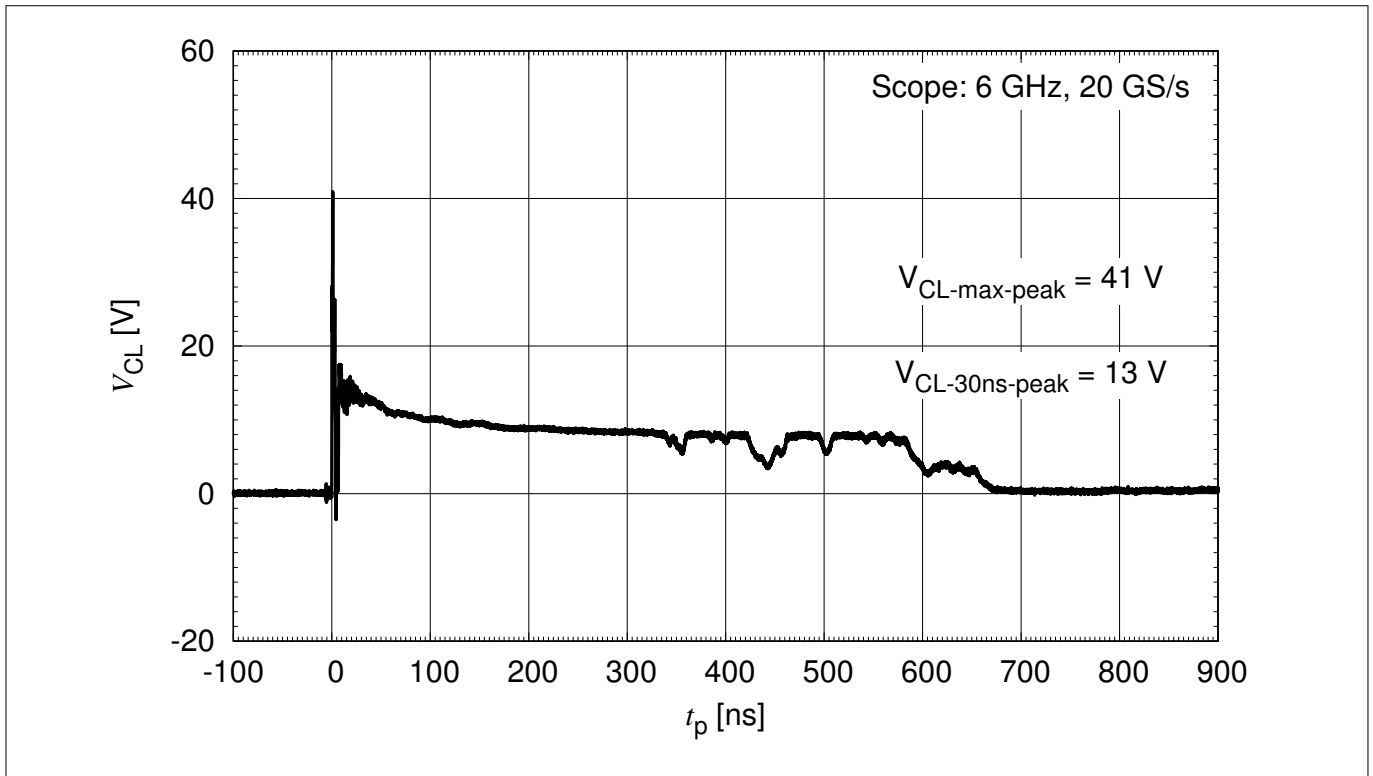


Figure 7 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV positive pulse according to IEC 61000-4-2

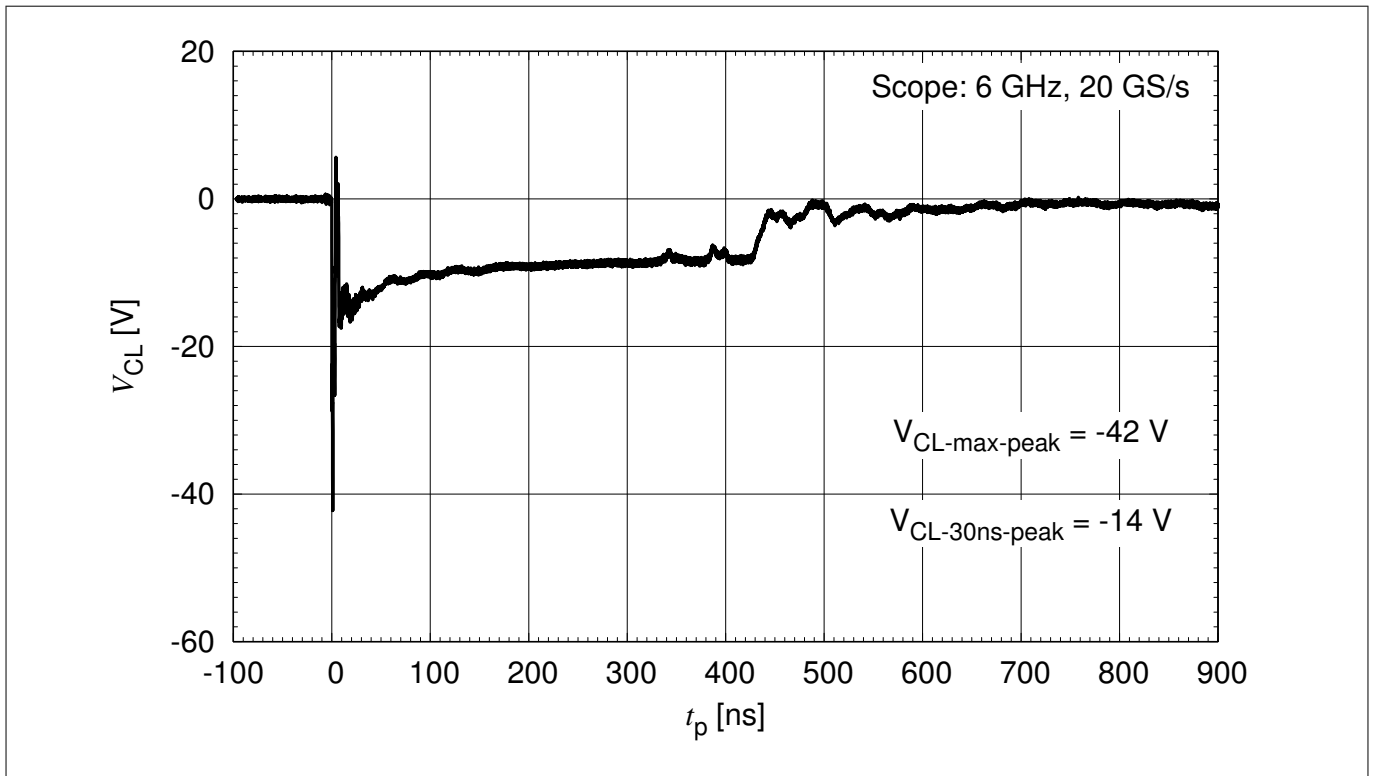


Figure 8 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV negative pulse according to IEC 61000-4-2

Typical characteristic diagrams

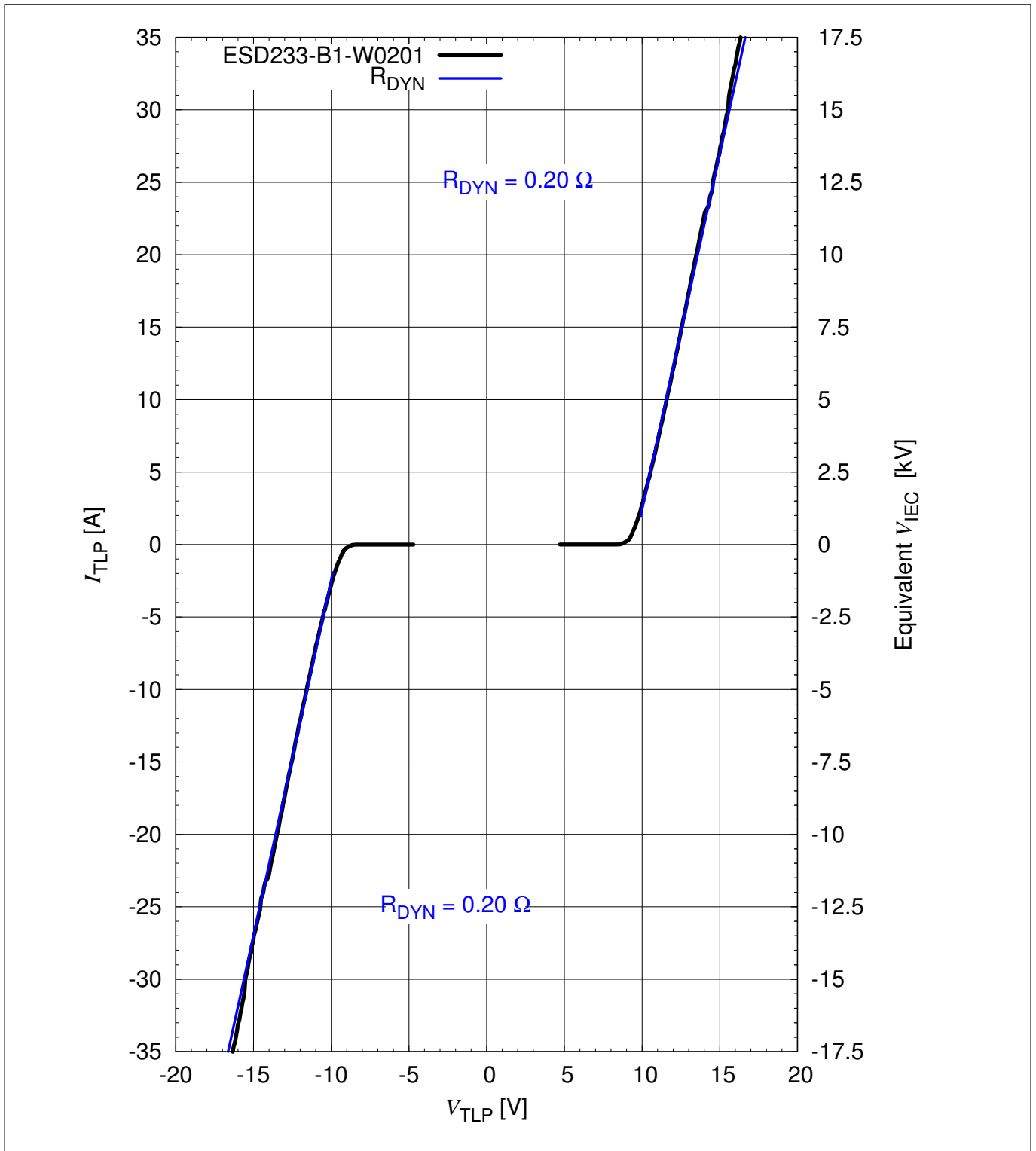


Figure 9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

Typical characteristic diagrams

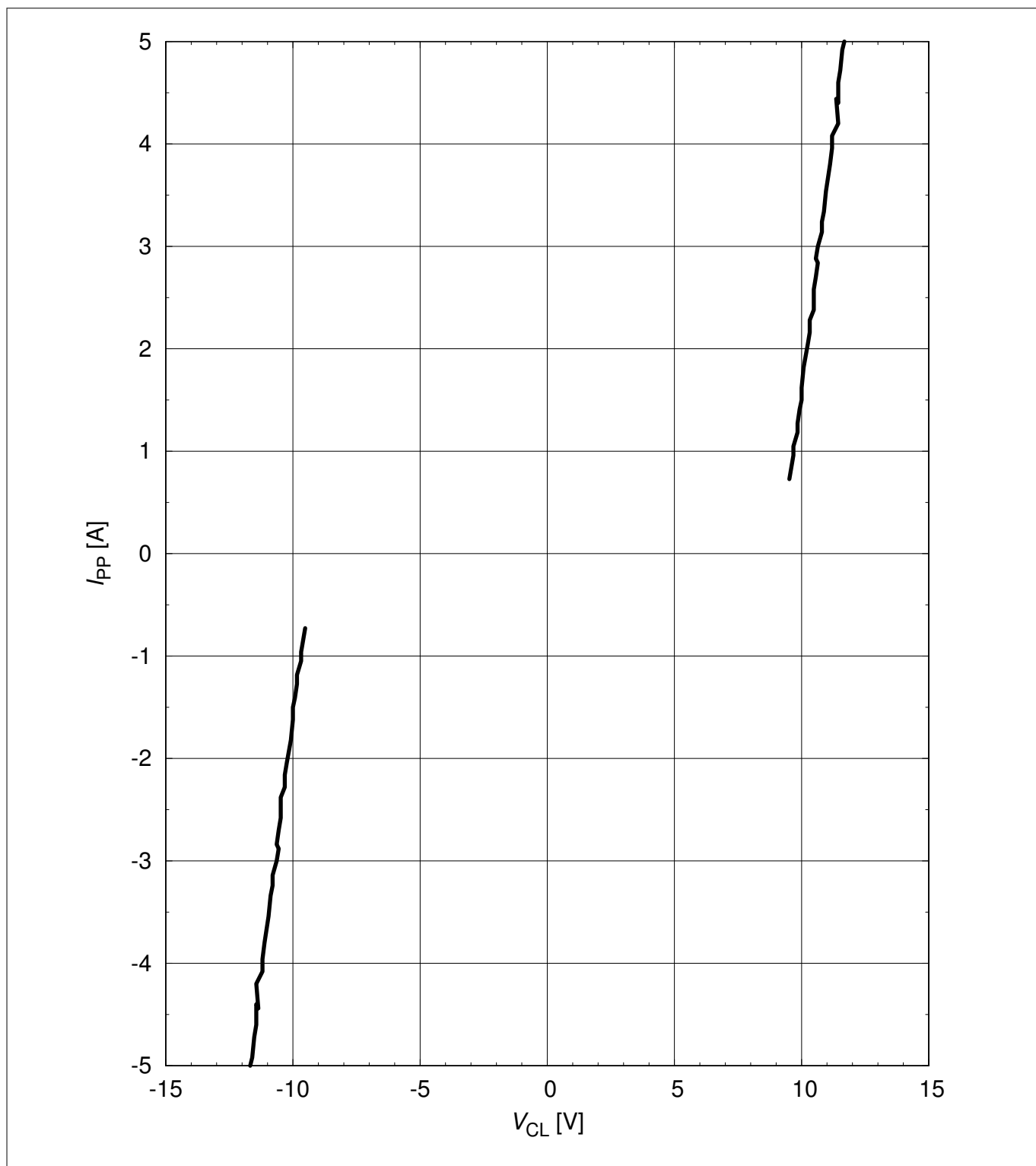


Figure 10 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ according to IEC61000-4-5 [1]

Typical characteristic diagrams

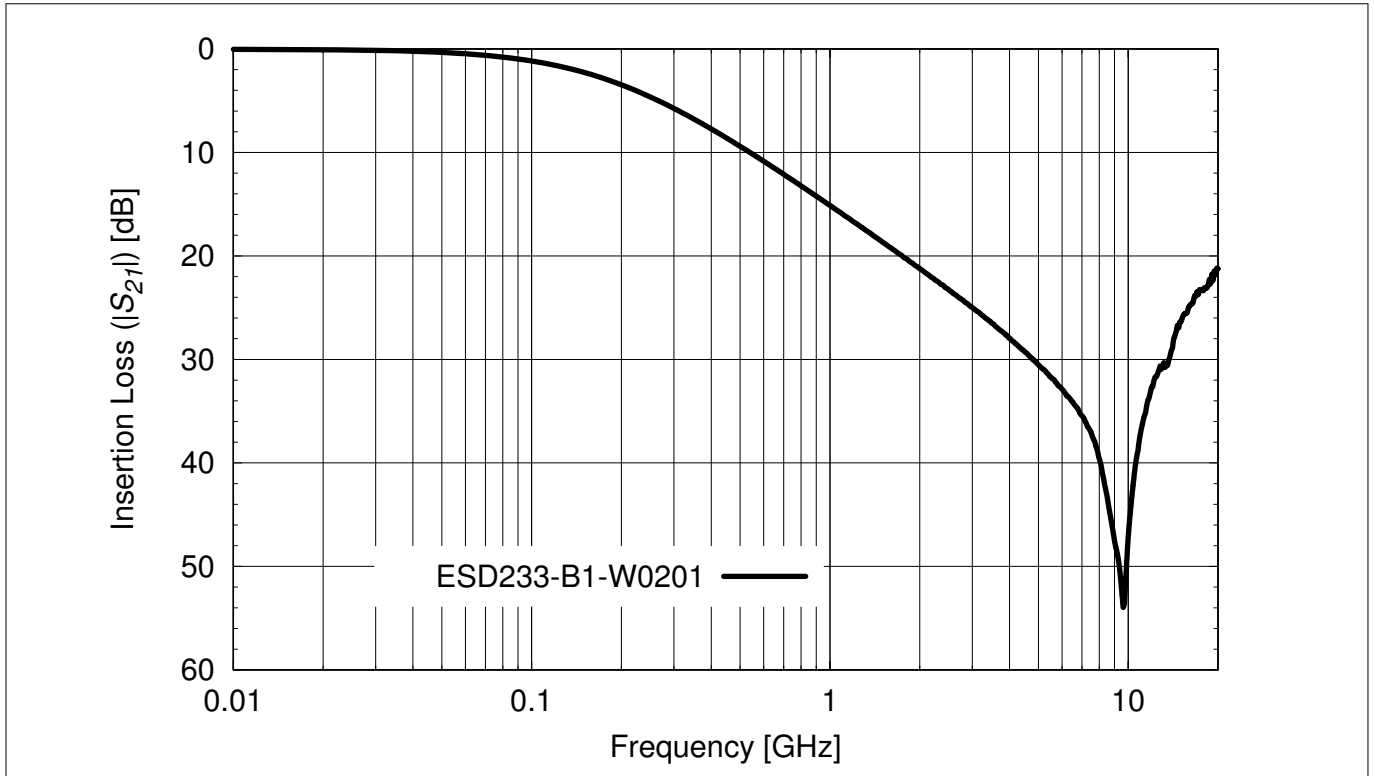


Figure 11 Insertion loss vs. frequency in a 50 Ω system

Package information

4 Package information

4.1 WLL-2-1 Package

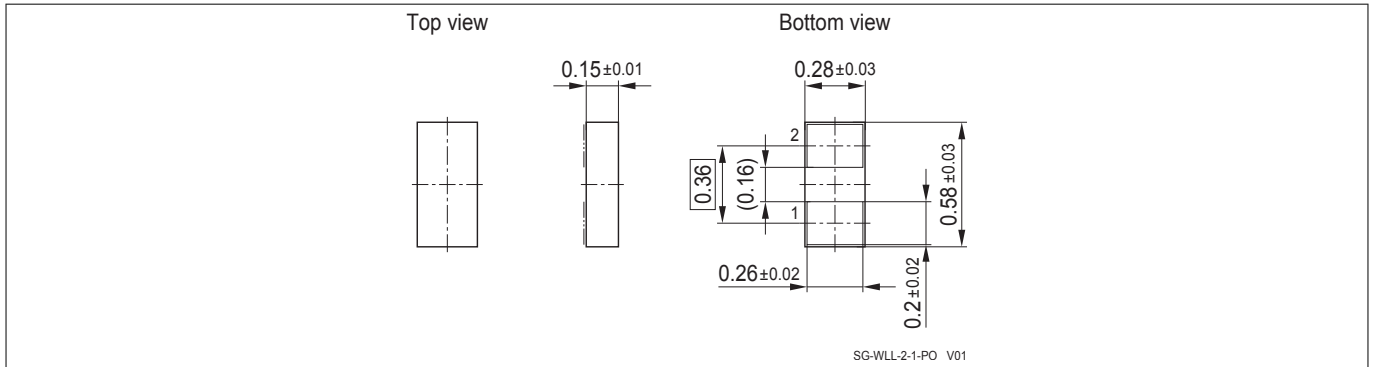


Figure 12 WLL-2-1 Package outline (dimension in mm)

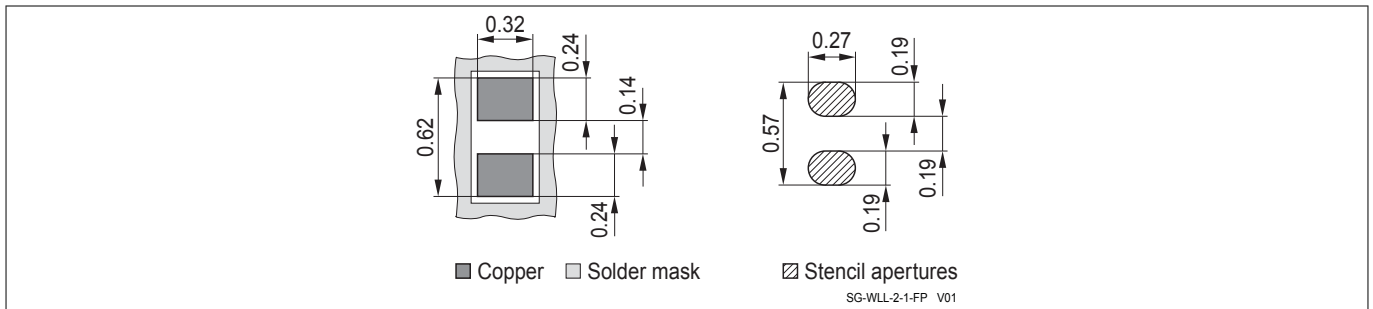


Figure 13 WLL-2-1 Footprint (dimension in mm), recommendations for Printed Circuit Board Assembly see [2]

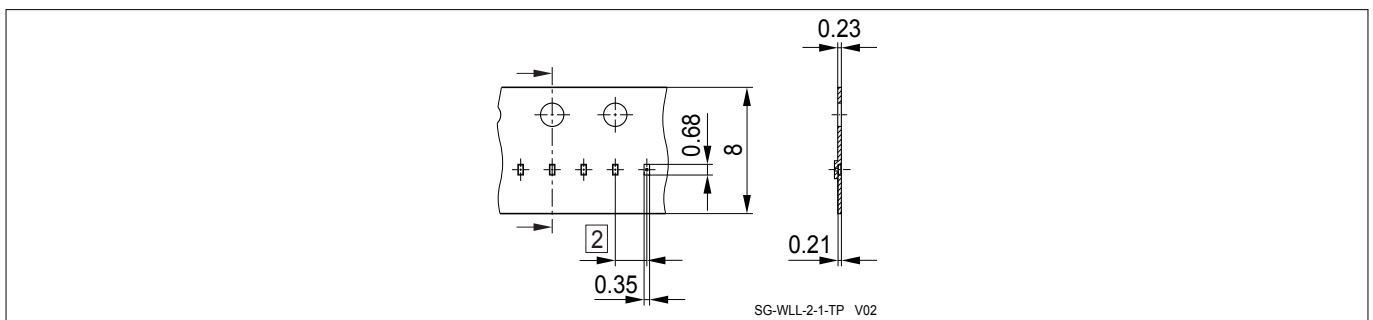


Figure 14 WLL-2-1 Packing (dimension in mm)

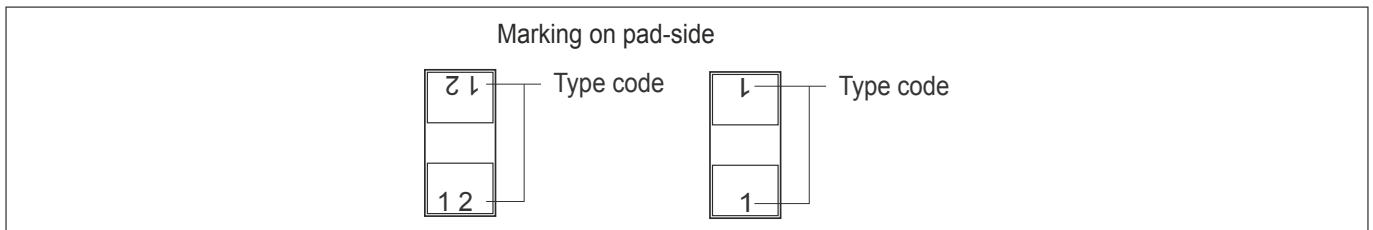


Figure 15 WLL-2-1 Marking example (see also Table 1)

References

5 References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages
http://www.infineon.com/Packageinformation_WLL
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

Revision history

Revision history: Revision 0.9.1, 2016-01-25

Page or Item	Subjects (major changes since previous revision)
Revision 1.0, 2017-05-22	
Chapter 2, 3	Tables of DC, AC characteristics updated
	Typical characteristic diagrams added

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