IFX80471

Step-Down DC/DC Controller

IFX80471SKV
IFX80471SKV50

Data Sheet

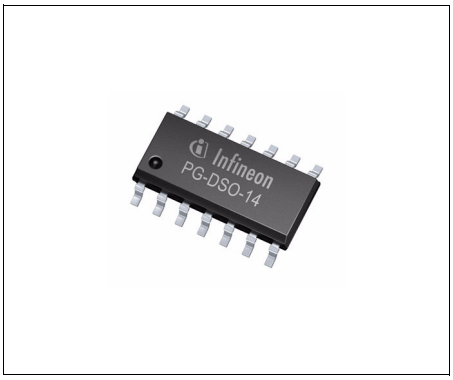
Rev. 1.0, 2011-02-07

Standard Power

Table of Contents

RoHS

1 Overview



PG-DSO-14

Features

- Input voltage range from 5V up to 60V
- Output voltage: 5V fixed or adjustable
- Output voltage accuracy: 3%
- Output current up to 2.3A
- 100% maximum duty cycle
- Less than 120µA quiescent current at low loads[1)]
- 2µA max. shutdown current at device off (IFX80471SKV)
- Fixed 360kHz switching frequency
- Frequency synchronization input for external clocks
- Current Mode control scheme
- Integrated output undervoltage reset circuit[2)]
- On chip low battery detector (on chip comparator)
- Temperature range -40°C to 125 °C
- Green Product (RoHS compliant)

[1)] dependent on external component

[2)] for the adjustable version IFX80471SKV the reset functionality is available for output voltages > 7V

For automotive and transportation applications, please refer to the Infineon TLE and TLF voltage regulator series.

Description

The IFX80471 step-down DC-DC switching controllers provide high efficiency over loads ranging from 1mA up to 2.3A. A unique PWM/PFM control scheme operates with a duty cycle up to 100% resulting in a very low dropout voltage. This control scheme eliminates minimum load requirements and reduces the supply current under light loads to 120µA, depending on dimensioning of external components. In addition the adjustable version IFX80471SKV can be shut down via the Enable input reducing the input current to <2µA. The IFX80471 step-down controllers drive an external P-channel MOSFET, allowing design flexibility for applications up to 11.5W of output power at 5V output voltage. The IFX80471 offers high switching frequency of up to 360kHz as well as operation in continuous-conduction mode and allows the usage of tiny surface-mount inductors. Output capacitor requirements are also reduced, minimizing PC board area and system costs. The output voltage of the IFX80471SKV50 is preset to 5V and is adjustable for the IFX80471SKV. The IFX80471SKV50 features a reset function with a threshold between 4.5V and 4.8V, including a small hysteresis of typ. 50mV. Input voltages of both IFX80471 versions can be up to 60V.

Type	Package	Marking
IFX80471SKV	PG-DSO-14	I80471V
IFX80471SKV50	PG-DSO-14	I80471V50

2 Block Diagram

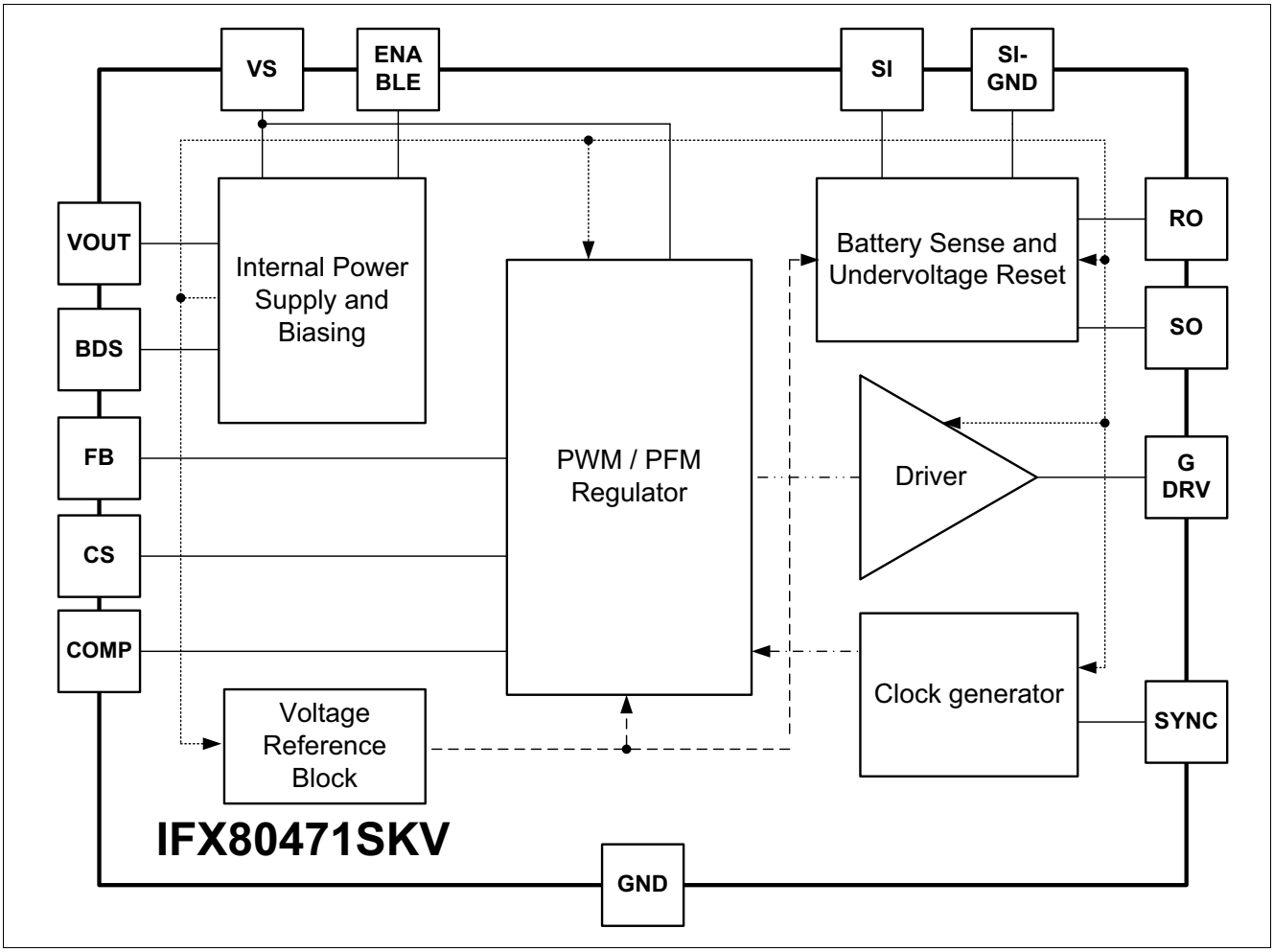


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment

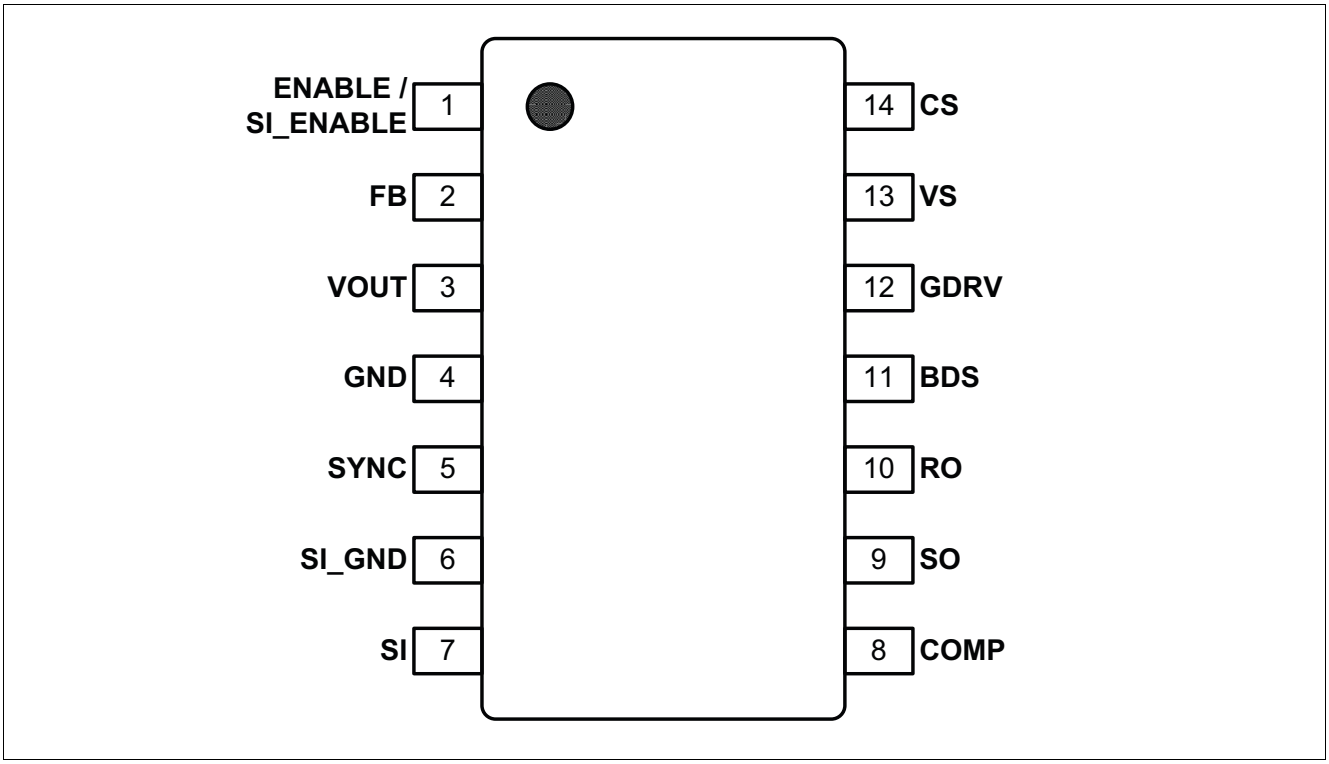


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

Pin	Symbol	Function
1	ENABLE	**Active-High enable input (only adjustable version, IFX80471SKV) for the device.** The device is shut down when ENABLE is driven low. In this shut down-mode the reference, the output and the external MOSFET are turned off. Connect to logic high for normal operation.
1	SI_ENABLE	**Active-High enable input (only 5V version, IFX80471SKV50) for SI_GND input.** SI_GND is switched to high impedance when SI_ENABLE is low. High level at SI_ENABLE connects SI_GND to GND with low impedance. SO is undefined when SI_ENABLE is low.
2	FB	**Feedback input.** 1. For adjustable version (IFX80471SKV) connect this pin to an external voltage divider from the output to GND (see **Chapter 7.2**). 2. For the 5V fixed output voltage version (IFX80471SKV50) the FB is connected to an on-chip voltage divider supplied internally by VOUT. It does not have to be connected externally to the output.
3	VOUT	**Buck output voltage input.** Input for the internal supply. Connect always to the output of the buck converter (output capacitor).

Pin	Symbol	Function
4	GND	**Ground connection.** Analog signal ground.
5	SYNC	**Input for external frequency synchronization.** An external clock signal connected to this pin allows switching frequency synchronization of the device. The internal oscillator is clocked then by the frequency applied at the SYNC input.
6	SI_GND	**SI-Ground input.** Ground connection for SI comparator resistor divider. Depending on SI_ENABLE this input is switched to high impedance or low ohmic to GND.
7	SI	**Sense comparator input.** Input of the low-battery comparator. This input is compared to an internal 1.25V reference where SO gives the result of the comparison. Can be used for any comparison, not necessarily as battery sense.
8	COMP	**Compensation input.** Connect via RC-compensation network to GND.
9	SO	**Sense comparator output.** Open drain output from SI comparator at the adjustable version (IFX80471SKV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (IFX80471SKV50).
10	RO	**Reset output.** Open drain output from undervoltage reset comparator at the adjustable version (IFX80471SKV), Pull down structure with an internal 20kΩ pull up resistor to VOUT at the 5V version (IFX80471SKV50).
11	BDS	**Buck driver supply input.** Connect a ceramic capacitor between BDS and VS to generate clamped gate-source voltage to supply the driver of the PMOS power stage.
12	GDRV	**Gate drive output.** Connect to the gate of the external P-Channel MOSFET. The voltage at GDRV swings between the levels of VS and BDS.
13	VS	**Device supply input.** Connect a 220nF ceramic cap close to the pin in addition to the low ESR tantalum input capacitance.
14	CS	**Current-sense input.** Connect current-sense resistor between VS and CS. The voltage drop over the sense-resistor determines the peak current flowing in the buck circuit. The external MOSFET is turned off when the peak current is exceeded.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Device supply input VS						
4.1.1	Voltage	V_{VS}	-0.3	61	V	–
4.1.2	Current	I_{VS}	–	–	–	–
Current sense input CS						
4.1.3	Voltage	V_{CS}	-0.3	61	V	$\lvert V_{VS} - V_{CS}\rvert < 0.3V$
4.1.4	Current	I_{CS}	–	–	–	–
Gate drive output GDRV						
4.1.5	Voltage	V_{GDRV}	– 0.3	61	V	-0.3V < $\lvert V_{VS} - V_{GDRV}\rvert$ < 6.8V; -0.3V < $\lvert V_{BDS} - V_{GDRV}\rvert$ < 6.8V
4.1.6	Current	I_{GDRV}	–	–	–	limited internally
Buck driver supply input BDS						
4.1.7	Voltage	V_{BDS}	– 0.3	61	V	-0.3V < $\lvert V_{VS} - V_{BDS}\rvert$ < 6.8V
4.1.8	Current	I_{BDS}	–	–	–	–
Feedback input FB						
4.1.9	Voltage	V_{FB}	– 0.3	6.8	V	–
4.1.10	Current	I_{FB}	–	–	–	–
Enable input SI_ENABLE						
4.1.11	Voltage	V_{SI_ENABLE}	– 0.3	61	V	IFX80471SKV50
4.1.12	Current	I_{SI_ENABLE}	–	–	–	–
SI-Ground input SI_GND						
4.1.13	Voltage	V_{SI_GND}	– 0.3	61	V	–
4.1.14	Current	I_{SI_GND}	–	–	–	–
Enable input ENABLE						
4.1.15	Voltage	V_{ENABLE}	– 0.3	61	V	IFX80471SKV
4.1.16	Current	I_{ENABLE}	–	–	V	–
Sense comparator input SI						
4.1.17	Voltage	V_{SI}	– 0.3	61	V	–
4.1.18	Current	I_{SI}	–	–	V	–
Sense comparator output SO						
4.1.19	Voltage	V_{SO}	– 0.3	6.8	V	–
4.1.20	Current	I_{SO}	–	–	V	limited internally

Absolute Maximum Ratings (cont'd)[1)]

all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Buck output voltage input VOUT						
4.1.21	Voltage	V_{VOUT}	– 0.3	15	V	IFX80471SKV
4.1.22	Voltage	V_{VOUT}	– 0.3	6.8	V	IFX80471SKV50
4.1.23	Current	I_{VOUT}	–	–	V	–
Compensation input COMP						
4.1.24	Voltage	V_{COMP}	– 0.3	6.8	V	–
4.1.25	Current	I_{COMP}	–	–	V	–
Reset output RO						
4.1.26	Voltage	V_{RO}	– 0.3	6.8	V	–
4.1.27	Current	I_{RO}	–	–	V	limited internally
Frequency synchronization input SYNC						
4.1.28	Voltage	V_{SYNC}	– 0.3	6.8	V	–
4.1.29	Current	I_{SYNC}	–	–	V	–
Temperatures						
4.1.30	Junction Temperature	T_J	-40	150	°C	–
4.1.31	Storage temperature	T_{STG}	-50	150	°C	–
ESD Susceptibility						
4.1.32	ESD Resistivity Pin V_{OUT}	V_{ESD_VOUT}	-1.5	1.5	kV	HBM[2)]
4.1.33	ESD Resistivity all Pins except V_{OUT}	V_{ESD}	-2	2	kV	HBM[2)]
4.1.34	ESD Resistivity to GND	V_{ESD}	-500	500	V	CDM[3)]

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to EIA/JESD 22-A114B

3) ESD susceptibility, Charged Device Model "CDM" EIA/JESD22-C101 or ESDA STM5.3.1

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 1

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply Voltage Range	V_{VS}	5	60	V	–
4.2.2	Output voltage adjust range IFX80471SKV	V_{OUT}	7	15	V	IFX80471SKV
4.2.3	Sense Resistor	R_{SENSE}	10	47	mΩ	Calculation see **Chapter 7**
4.2.4	PMOS, on+off delay	$t_{on+off\ delay}$	–	t_{min}-300 [1]	ns	t_{min}= V_{VOUT} / (V_{VS}*f_{SW})
4.2.5	Buck driver supply capacitor	C_{BDS}	220	–	nF	–
4.2.6	Buck inductance	L_1	22	100	µH	–[2]
4.2.7	Buck output capacitor	C_{OUT}	100	–	µF	–
4.2.8	Junction Temperature	T_j	-40	125	°C	–

1) A too high PMOS on+off delay might cause an instable output voltage

2) a recommended minimum value for L_1 is 47µH

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Soldering Point[1)]	R_{thJSP}	–	50	–	K/W	–
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	140	–	K/W	Footprint only

1) Not subject to production test, specified by design.

5 Electrical Characteristics

5.1 Electrical Characteristics

Electrical Characteristics: Power

5V < V_{VS} < 48V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Current Consumption[1] IFX80471SKV50							
5.1.1	Current consumption of VS	I_{VS}	–	80	150	µA	V_{VS} = 48V; PFM mode
			–	70	85	µA	V_{VS} = 13.5V; PFM mode; T_j = 25 °C
5.1.2	Current consumption of SI_ENABLE	I_{SI_ENABLE}	–	9	30	µA	V_{VS} = 48V; V_{SI_ENABLE} = 48V; PFM mode
5.1.3	Current consumption of VOUT	I_{VOUT}	–	95	130	µA	V_{SI_ENABLE} = L; V_{VOUT} = 5.5V; V_{VS}=13.5V; PFM mode; T_j = 25°C
			–	140	220	µA	V_{SI_ENABLE} = H; V_{VOUT} = 5.5V; V_{VS} = 13.5V; V_{SI} > $V_{SI, high}$; PFM mode
5.1.4	Current consumption of SI	I_{SI}	–	0.2	0.5	µA	V_{SI_ENABLE} = H; V_{VS} = 13.5V; V_{SI} = 10V; PFM mode
Current Consumption[1] IFX80471SKV (variable)							
5.1.5	Current consumption of VS	I_{VS}	–	80	150	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode; V_{OUT} ≥ 7V
			–	70	85	µA	V_{VS} = 13.5V; V_{ENABLE} = H; PFM mode; T_j = 25 °C; V_{OUT} ≥ 7V
5.1.6	Current consumption of VS		–		2	µA	V_{ENABLE} = 0V; T_j < 105°C
5.1.7	Current consumption of ENABLE	I_{EN}	–	9	30	µA	V_{VS} = 48V; V_{ENABLE} = H; PFM mode

Electrical Characteristics: Power (cont'd)

5V < V_{VS} < 48V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.8	Current consumption of VOUT	I_{VOUT}	–	140	220	µA	V_{OUT} = 8V; V_{VS} = 13.5V; V_{ENABLE} = H; $V_{SI} > V_{SI, high}$; PFM mode
5.1.9	Current consumption of SI	I_{SI}	–	0.2	0.5	µA	V_{VS} = 13.5V; V_{ENABLE} = H; V_{SI} = 10V; PFM mode; T_j = 25°C
5.1.10	Current consumption of FB	I_{FB}	–	0.2	0.5	µA	V_{VS} = 13.5V; V_{FB} = 1.25V; V_{ENABLE} = H; PFM mode; T_j = 25°C
Buck Controller							
5.1.11	Output voltage	V_{VOUT}	4.85	5.00	5.15	V	IFX80471SKV50; V_{VS}=13.5V& 48V; PWM mode I_{OUT} = 0.5 to 2A; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω
			4.75	5.00	5.25	V	IFX80471SKV50; V_{VS} = 24V; PFM mode; I_{OUT} = 15mA; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
5.1.12	FB threshold voltage	$V_{FB, th}$	1.225	1.25	1.275	V	IFX80471SKV
5.1.13	Output voltage	V_{VOUT}	9.7	10.0	10.3	V	IFX80471SKV; Calibrated divider, see **Chapter 7.2**; V_{VS} = 13.5V & 48V; I_{OUT} = 0.5 to 2A; PWM mode; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;
			9.5	10.0	10.5	V	IFX80471SKV; Calibrated divider, see **Chapter 7.2**; V_{VS} = 24V; I_{OUT} = 15mA; PFM mode; R_{SENSE} = 22mΩ; R_{M1} = 0.25Ω; R_{L1} = 0.1Ω;

Electrical Characteristics: Power (cont'd)

5V < V_{VS} < 48V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.14	Buck output voltage adjust range	V_{VOUT}	$V_{FB, th}$	–	7	V	IFX80471SKV, supplied by V_S only, complete current to supply the IC drawn from VS, no reset function [2]
			7	–	15	V	IFX80471SKV, current to supply the IC drawn from VS and VOUT, as specified [2]
5.1.15	Buck output voltage accuracy	V_{VOUT}	0.97 * V_{OUT_nom}	–	1.03 * V_{OUT_nom}		IFX80471SKV; PWM mode [2]
5.1.16	Buck output voltage accuracy	V_{VOUT}	0.95 * V_{OUT_nom}	–	1.05 * V_{OUT_nom}		IFX80471SKV, PFM mode [2]
5.1.17	Line regulation	$\lvert \Delta V_{VOUT} \rvert$	–	–	35	mV	IFX80471SKV50, V_{VS} = 9V to 16V; I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
			–	–	50	mV	IFX80471SKV50, V_{VS} = 16V to 32V; I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
5.1.18	Line regulation	$\Delta V_{VOUT} / V_{VOUT}$	–	–	2.5	%	IFX80471SKV, V_{VS} = 12V to 36V; V_{VOUT}=10V I_{OUT} = 1A; R_{SENSE} = 22mΩ; PWM mode
5.1.19	Load regulation	$\Delta V_{VOUT} / \Delta I_{LOAD}$	–	40	–	mV/A	IFX80471SKV50; I_{OUT} = 0.5A to 2A; V_{VS} = 5.8V & 48V; R_{SENSE} = 22mΩ
			–	8 * V_{OUT_nom} / V	–	mV/A	IFX80471SKV; I_{OUT} = 0.5 to 2A; V_{VS}= 13.5V & 48V; R_{SENSE} = 22mΩ
5.1.20	Gate driver, PMOS off	$V_{VS} - V_{GDRV}$	0	–	0.2	V	V_{ENABLE/SI_ENABLE} = 5 V; C_{BDS} = 220 nF; C_{GDRV} = 4.7nF
5.1.21	Gate driver, PMOS on	$V_{VS} - V_{GDRV}$	6	–	8.2	V	V_{ENABLE/SI_ENABLE} = 5 V; C_{BDS} = 220 nF; C_{GDRV} = 4.7nF[3]
5.1.22	Gate driver, UV lockout	$V_{VS} - V_{BDS}$	2.75	–	4	V	Decreasing (V_{VS}-V_{BDS}) until GDRV is permanently at VS level
5.1.23	Gate driver, peak charging current	I_{GDRV}	–	1	–	A	PMOS dependent; [2]
5.1.24	Gate driver, peak discharging current	I_{GDRV}	–	1	–	A	PMOS dependent; [2]

Electrical Characteristics: Power (cont'd)

5V < V_{VS} < 48V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.25	Gate driver, gate voltage, rise time	t_r	–	45	60	ns	V_{ENABLE/SI_ENABLE} = 5 V; C_{BDS} = 220 nF; C_{GDRV} = 4.7nF
5.1.26	Gate driver, gate voltage, fall time	t_f	–	50	65	ns	V_{ENABLE/SI_ENABLE} = 5 V; C_{BDS} = 220 nF; C_{GDRV} = 4.7nF
5.1.27	Peak current limit threshold voltage	V_{LIM} = V_{VS} - V_{CS}	50	70	90	mV	
5.1.28	Oscillator frequency	f_{OSC}	290	360	420	kHz	PWM mode only
5.1.29	Maximum duty cycle	d_{MAX}	100	–	–	%	PWM mode only
5.1.30	Minimum on time	t_{MIN}	–	220	400	ns	PWM mode only
5.1.31	SYNC capture range	Δf_{sync}	250	–	530	kHz	PWM mode only
5.1.32	SYNC trigger level high	$V_{SYNC,h}$	4.0	–	–	V	2)
5.1.33	SYNC trigger level low	$V_{SYNC,l}$	–	–	0.8	V	2)
Reset Generator							
5.1.34	Reset headroom	$V_{RT,HEAD}$	80	–	–	mV	IFX80471SKV50; V_{OUT} (V_S=6V, I_{LOAD}=1A) -$V_{VOUT,RT}$
5.1.35	Reset threshold	$V_{VOUT, RT}$	4.5	4.65	4.8	V	IFX80471SKV50; V_{VOUT} increasing/decreasing
5.1.36	Reset threshold hysteresis	$\Delta V_{VOUT, RT}$	–	50	–	mV	IFX80471SKV50 2)
5.1.37	Reset threshold	$V_{FB, RT}$	–	1.12	–	V	IFX80471SKV; V_{VOUT} decreasing
			–	1.17	–	V	IFX80471SKV; V_{VOUT} increasing
5.1.38	Reset output pull up resistor	R_{RO}	10	20	40	kΩ	IFX80471SKV50; Internally connected to V_{OUT}
5.1.39	Reset output High voltage	$V_{RO, H}$	0.8 * V_{VOUT}	–	–	V	IFX80471SKV50; I_{RO} = 0mA
5.1.40	Reset output Low voltage	$V_{RO,L}$	–	0.2	0.4	V	$I_{RO, L}$ = 1mA; 2.5V < V_{VOUT} < V_{RT}
			–	0.2	0.4	V	$I_{RO, L}$ = 0.2mA; 1V < V_{VOUT} < 2.5V
5.1.41	Reset delay time	t_{rd}	17	21	25	ms	IFX80471SKV
			70	82	100	ms	IFX80471SKV50
5.1.42	Reset reaction time	t_{rr}	–	–	10	µs	2)
Overvoltage Lockout							
5.1.43	Overvoltage threshold	$V_{VOUT, OV}$	–	V_{OUT_nom} + 100	–	mV	IFX80471SKV50; V_{VOUT} increasing
5.1.44	Overvoltage threshold	$V_{FB, OV}$	–	$V_{FB,th,nom}$ + 20	–	mV	IFX80471SKV; V_{VOUT} increasing

Electrical Characteristics: Power (cont'd)

5V < V_{VS} < 48V; T_j = -40 °C to +125 °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
ENABLE Input							
5.1.45	Enable ON-threshold	$V_{enable,ON}$	4.5	–	–	V	
5.1.46	Enable OFF-threshold	$V_{enable,OFF}$	–	–	0.8	V	
SI_ENABLE Input							
5.1.47	Enable ON-threshold	$V_{enable,ON}$	4.5	–	–	V	
5.1.48	Enable OFF-threshold	$V_{enable,OFF}$	–	–	0.8	V	
SI_GND Input							
5.1.49	Switch ON resistance	R_{SW}	50	100	230	Ω	V_{SI_ENABLE} = 5V; I_{SI_GND} = 3mA
Battery Voltage Sense							
5.1.50	Sense threshold	$V_{SI, low}$	1.22	1.25	1.28	V	V_{VS} decreasing
5.1.51	Sense threshold	$V_{SI, high}$	–	1.33	–	V	V_{VS} increasing
5.1.52	Sense threshold hysteresis	$V_{SI, hys}$	30	80	120	mV	
5.1.53	Sense output pull up resistor	R_{SO}	10	20	40	kΩ	IFX80471SKV50; Internally connected to V_{VOUT}
5.1.54	Sense out output High voltage	$V_{SO,H}$	0.8 * V_{VOUT}			V	$I_{SO,H}$ =0mA
5.1.55	Sense out output Low voltage	$V_{SO,L}$		0.2	0.4	V	$I_{SO,L}$ = 1mA; 2.5V < V_{VOUT}; V_{SI} < 1.13 V
				0.4	V_{VOUT}	V	I_{SOL}=0.2mA; 1V < V_{VOUT} < 2.5V; V_{SI} < 1.13 V
Thermal Shutdown							
5.1.56	Thermal shutdown junction temperature	T_{jSD}	150	175	200	°C	2)
5.1.57	Temperature hysteresis	ΔT		30		K	2)

1) The device current measurements for I_{VS} and I_{FB} exclude MOSFET driver currents.

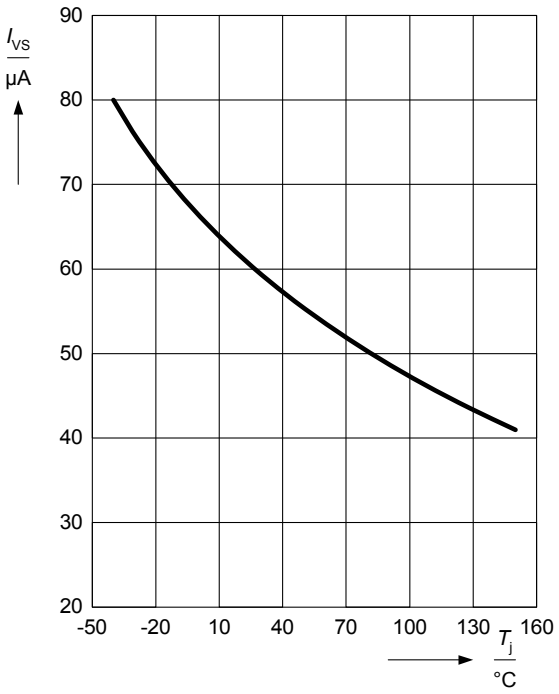
2) Not subject to production test - specified by design

3) For 4V < V_{VS} < 6V: V_{GDRV} ≈ 0V.

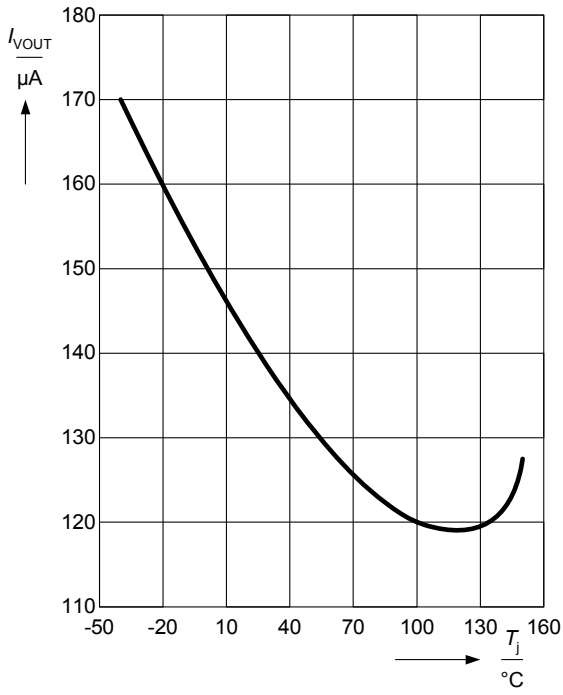
5.2 Typical Performance Characteristics

Typical Performance Characteristics

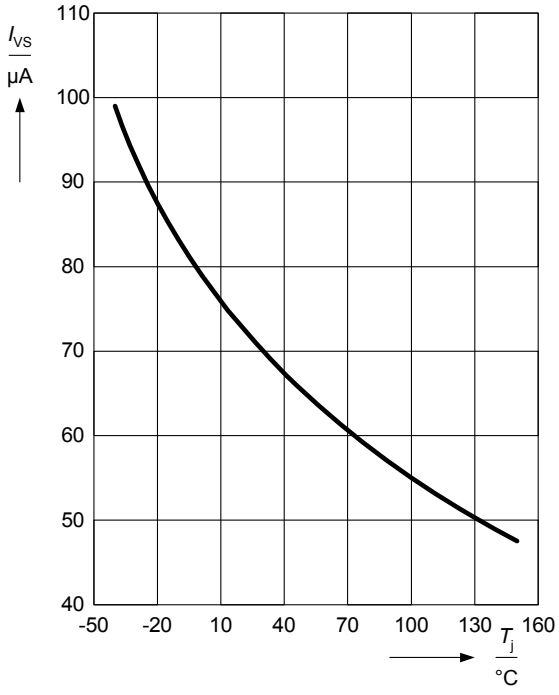
Current Consumption I_{VS} versus Junction Temperature T_J (INH = ON), V_{VS} = 13.5 V



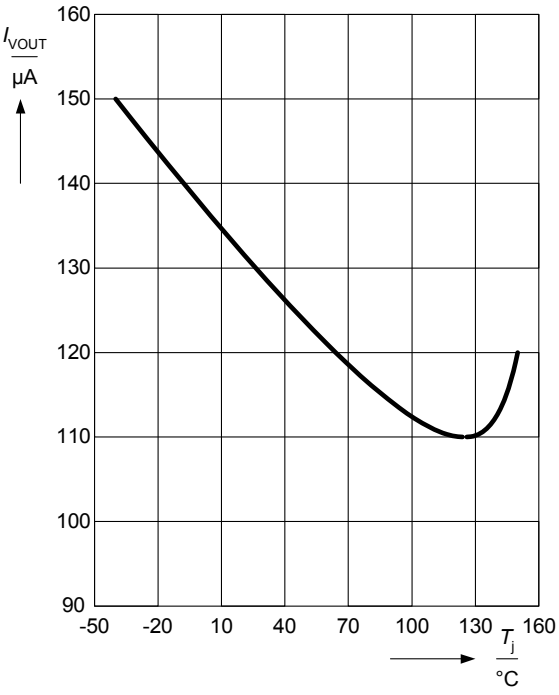
Current Consumption I_{VOUT} versus Junction Temperature T_J (INH = ON), V_{VOUT} = 5.5 V



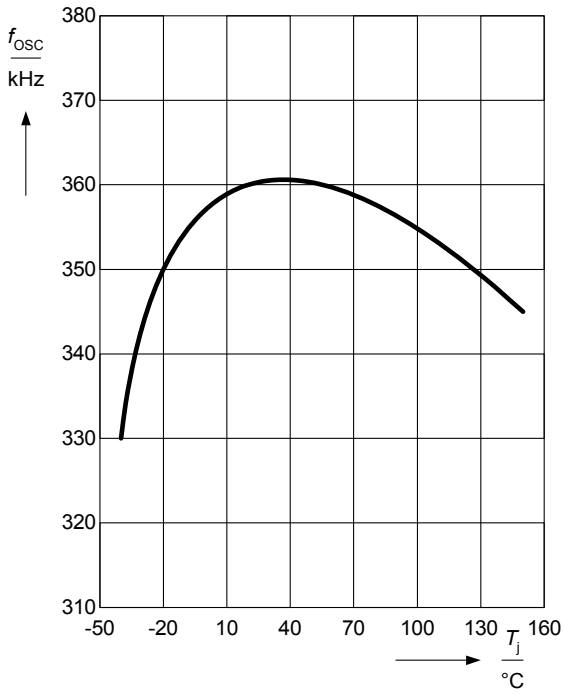
Current Consumption I_{VS} versus Junction Temperature T_J (INH = ON), V_{VOUT} = 48 V



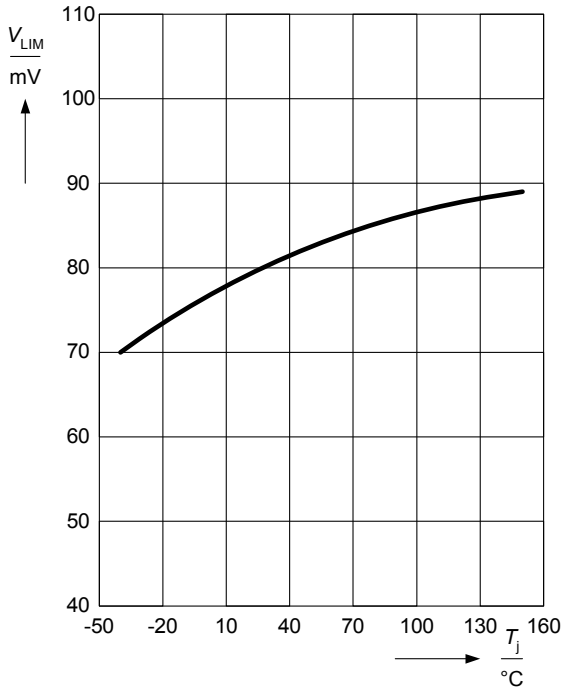
Current Consumption I_{VOUT} vs. Junction Temperature T_J (INH = ON), VOUT = 10 V (IFX80471SKV)



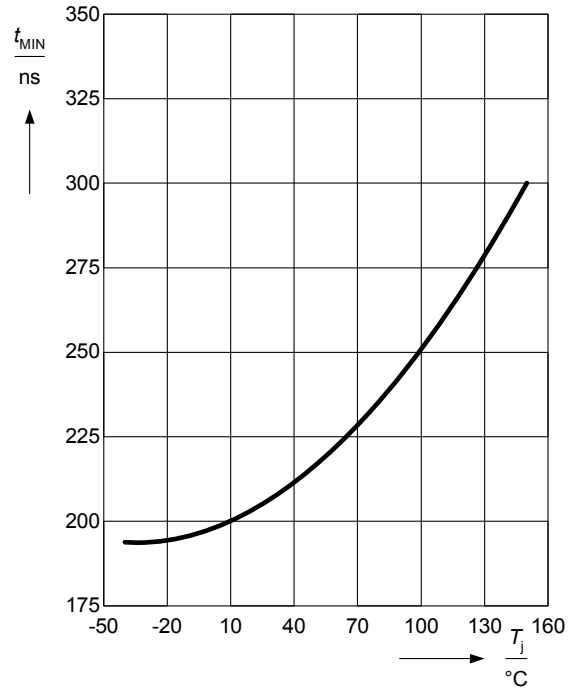
Internal oscillator frequency f_{OSC} versus Junction Temperature T_j)



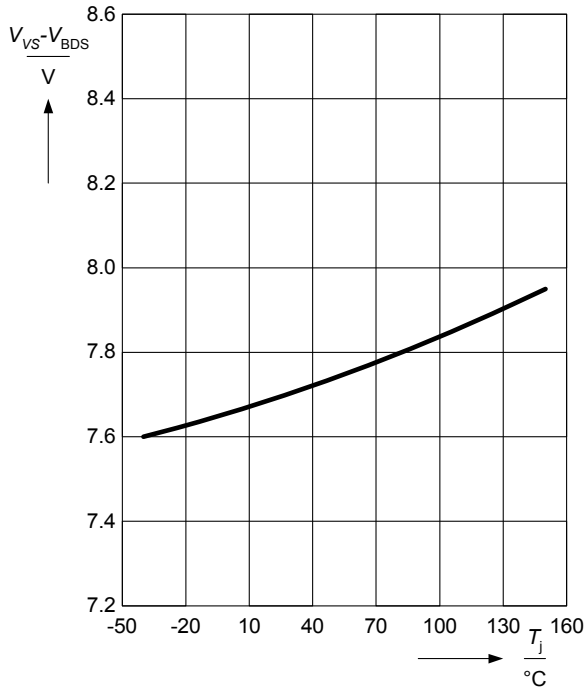
Peak current limit threshold voltage V_{LIM} versus Junction Temperature T_j



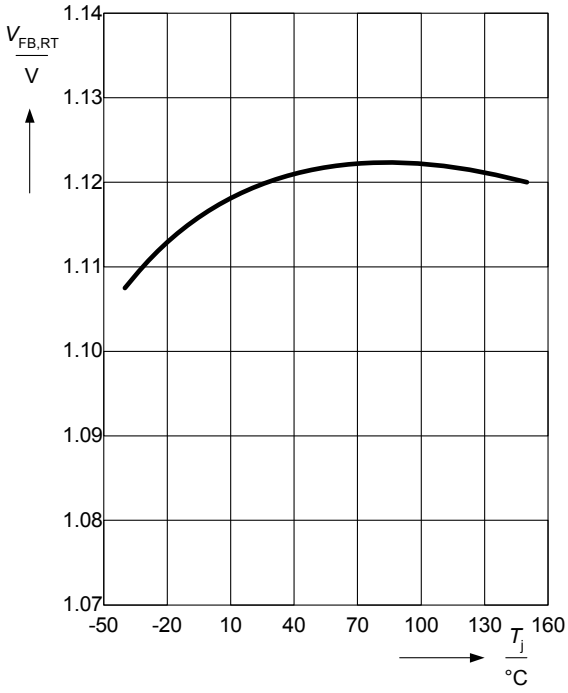
Minimum on time t_{MIN} (blanking) versus Junction Temperature T_j



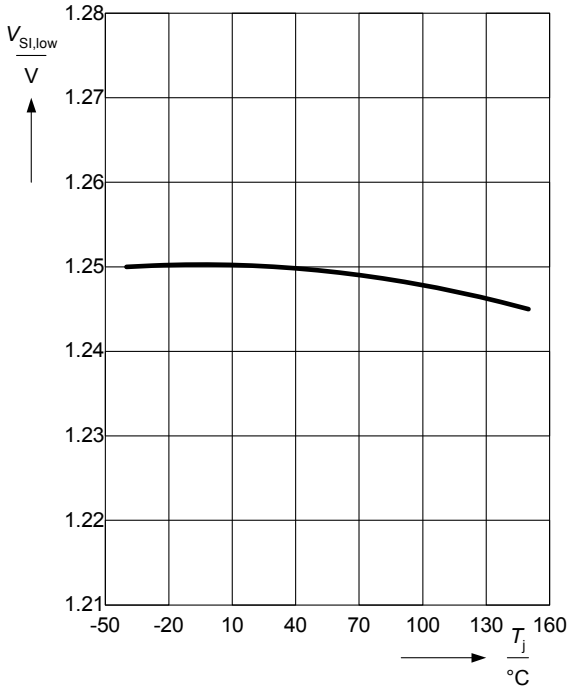
Gate driver supply V_{VS} - V_{BDS} versus Junction Temperature T_j



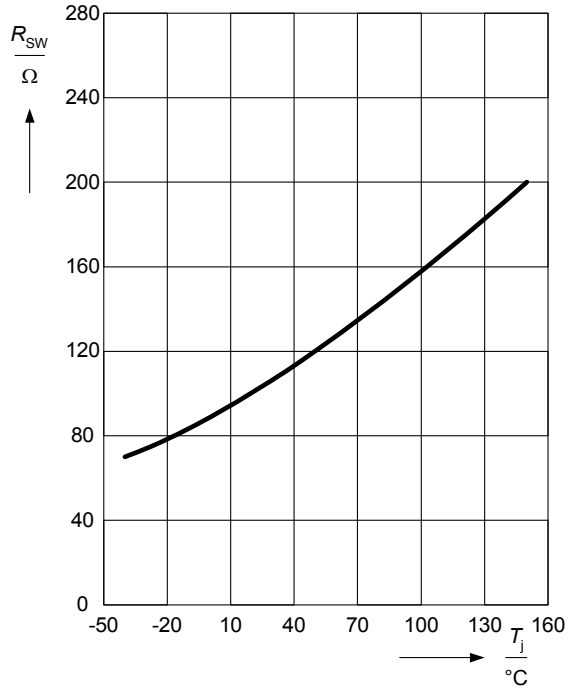
Lower Reset threshold $V_{FB,RT}$ versus Junction Temperature T_j (IFX80471SKV)



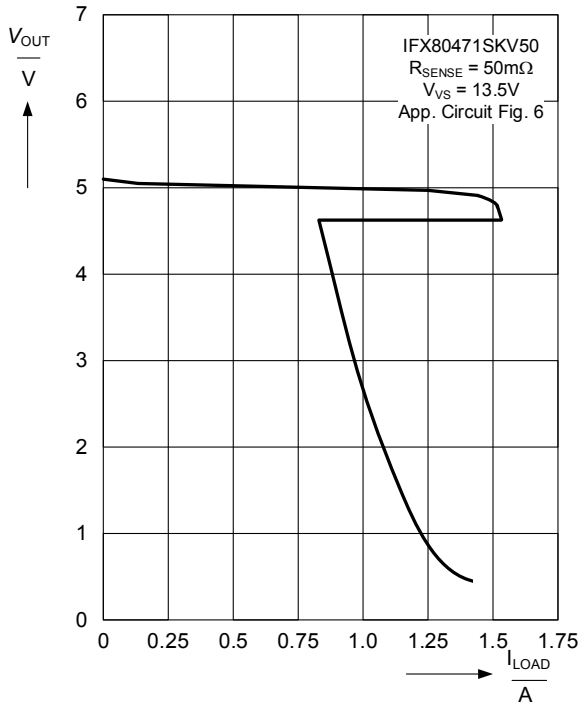
Lower Sense threshold V_{SI}, low versus Junction Temperature T_j



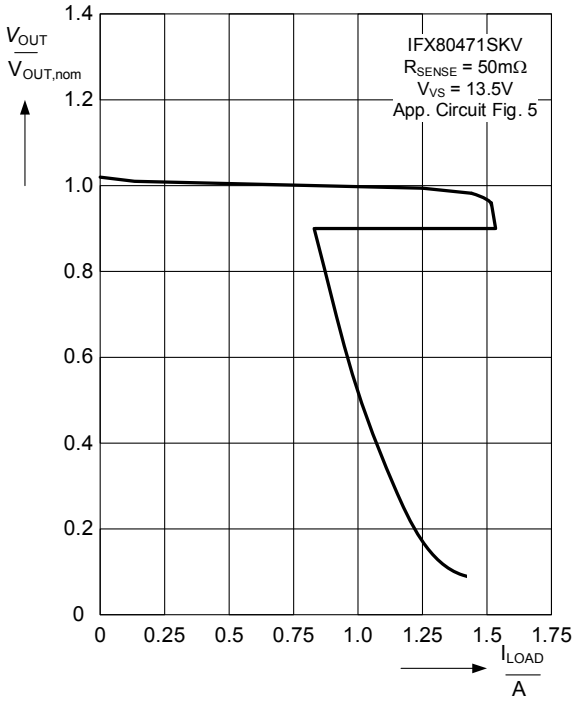
On resistance of SI_GND switch R_{SW} versus Junction Temperature T_j



Output Voltage versus Load Current (IFX80471SKV50)



Output voltage vs. Load Current (IFX80471SKV)



6 Detailed Circuit Description

In the following, the internal blocks of the IFX80471 are described in more detail. For selecting external components please refer to the section **“Application Information” on Page 21**.

6.1 PFM/PWM Step-down regulator

To meet also high requirements in terms of current consumption a special PFM (Pulse Frequency Modulation) - PWM (Pulse Width Modulation) control scheme for highest efficiency is implemented in the IFX80471 regulators. Under light load conditions the output voltage is able to increase slightly and at a certain threshold the controller jumps into PFM mode. In this PFM operation the PMOS is triggered with a certain on time (depending on input voltage, output voltage, inductance- and sense resistor value) whenever the buck output voltage decreases to the so called WAKE-threshold. The switching frequency of the step down regulator is determined in the PFM mode by the load current. It increases with increasing load current and turns finally to the fixed PWM frequency at a certain load current depending on the input voltage, current sense resistor and inductance. The diagram below shows the buck regulation circuit of the IFX80471.

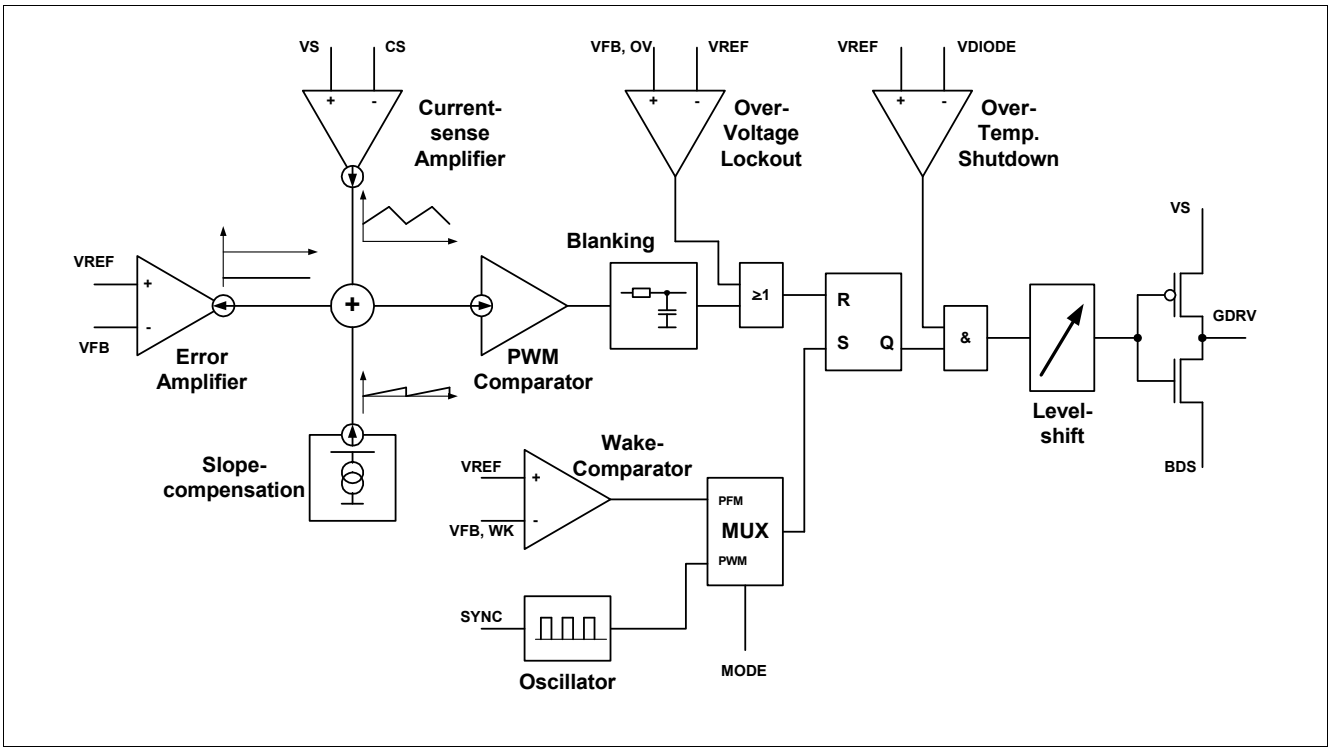


Figure 3 Buck control scheme

The IFX80471 uses a slope-compensated peak current mode PWM control scheme in which the feedback or output voltage of the step down circuit and the peak current of the current through the PMOS are compared to form the OFF signal for the external PMOS. The ON-trigger is set periodically by the internal oscillator when acting in PWM mode and is given by the output of the WAKE-comparator when operating in PFM mode. The Multiplexer (MUX) is switched by the output of the MODE-detector which distinguishes between PFM and PWM by tracking the output voltage (go to PFM) and by tracking the gate trigger frequency (goto PWM). In PFM mode the peak current limit is reduced to prevent overshoots at the output of the buck regulator. In order to avoid a gate turn off signal due to the current peak caused by the parasitic capacitance of the catch diode the blanking filter is necessary. The blanking time is set internally to 200ns and determines (together with the PMOS turn on and turn off delay) the minimum duty cycle of the device. In addition to the PFM/PWM regulation scheme an overvoltage lockout and thermal protection are implemented to guarantee safe operation of the device and of the supplied application circuit.

6.2 Battery voltage sense

To detect undervoltage conditions at the battery a sense comparator block is available within the IFX80471. The voltage at the SI input is compared to an internal reference of typ. 1.25V. The output of the comparator drives a NMOS structure giving a low signal at SO as soon as the voltage at SI decreases below this threshold. In the 5V fixed version an internal pull up resistor is connected from the drain of the NMOS to the output of the buck converter, in the variable version SO is open drain.

The sense in voltage divider can be switched to high impedance by a low signal at the SI_ENABLE to avoid high current consumption to GND (IFX80471SKV50 only).

Of course the sense comparator can be used for any input voltage and does not have to be used for the battery voltage sense only.

6.3 Undervoltage Reset

The output voltage is monitored continuously by the internal undervoltage reset comparator. As soon as the output voltage decreases below the thresholds given in the characteristics the NPN structure pulls RO low (latched). In the 5V fixed version an internal pull up resistor is connected from the collector of the NPN to the output of the buck converter, in the variable version RO is open collector.

At power up RO is kept low until the output voltage has reached its reset threshold and stayed above this threshold for the power on reset delay time.

7 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

7.1 General

The IFX80471 step-down DC-DC controllers are designed primarily for use in industrial applications and offer a large flexibility in the input voltage range they can handle. Using an external P-MOSFET and current-sense resistor allows design flexibility and the improved efficiencies associated with high-performance P-channel MOSFETs. The unique, peak current-limited, PWM/PFM control scheme gives these devices excellent efficiency over wide load ranges, while drawing around 100µA current from the battery under no load condition. This wide dynamic range optimizes the IFX80471 for applications, where load currents can vary considerably as individual circuit blocks are turned on and off to conserve energy. Operation to a 100% duty cycle allows the lowest possible dropout voltage, maintaining operation during cold cranking. High switching frequencies and a simple circuit topology minimize PC board area and component costs.

7.2 Output voltage at adjustable version - feedback divider

The output voltage is sensed either by an internal voltage divider connected to the VOUT pin (IFX80471SKV50, fixed 5V version) or an external divider from the Buck output voltage to the FB pin (IFX80471SKV, adjustable version). The Vout pin has to be connected always to the Buck converter output regardless which output voltage for the adjustable version is desired.

To determine the resistors of the feedback divider for the desired output voltage V_{OUT} at the IFX80471SKV select R_{FB2} between 5kΩ and 500kΩ and obtain R_{FB1} with the following formula:

$$R_{FB1} = R_{FB2} \cdot \left(\frac{V_{OUT}}{V_{FB,\,th}} - 1 \right)$$

V_{FB} is the threshold of the error amplifier with its value of typical 1.25V which shows that the output voltage can be adjusted in a range from 1.25V to 15V. However the integrated Reset function will only be operational if the output voltage level is adjusted to >7V.
Also the current consumption will be increased in PFM mode in the range between
1.25V and 7V.

7.3 SI_Enable

Connecting SI_ENABLE to 5V causes SI_GND to have low impedance. Thus the SI comparator is in operation and can be used to monitor the battery voltage. SO output signal is valid. Connecting SI_ENABLE to GND causes SI_GND to have high impedance. Thus the SI comparator is not able to monitor the battery voltage. SO output signal is invalid.

7.3.1 Battery sense comparator - voltage divider

The formula to calculate the resistor divider for the sense comparator is basically the same as for the feedback divider in section before. With the selected resistor R_{SI2}, the desired threshold of the input voltage $V_{IN, UV}$ and the lower sense threshold $V_{SI, low}$ the resistor R_{SI1} is given to:

$$R_{SI1} = R_{SI2} \cdot \left(\frac{V_{IN, UV}}{V_{SI, low}} - 1 \right)$$

For high accuracy and low ohmic resistor divider values the on-resistance of the SI_GND NMOS (typ. 100Ω) has to be added to R_{SI2}.

7.4 Undervoltage reset - delay time

The diagram below shows the typical behavior of the reset output in dependency on the input voltage V_{IN}, the output voltage V_{VOUT} or V_{FB}.

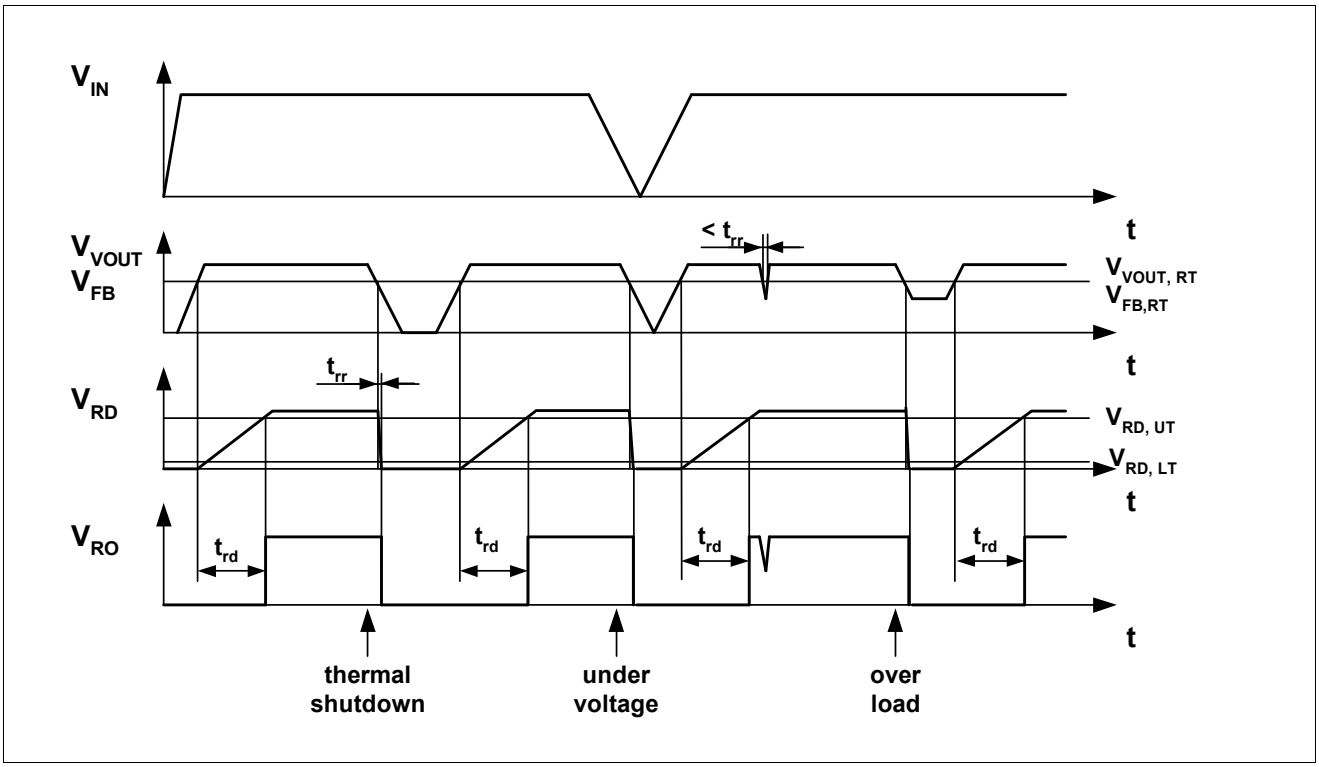


Figure 4 Reset timing

7.5 100% duty-cycle operation and dropout

The IFX80471 operates with a duty cycle up to 100%. This feature allows to operate with the lowest possible drop voltage at low battery voltage as it occurs at cold cranking. The MOSFET is turned on continuously when the supply voltage approaches the output voltage level, conventional switching regulators with less than 100% duty cycle would fail in that case.

The drop- or dropout voltage is defined as the difference between the input and output voltage levels when the input is low enough to drop the output out of regulation. Dropout depends on the MOSFET drain-to-source on-resistance, the current-sense resistor and the inductor series resistance. It is proportional to the load current:

$$V_{drop} = I_{LOAD} \cdot (R_{DS(ON)PMOS} + R_{SENSE} + R_{INDUCTANCE})$$

7.6 SYNC Input and Frequency Control

The IFX80471's internal oscillator is set for a fixed PWM switching frequency of 360kHz or can be synchronized to an external clock at the SYNC pin. When the internal clock is used SYNC has to be connected to GND. SYNC is a negative-edge triggered input that allows synchronization to an external frequency ranging between 270kHz and 530kHz. When SYNC is clocked by an external signal, the converter operates in PWM mode until the load current drops below the PWM to PFM threshold. Thereafter the converter continues operation in PFM mode.

7.7 Shutdown Mode

Connecting ENABLE to GND places the IFX80471SKV in shutdown mode. In shutdown, the reference, control circuitry, external switching MOSFET, and the oscillator are turned off and the output falls to 0V. Connect ENABLE to voltages higher than 4.5V for normal operation. As this input operates analogue way the voltage applied at this pin should have a slope of 0.5V/3µs as a minimum requirement to avoid undefined states within the device.

7.8 Buck converter circuit

A typical choice of external components for the buck converter circuit is given in **Figure 5** and **Figure 6**. For basic operation of the buck converter the input capacitors C_{IN1}, C_{IN2}, the driver supply capacitor C_{BDS}, the sense resistor R_{SENSE}, the PMOS device, the catch diode D1, the inductance L1 and the output capacitor C_{OUT} are necessary. In addition for low electromagnetic emission a Pi-filter at the input and/or a small resistor in the path between GDRV and the gate of the PMOS may be necessary.

7.8.1 Buck inductance (L1) selection in terms of ripple current

The internal PWM/PFM control loop includes a slope compensation for stable operation in PWM mode. This slope compensation is optimized for inductance values of 47µH and Sense resistor values of 47mΩ for the 5V output voltage versions. When choosing an inductance different from 47µH the Sense resistor has to be changed also:

$$\frac{R_{SENSE}}{L1} = (0{,}5 \ldots 1{,}0) \times 10^3 \frac{\Omega}{H}$$

Increasing this ratio above 1000 Ω/H may result in sub harmonic oscillations as well-known for peak current mode regulators without integrated slope compensation.

To achieve the same effect of slope compensation in the adjustable voltage version also the inductance in µH is given by

$$\left(2{,}0 \times 10^{-4} \cdot \frac{H}{V\Omega} \cdot V_{OUT} \cdot R_{SENSE}\right) < L1 < \left(4{,}0 \times 10^{-4} \cdot \frac{H}{V\Omega} \cdot V_{OUT} \cdot R_{SENSE}\right)$$

The inductance value determines together with the input voltage, the output voltage and the switching frequency the current ripple which occurs during normal operation of the step down converter. This current ripple is important for the all over ripple at the output of the switching converter.

$$\Delta I = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{f_{SW} \cdot V_{IN} \cdot L1}$$

In this equation f_{sw} is the actual switching frequency of the device, given either by the internal oscillator or by an external source connected to the SYNC pin. When picking finally the inductance of a certain supplier (Epcos, Coilcraft etc.) the saturation current has to be considered. The saturation current value of the desired inductance has to be higher than the maximum peak current which can appear in the actual application.

7.8.2 Determining the current limit

The peak current which the buck converter is able to provide is determined by the peak current limit threshold voltage V_{LIM} and the sense resistor R_{SENSE}. With a maximum peak current given by the application ($I_{PEAK, PWM}$=I_{LOAD}+0.5ΔI) the sense resistor is calculated to

$$R_{SENSE} = \frac{V_{LIM}}{2 \cdot I_{PEAK, PWM}}$$

The equation above takes account for the foldback characteristic of the current limit as shown in the figures 'Output Voltage versus Load Current' on page 17/18 by introducing a factor of 2. It must be assured by correct dimensioning of R_{SENSE} that the load current doesn't reach the foldback part of the characteristic curve.

7.8.3 PFM and PWM thresholds

The crossover thresholds PFM to PWM and vice versa strongly depend on the input voltage V_{IN}, the Buck converter inductance L1, the sense resistor value R_{SENSE} and the turn on and turn off delays of the external PMOS.

7.8.4 Buck output capacitor (C_{OUT}) selection:

The choice of the output capacitor effects straight to the minimum achievable ripple which is seen at the output of the buck converter. In continuous conduction mode the ripple of the output voltage can be estimated by the following equation:

$$V_{Ripple} = \Delta I \cdot \left(R_{ESRCOUT} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right)$$

From the formula it is recognized that the ESR has a big influence in the total ripple at the output, so low ESR tantalum or ceramic capacitors are recommended for the application (recommended range: 50mOhm to 150mOhm).

One other important thing to note are the requirements for the resonant frequency of the output LC-combination. The choice of the components L and C have to meet also the specified range given in **Chapter 4.2** otherwise instabilities of the regulation loop might occur.

7.8.5 Input capacitor (C_{IN1}) selection:

At high load currents, where the current through the inductance flows continuously, the input capacitor is exposed to a square wave current with its duty cycle V_{OUT}/V_I. To prevent a high ripple to the battery line a capacitor with low ESR should be used. The maximum RMS current which the capacitor has to withstand is calculated to:

$$I_{RMS} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}}} \cdot \sqrt{1 + \frac{1}{3} \cdot \left(\frac{\Delta I}{2 \cdot I_{LOAD}}\right)^2}$$

For low ESR an e.g. Al-electrolytic capacitance in parallel to an ceramic capacitance could be used.

7.8.6 Freewheeling diode / catch diode (D1)

For lowest power loss in the freewheeling path Schottky diodes are recommended. With those types the reverse recovery charge is negligible and a fast hand over from freewheeling to forward conduction mode is possible. Depending on the application (12V battery systems) 40V types could be also used instead of the 60V diodes. Also for high temperature operation select a Schottky-diode with low reverse leakage.

A fast recovery diode with recovery times in the range of 30ns can be also used if smaller junction capacitance values (smaller spikes) are desired.

7.8.7 Buck driver supply capacitor (C_{BDS})

The voltage at the ceramic capacitor is clamped internally to 7V, a ceramic type with a minimum of 220nF and voltage class 16V would be sufficient.

7.8.8 Input pi-filter components for reduced EME

At the input of Buck converters a square wave current is observed causing electromagnetic interference on the battery line. The emission to the battery line consists on one hand of components of the switching frequency (fundamental wave) and its harmonics and on the other hand of the high frequency components derived from the current slope. For proper attenuation of those interferers a π-type input filter structure is recommended which is built up with inductive and capacitive components in addition to the Input caps C_{IN1} and C_{IN2}. The inductance can be chosen up to the value of the Buck converter inductance, higher values might not be necessary, the additional capacitance should be a ceramic type in the range up to 100nF.

Inexpensive input filters show due to their parasitics a notch filter characteristic, which means basically that the low pass filter acts from a certain frequency as a high pass filter and means further that the high frequency components are not attenuated properly. To slower down the slopes at the gate of the PMOS switch and get down the emission in the high frequency range a small gate resistor can be put between GDRV and the PMOS gate.

7.8.9 Frequency compensation

The external frequency compensation pin should be connected via a 22nF ($\geq$10V) ceramic capacitor and a 430 Ω (1/8W) resistor to GND. This node should be kept free from switching noise.

7.9 Components recommendation - Overview

Device	Values / Remarks
C_{IN1}	100µF, 60V
C_{IN2}	220nF, 60V
L1	47µH, 1.6A, 145mΩ
	47µH, 3.5A, 47mΩ
	47µH, 3.8A, 110mΩ
	68µH, 3.5A, 130mΩ
	47µH, 4.0A, 97mΩ
M1	60V, 3.44A, 130mΩ, NL
	60V, 2.9A, 130mΩ, NL
	60V, 9A, 250mΩ, LL
C_{BDS}	220nF, 16V
D1	Schottky, 60V, 3A
	Schottky, 40V, 3A
	Schottky, 40V, 3A
C_{OUT}	Low ESR Tantalum, 100µF, 10V
C_{COMP}	see 7.8.9.

7.10 Layout recommendation

The most sensitive points for Buck converters - when considering the layout - are the nodes at the input, output and the gate of the PMOS transistor and the feedback path.

For proper operation and to avoid stray inductance paths the external catch diode, the Buck inductance and the input capacitor C_{IN1} have to be connected as close as possible to the PMOS device. Also the GDRV path from the controller to the MOSFET has to be as short as possible. Best suitable for the connection of the cathode of the catch diode and one terminal of the inductance would be a small plain located next to the drain of the PMOS.

The GND connection of the catch diode must be also as short as possible. In general the GND level should be implemented as surface area over the whole PCB as second layer, if necessary as third layer. The feedback path has to be well grounded also, a ceramic capacitance might help in addition to the output cap to avoid spikes.

To obtain the optimum filter capability of the input pi-filter it has to be located also as close as possible to the input. To filter the supply input of the device (VS) the ceramic cap should be connected directly to the pin.

As a guideline an EMC optimized application board / layout is available.

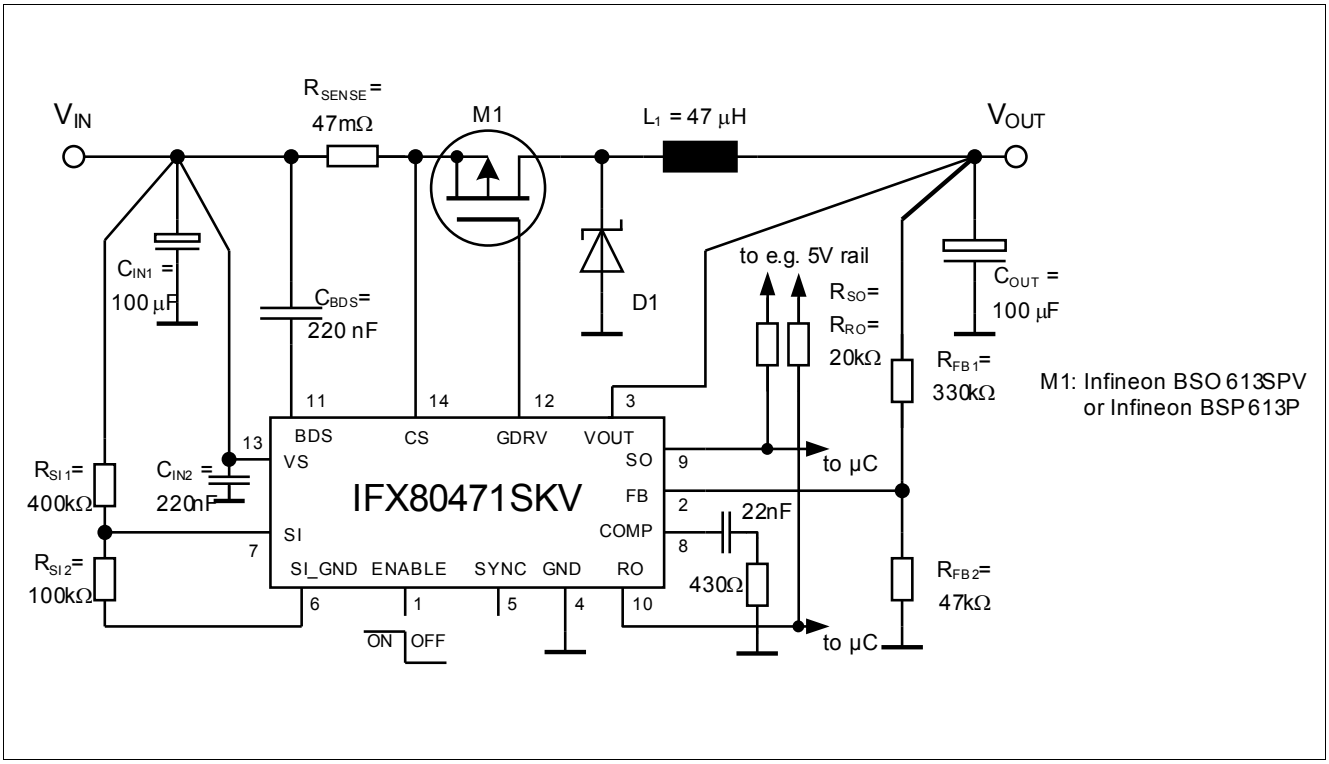


Figure 5 Application Diagram circuit IFX80471SKV

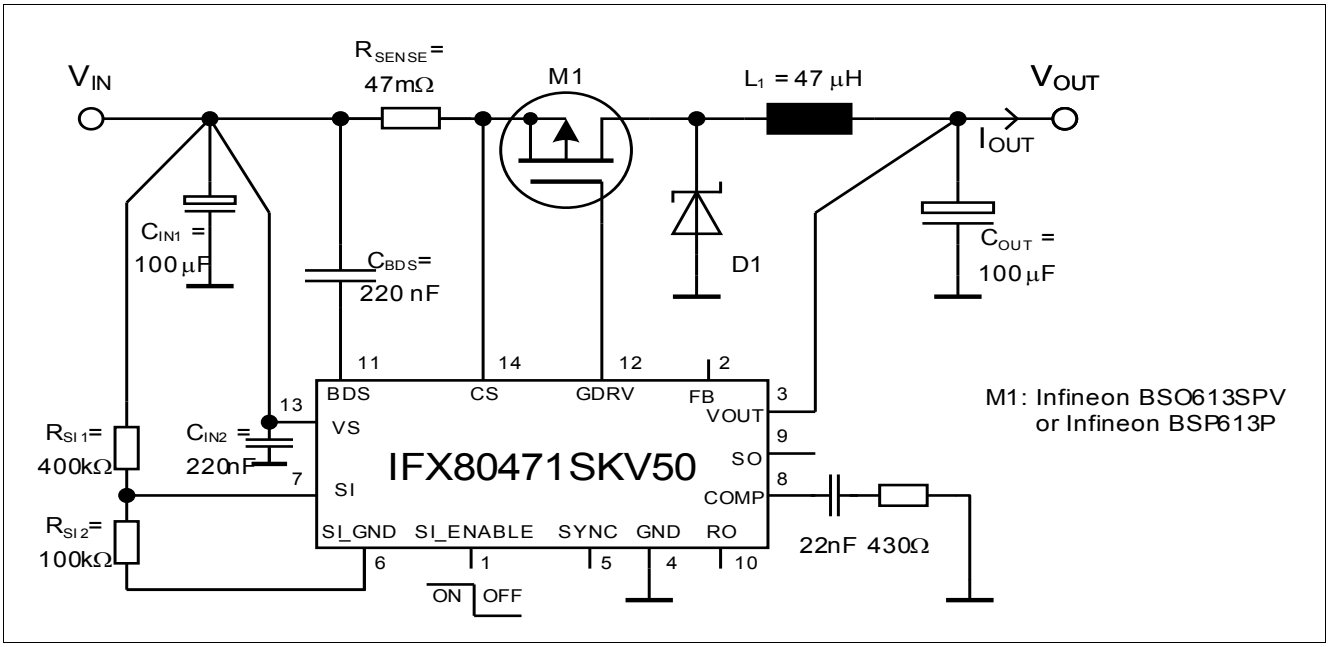


Figure 6 Application Diagram circuit IFX80471SKV50

Note: This is a very simplified example of an application circuit. The function must be verified in the real application.

8 Package Outlines

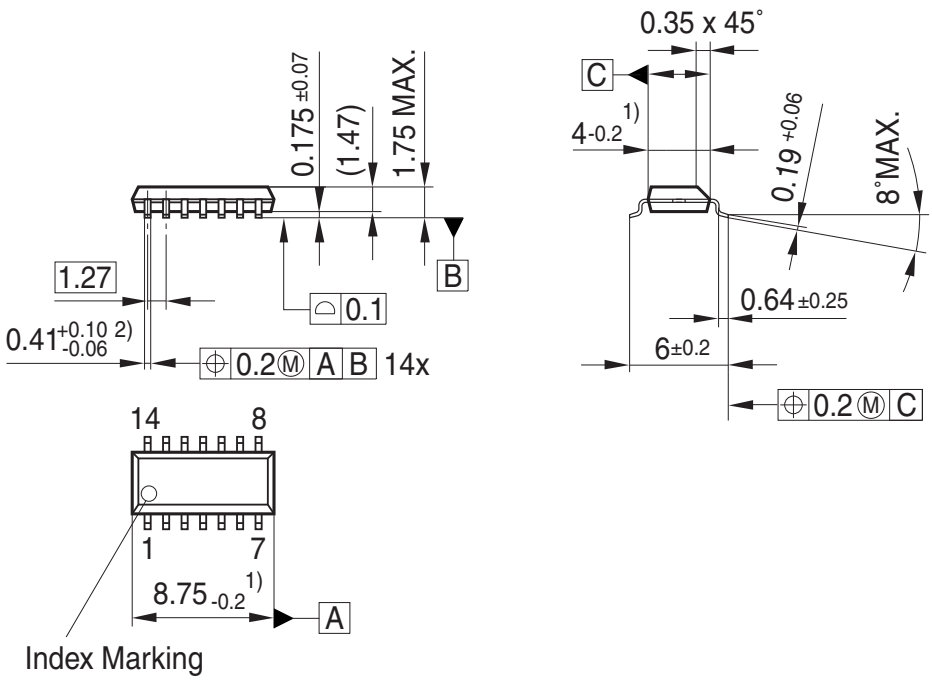


Figure 7 PG-DSO-14

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

9 Revision History

Revision	Date	Changes
1.0	2011-02-07	Data Sheet - Initial Release

Edition 2011-02-07

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

单击下面可查看定价，库存，交付和生命周期等信息

>>Infineon Technologies(英飞凌)

>>点击查看相关商品