TLE7181EM

H-Bridge and Dual Half Bridge Driver IC

Automotive Power

Never stop thinking

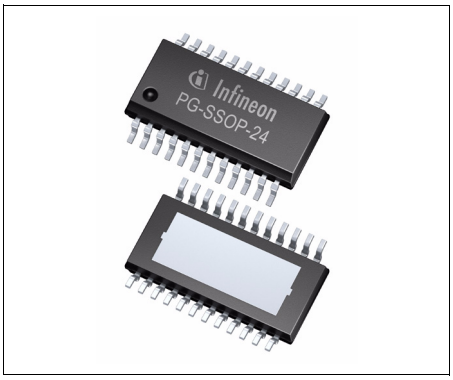
Table of Contents

H-Bridge and Dual Half Bridge Driver IC

AEC Qualified

RoHS

1 Overview



PG-SSOP-24

Features

- PWM/DIR-interface drives 4 N-Channel Power MOSFETs
- Unlimited D.C. switch on time of Low and Highside MOSFETs
- 0 …95% at 20kHz & 100% Duty cycle of High Side MOSFETs
- 0 ... 100 % Duty cycle of Low Side MOSFETs
- Additional output to drive a reverse polarity protection N-MOSFET
- Current sense OPAMP
- Low quiescent current mode
- Internal shoot through protection
- Adjustable dead time
- 1 bit diagnosis / $\overline{\text{ERR}}$
- Over current warning based on current sense OPAMP with fixed warning level
- Analog adjustable Short Circuit Protection levels via SCDL pin with open pin detection
- Over temperature warning
- Over voltage warning
- Under voltage warning and shutdown
- Green Product (RoHS compliant)
- AEC Qualified

Description

The TLE7181EM is a H-bridge driver IC dedicated to control 4 N-channel MOSFETs typically forming the converter for a high current DC motor drives in the automotive sector. It incorporates several protection features such as over current and short circuit detection as well as under-, over voltage and over temperature diagnosis.

Typical applications are fans, pumps and electric power steering. The TLE7181EM is designed for a 12V power net.

Table 1 Product Summary

Specified operating voltage	V_{SOP}	7.0 V … 34 V
Junction temperature	T_j	-40 °C .. 150°C
Maximum output source resistance	R_{Sou}	13.5 Ω
Maximum output sink resistance	R_{Sink}	9 Ω
maximum quiescent current[1)]	I_{QVS}	8 µA

1) typical value at T_j=25°CC

Type	Package	Marking
TLE7181EM	PG-SSOP-24	TLE7181EM

2 Block Diagram

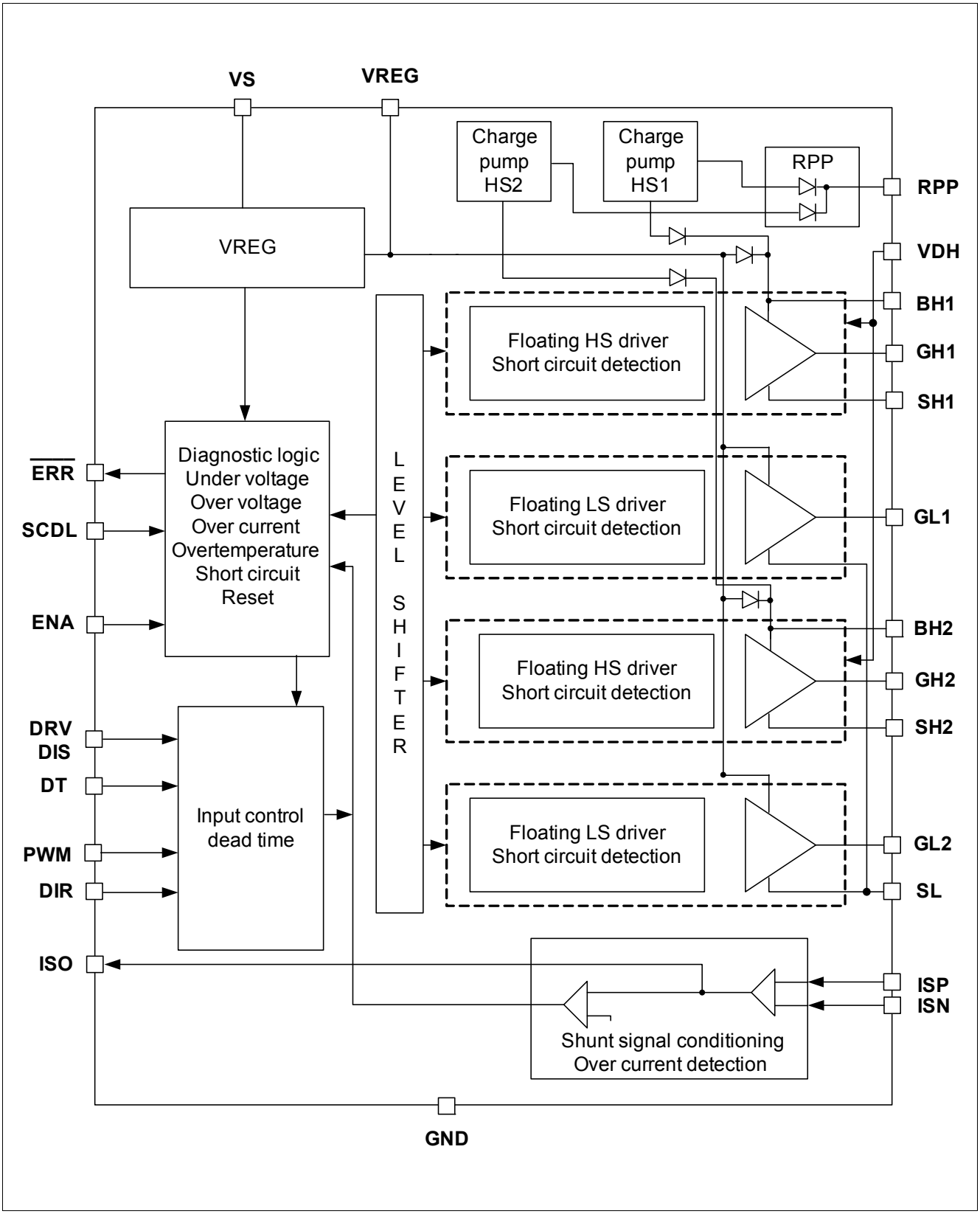


Figure 1 Block diagram TLE7181EM

3 Pin Configuration

3.1 Pin Assignment

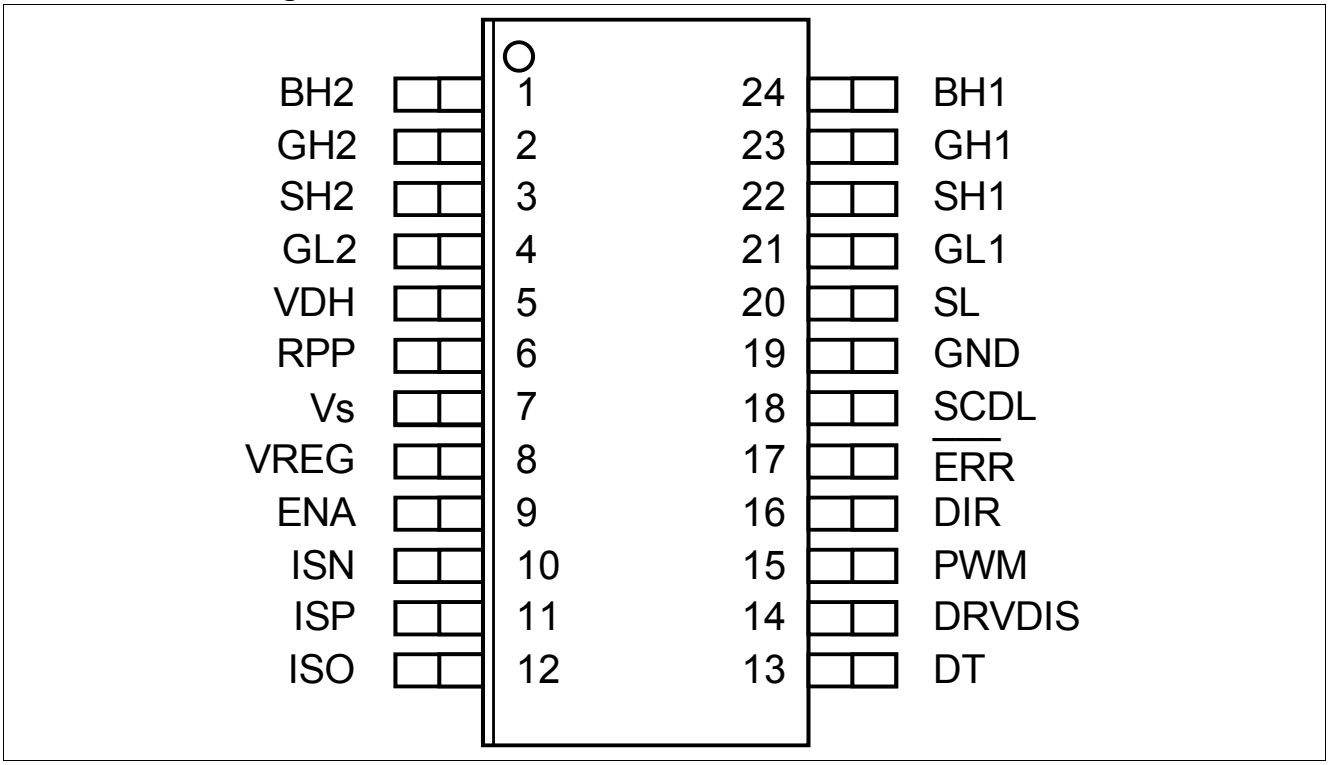


Figure 2 Pin Configuration

3.2 Pin Definitions and Functions

# of Pins	Symbol	Function
1	BH2	Pin for + terminal of the bootstrap capacitor of phase 2
2	GH2	Output pin for gate of high side MOSFET 2
3	SH2	Pin for source connection of high side MOSFET 2
4	GL2	Output pin for gate of low side MOSFET 2
5	VDH	Voltage input common drain high side for short circuit detection
6	RPP	charge pump output for reverse polarity protection of the motor bridge
7	VS	Pin for supply voltage
8	VREG	Output of supply for driver output stage - connect to a capacitor
9	ENA	Input pin for reset of $\overline{\text{ERR}}$ registers, active switch off of external MOSFETs and low quiescent current mode, set HIGH to enable operation
10	ISN	Input for OPAMP + terminal
11	ISP	Input for OPAMP - terminal
12	ISO	Output of OPAMP
13	DT	Input for adjustable dead time function, connect to GND via resistor
14	DRVDIS	Disable DIR/PWM interface & all output stages switched off
15	PWM	control input for PWM frequency and duty cycle
16	DIR	control input for spinning direction of the motor

# of Pins	Symbol	Function
17	$\overline{\text{ERR}}$	Push pull output stage
18	SCDL	Input pin for adjustable Short Circuit Detection function
19	GND	Ground pin
20	SL	Pin for common source of lowside MOSFETs
21	GL1	Output pin for gate of low side MOSFET 1
22	SH1	Pin for source connection of high side MOSFET 1
23	GH1	Output pin for gate of high side MOSFET 1
24	BH1	Pin for + terminal of the bootstrap capacitor of phase 1
Tab	Tab	should be connected to GND

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltages						
4.1.1	Supply voltage at VS	V_{VS}	-0.3	45	V	–
4.1.2	Supply voltage at VS	V_{VSRP}	-4.0	45	V	R_{VS}≥10Ω
4.1.3	Voltage range at VDH	V_{VDH}	-0.3	55	V	–
4.1.4	Voltage range at RPP	V_{RPP}	-0.3	55	V	–
4.1.5	maximum current at RPP	I_{RPP}	-25	25	mA	–
4.1.6	Voltage range at ENA	V_{ENA}	-0.3	45	V	–
4.1.7	Voltage range at SCDL	V_{SCDL}	-0.3	6	V	–
4.1.8	Voltage range at PWM, DIR, DT, DRVDIS	V_{DPI}	-0.3	6	V	–
4.1.9	Voltage range at $\overline{\text{ERR}}$, ISO	V_{DPO}	-0.3	6	V	–
4.1.10	Voltage range at ISP, ISN	V_{OPI}	-5.0	5.0	V	–
4.1.11	Voltage range at VREG	V_{VREG}	-0.3	15	V	–
4.1.12	Voltage range at BHx	V_{BH}	-0.3	55	V	–
4.1.13	Voltage range at GHx	V_{GH}	-0.3	55	V	–
4.1.14	Voltage range at GHx	V_{GHP}	-7.0	55	V	t_P<1µs; f=50kHz
4.1.15	Voltage range at SHx	V_{SH}	-2.0	45	V	–
4.1.16	Voltage range at SHx	V_{SHP}	-7.0	45	V	t_P<1µs; f=50kHz
4.1.17	Voltage range at GLx	V_{GL}	-0.3	18	V	–
4.1.18	Voltage range at GLx	V_{GLP}	-7.0	18	V	t_P<0.5µs; f=50kHz
4.1.19	Voltage range at SL	V_{SL}	-1.0	5.0	V	–
4.1.20	Voltage range at SL	V_{SLP}	-7.0	5.0	V	t_P<0.5µs; f=50kHz; C_{BS}≥330nF
4.1.21	Voltage difference Gxx-Sxx	V_{GS}	-0.3	15	V	–
4.1.22	Voltage difference BHx-SHx	V_{BS}	-0.3	15	V	–
Temperatures						
4.1.23	Junction temperature	T_j	-40	150	°C	–
4.1.24	Storage temperature	T_{stg}	-55	150	°C	–
4.1.25	Lead soldering temperature (1/16'' from body)	T_{sol}	–	260	°C	–
4.1.26	Peak reflow soldering temperature[2)]	T_{ref}	–	260	°C	–
Power Dissipation						
4.1.27	Power Dissipation (DC)	P_{tot}	–	2	W	–

Absolute Maximum Ratings (cont'd)[1)]

40 °C ≤ T_j ≤ 150 °C; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
ESD Susceptibility						
4.1.28	ESD Resistivity[3)]	V_{ESD}	–	2	kV	
4.1.29	CDM	V_{CDM}	–	1	kV	

1) Not subject to production test, specified by design.
2) Reflow profile IPC/JEDEC J-STD-020C
3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Specified supply voltage range	V_{VS1}	7.0	34	V	–
4.2.2	supply voltage range[1)]	V_{VS2}	5.5	45	V	V_{VS}<7V reduced functionality
4.2.3	Quiescent current at VS	I_{QVS1}	–	8	µA	V_{VS},V_{VDH}=12V; ENA=Low; T_j=25°C
4.2.4	Quiescent current at VS	I_{QVS2}	–	10	µA	V_{VS},V_{VDH}<15V; ENA=Low; T_j≤85°C
4.2.5	Quiescent current at VDH	I_{QVDH1}	–	8	µA	V_{VS},V_{VDH}=12V; ENA=Low; T_j=25°C
4.2.6	Quiescent current at VDH	I_{QVDH2}	–	10	µA	V_{VS},V_{VDH}<15V; ENA=Low; T_j≤85°C
4.2.7	Supply current at Vs (device enabled)[2)]	$I_{Vs(1)}$	–	22	mA	no switching
4.2.8	Supply current at Vs (device enabled)	$I_{Vs(2)}$	–	45	mA	4xQ_{GS}xf_{PWM}≤20mA ; V_{VS}=7.0..34V
4.2.9	D.C. switch on time of output stages	D_{DC}	–	∞	s	–
4.2.10	Duty cycle Highside output stage[3)]	D_{HS}	0	95	%	f_{PWM}=20kHz; continuous operation; C_{BS} ≥330nF
4.2.11	Duty cycle Lowside output stage	D_{LS}	0	100	%	–

1) operation above 34V limited by max. allowed power dissipation and max. ratings
2) Current can be higher, if driver output stages are unsupplied
3) max. limit of D.C. will increase, if f_{PWM} or external gate charge of the MOSFETs is reduced

The PWM frequency is limited by thermal constraints and the maximum duty cycle (minimum charging time of bootstrap capacitor).

Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case[1)]	R_{thJC}	–	–	5	K/W	–
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	35	–	K/W	[2)]

1) Not subject to production test, specified by design.

2) **Exposed Heatslug Package use this sentence**: Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.4 Default State of Inputs

Table 2 Default State of Inputs (if left open)

Characteristic	State	Remark
Default state of PWM and DIR	Low	Low side MOSFETs off and Highside MOSFETs on
Default state of DT	OPEN	maximum deadtime
Default state of ENA	Low	Output stages disabled device in sleep mode
Default state of SCDL	OPEN	Short circuit detection deactivation & warning
Default state of DRVDIS	High	All output stages off & no error will be reported

5 Description and Electrical Characteristics

5.1 MOSFET Driver

5.1.1 Driving MOSFET Output Stages

The TLE7181EM incorporates 2 high side and low side output stages for 4 external MOSFETs.

The 4 MOSFET output stages will be driven by the PWM/DIR interface. With the PWM/DIR interface only 2 inputs pins are necessary to drive a typical H-bridge topology for a DC-brush motor. The rotation direction of the motor can be chosen with the input pin DIR. The speed of the motor can is controlled by applying a PWM-signal at pin PWM.

The DRVDIS pin allows to switch off all 4 MOSFETs. **Table 3** provides an overview of the different states with this interface.

Table 3 PWM/DIR interface normal operation

DRVDIS	DIR	PWM	Highside switch1	Lowside switch1	Highside switch2	Lowside switch2
0	0	0	ON	OFF	ON	OFF
0	0	1	ON	OFF	OFF	ON
0	1	0	ON	OFF	ON	OFF
0	1	1	OFF	ON	ON	OFF
1	x	x	OFF	OFF	OFF	OFF

5.1.2 MOSFET Output Stages

The six push-pull MOSFET driver stages of the TLE7181EM are realized as separate floating blocks. This means that the output stage is follows the individual MOSFET source voltages and so ensuring stable MOSFET driving even in harsh electrical environment.

All 4 output stages have the same output power and thanks to the used bootstrap principle they can be switched all up to high frequencies.

Each output stage has its own short circuit detection block. For more details about short circuit detection see **Chapter 5.2.2**.

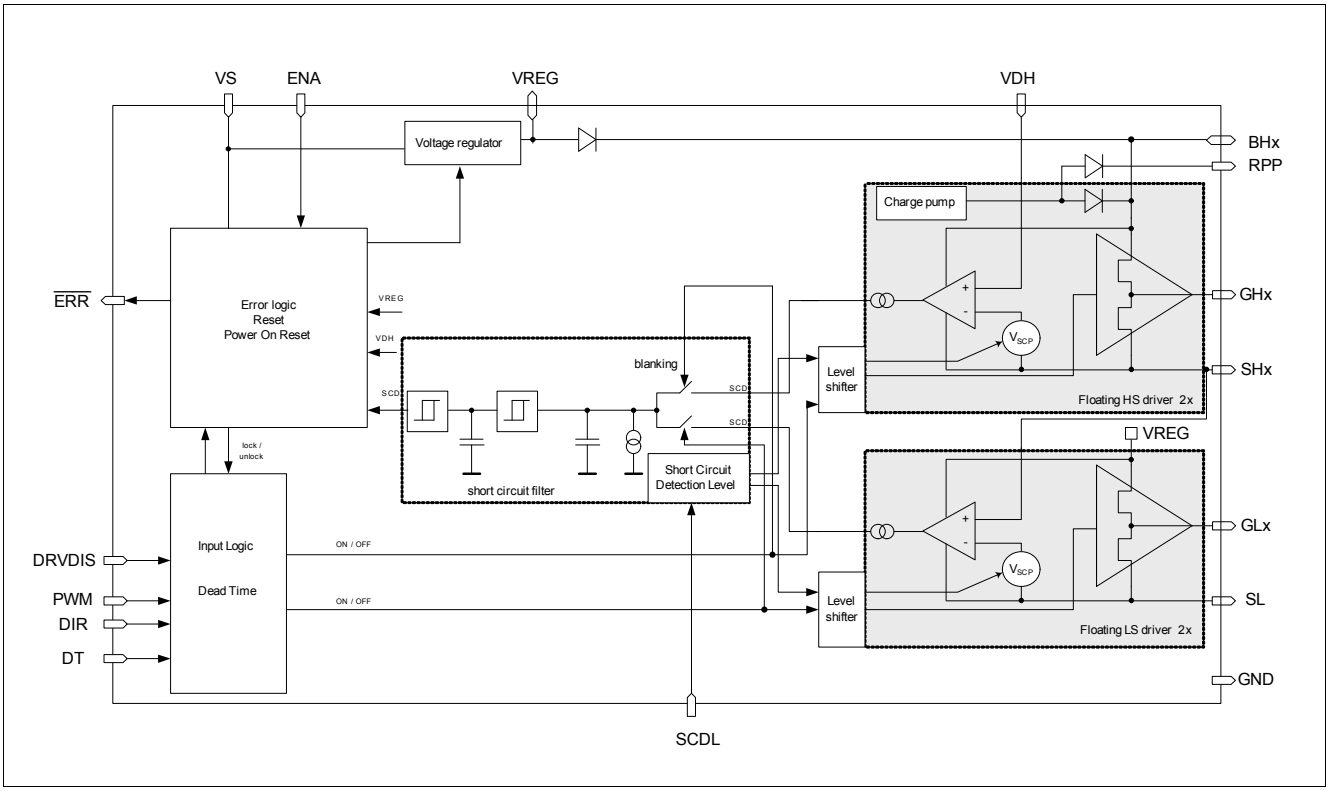


Figure 3 Block Diagram of Driver Stages including Short Circuit Detection

5.1.3 Dead Time

In bridge applications it has to be assured that the external high side and low side MOSFETs are not “on” at the same time, connecting directly the battery voltage to GND. The dead time generated in the TLE7181EM can be programmed by applying an resistor between the DT pin and GND. Higher external resistor values lead to higher dead time.

A minimum dead time applied, if the DT pin is connected to GND.

The typical dead time can be calculated with the following formula:

$$t_{deadtime}[\mu s] = \frac{0.081}{0.02 + {}^{2.4}\!/_{4+Rdt[k\Omega]}}$$

If an exact dead time of the bridge is needed, the use of the µC PWM generation unit is recommended.

5.1.4 Bootstrap Principle

The TLE7181EM provides a bootstrap based supply for its high side output stages.

The bootstrap capacitors are charged by switching on the external low side MOSFETs, connecting the bootstrap capacitor to GND. Under this condition the bootstrap capacitor will be charged from the VREG capacitor via the integrated bootstrap diode. If the low side MOSFET is switched off and the high side MOSFET is switched on, the bootstrap capacitor will float together with the SHx voltage to the supply voltage of the bridge. Under this condition the supply current of the high side output stage will discharge the bootstrap capacitor. This current is specified. The size of the capacitor together with this current will determine how long the high side MOSFET can be kept on without recharging the bootstrap capacitor.

5.1.5 100% D.C. charge pumps

100% D.C. charge pumps are implemented for each high side output stage. Therefore the high side output stages can be switch on for an unlimited time. These integrated charge pumps can handle leakage currents which will be caused by external MOSFETs and the TLE7181EM itself. They are not strong enough to drive a 99% duty cycle for a longer time. the charge pumps are running when the driver is not in sleep mode and assure that the bootstrap capacitors are charged as long as the user does not apply critical duty cycle for a longer time.

5.1.6 Reverse polarity protection of motor bridge

The TLE7181EM provides an additional RPP pin to protect motor bridge for reverse polarity. This RPP pin can drive an additional external N-channel power MOSFET designed in between battery and the motor bridge. The RPP pin is internally supplied by the two integrated 100% D.C. charge pumps. They are especially designed to handle additional current which is needed to drive a the gate charge of the reverse polarity MOSFET. The guarantied output current of the charge pumps is specified.

5.1.7 Sleep mode

If ENA pin is set to low, the ERR flag will be set to low and the output stages will be switched off.

After ENA pin is kept low for t_{LQM} the sleep mode of the Driver IC will be activated.

In Sleep mode the complete chip is deactivated. This means the internal supply structure of the TLE7181EM will be switched off. This mode is designed for lowest current consumption from the power net of the car. The passive clamping is active. For details see the description of passive clamping, see **Chapter 5.2.9**.

The TLE7181EM will wake up, if ENA is set to high.The ENA pin is 45V compatible, so ENA can be directly be connected to the ignition key signal KL15.

5.1.8 Wake up

A special start up procedure is implemented into the TLE7181EM to guarantee charged bootstrap capacitors.

This start up procedure is automatically performed before normal H-bridge motor control with PWM/DIR is possible.

If the ENA pin is set to high, the VREG voltage starts to increase. As soon as the under voltage threshold VREG_UV is reached, both low side output stages will be switched on for a short period of time for fast charging of the bootstrap capacitors. When the bootstrap capacitor voltage is high enough the auto start up procedure is completed and the low side MOSFETs will be driven accoring the input pattern.

During wake up procedure the ERR signal is set to low. It will be set to high, if no error occurs at the TLE7181EM and auto start procedure is completed.

To assure that the driver is finally in the normal operation mode, it is recommended to set the DRVDIS pin to high for minimum 1us. After that procedure the output stages can be driven by PWM/DIR interface.

5.1.9 Electrical Characteristics

Electrical Characteristics MOSFET Drivers

V_S = 7.0 to 34V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Control inputs							
5.1.1	Low level input voltage of PWM; DIR	V_{I_LL}	–	–	1.0	V	–
5.1.2	High level input voltage of PWM; DIR	V_{I_HL}	2.0	–	–	V	–
5.1.3	Input hysteresis of PWM; DIR	d_{VI}	100	200	–	mV	–
5.1.4	PWM; DIR pull-down resistors to GND	R_{IL}	20	–	50	kΩ	–
5.1.5	Low level input voltage of ENA	V_{E_LL}	–	–	0.75	V	–
5.1.6	High level input voltage of ENA	V_{E_HL}	2.1	–	–	V	–
5.1.7	Input hysteresis of ENA	d_{VE}	50	200	–	mV	–
5.1.8	ENA pull-down resistor to GND	R_{IL}	70	125	200	kΩ	–
5.1.9	Low level input voltage of DRVDIS	V_{D_LL}	–	–	1.0	V	–
5.1.10	High level input voltage of DRVDIS	V_{D_HL}	2.0	–	–	V	–
5.1.11	Input hysteresis of DRVDIS	d_{VD}	100	200	–	mV	–
5.1.12	DRVDIS pull-up resistor to internal supply	R_{DH}	30	50	80	kΩ	–
MOSFET driver output							
5.1.13	Output source resistance	R_{Sou}	2	–	13.5	Ω	I_{Load}=-20mA
5.1.14	Output sink resistance	R_{Sink}	2	–	9.0	Ω	I_{Load}=20mA
5.1.15	High level output voltage Gxx vs. Sxx	V_{Gxx1}	–	11	15	V	13.5V≤V_{VS}≤34V; I_{Load}=0mA
5.1.16	High level output voltage Gxx vs. Sxx	V_{Gxx2}	–	11	13.5	V	13.5V≤V_{VS}≤34V; C_{Load}=20nF; D.C.=50%; f_{PWM}=20kHz
5.1.17	High level output voltage GHx vs. SHx[1)]	V_{GHx3}	–	V_{VS}-1.5	–	V	7.0V<V_{VS}<13.5V; C_{Load}=20nF; D.C.=50%; f_{PWM}=20kHz
5.1.18	High level output voltage GLx vs. GND[1)]	V_{GLx3}	–	V_{VS}-0.5	–	V	7.0V<V_{VS}<13.5V; C_{Load}=20nF; f_{PWM}=20kHz & D.C.=50%; or D.C=100%

Electrical Characteristics MOSFET Drivers

V_S = 7.0 to 34V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.1.19	High level output voltage GHx vs. SHx[1)2)]	V_{GHx4}	5.0 + V_{diode}	–	–	V	V_{VS}=7.0V; C_{Load}=20nF; D.C.=95%; f_{PWM}=20kHz; passive freewheeling
5.1.20	High level output voltage GHx vs. SHx[1)]	V_{GHx5}	5.0	–	–	V	V_{VS}=7.0V; C_{Load}=20nF; D.C.=95%; f_{PWM}=20kHz
5.1.21	High level output voltage GLx vs. SLx[1)]	V_{GLx5}	6.0	–	–	V	V_{VS}=7.0V; C_{Load}=20nF; D.C.=95%; f_{PWM}=20kHz
5.1.22	High level output voltage GHx vs. SHx[1)]	V_{GHx5}	10	–	–	V	7.0V≤V_{VS}≤13.5V; C_{Load}=20nF; D.C.=100%
5.1.23	High level output voltage GLx vs. SLx[1)]	V_{GLx5}	6.5	–	–	V	V_{VS}=7.0V; C_{Load}=20nF; D.C.=100%
5.1.24	Rise time	t_{rise}	–	250	–	ns	C_{Load}=11nF; R_{Load}=1Ω; V_{VS}=7V; 20-80%
5.1.25	Fall time	t_{fall}	–	200	–	ns	
5.1.26	High level output voltage (in passive clamping)[1)]	V_{GxxUV}	–	–	1.2	V	Sleep mode or VS_UVLO
5.1.27	Pull-down resistor at BHx to GND	R_{BHUVx}	–	–	85	kΩ	Sleep mode or VS_UVLO
5.1.28	Pull-down resistor at VREG to GND	R_{VRUV}	–	–	30	kΩ	Sleep mode or VS_UVLO
5.1.29	Bias current into BHx	I_{BHx}	–	–	150	µA	V_{CBS}>5V; no switching
5.1.30	Bias current out of SHx	I_{SHx}	–	40	–	µA	V_{SHx}=V_{SL}; ENA=HIGH; affected highside output stage static on; V_{CBS}>5V
5.1.31	Bias current out of SL	I_{SL}	–	–	1.4	mA	0≤V_{SHx}≤V_{VS}+1V; ENA=HIGH; no switching; V_{CBS}>5V

Electrical Characteristics MOSFET Drivers

V_S = 7.0 to 34V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Dead time & input propagation delay times							
5.1.32	Programmable internal dead time	t_{DT}	0.08 0.25 0.82 1.0 2.0	0.13 0.42 1,21 1.88 3.62	0.20 0.57 1.65 2.7 5.6	µs	R_{DT}=0kΩ R_{DT}=10kΩ R_{DT}=47kΩ R_{DT}=100kΩ R_{DT}=1000kΩ
5.1.33	Max. internal dead time	t_{DT_MAX}	2.3	4.0	6.4	µs	DT pin open
5.1.34	Dead time deviation between channels	d_{tDT1}	-20	–	20	%	–
			-15	–	15	%	R_{DT}≤47kΩ
5.1.35	Dead time deviation between channels LSoff -> HS on	d_{tDTH1}	-14	–	14	%	–
			-12	–	12	%	R_{DT}≤47kΩ
5.1.36	Dead time deviation between channels HSoff -> LS on	d_{tDTL1}	-14	–	14	%	–
			-12	–	12	%	R_{DT}≤47kΩ
5.1.37	Input propagation time (low on)	$t_{P(ILN)}$	0	100	200	ns	C_{Load}=10nF; R_{Load}=1Ω
5.1.38	Input propagation time (low off)	$t_{P(ILF)}$	0	100	200	ns	
5.1.39	Input propagation time (high on)	$t_{P(IHN)}$	0	100	200	ns	
5.1.40	Input propagation time (high off)	$t_{P(IHF)}$	0	100	200	ns	
5.1.41	Absolute input propagation time difference between above propagation times	$t_{P(diff)}$	–	50	100	ns	
VREG							
5.1.42	VREG output voltage	V_{VREG}	11	12.5	14	V	V_{VS}≥13.5V; I_{Load}=-35mA
5.1.43	VREG over current limitation	$I_{VREGOCL}$	100	–	500	mA	–[3]
5.1.44	Voltage drop between Vs and VREG	V_{VsVREG}	–	–	0.5	V	V_{VS}≥7V; I_{Load}=-35mA; Ron operation
100% D.C. charge pump							
5.1.45	Charge pump frequency[1]	f_{CP}	–	21	–	MHz	–
Motor bridge reverse polarity protection output							
5.1.46	High level output voltage RPP vs. VS	V_{RPP1}	–	11	15	V	I_{Load}=0µA
5.1.47	High level output voltage RPP vs. VS	V_{RPP2}	–	11	12.5	V	I_{Load}≥-30µA
5.1.48	D.C. output current at RPP	I_{RPP1}	–	-110	-150	µA	V_{RPP}≥10V; Lowside on
5.1.49	Rise time[1]	$t_{RPPrise}$	–	1	2	ms	C_{LOAD}=10nF
5.1.50	Rise time[1]	$t_{RPPrise}$	–	10	20	µs	C_{LOAD}=100pF

Electrical Characteristics MOSFET Drivers

V_S = 7.0 to 34V, T_j = -40 to +150°C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
ENA and Low quiescent current mode							
5.1.51	ENA propagation time to output stages switched off	t_{PENA_H-L}	–	2.0	3.0	µs	–
5.1.52	Low time of ENA signal without clearing error register	t_{RST0}	–	–	1.2	µs	–
5.1.53	High time of ENA signal after ENA rising edge for error logic active	t_{RST1}	4	5.75	7	µs	–
5.1.54	go to sleep time	t_{sleep}	310	415	540	µs	–
5.1.55	wake up time	t_{wake}	–	50	100	µs	C_{REG}=2.2µF; C_{BS}=330nF

1) Not subject to production test, specified by design.

2) V_{diode} is the bulk diode of the external low side MOSFET

3) normally no error flag; Error flag might by triggered by under voltage VREG caused by very high load current

5.2 Protection and Diagnostic Functions

5.2.1 State diagram of different operation modes

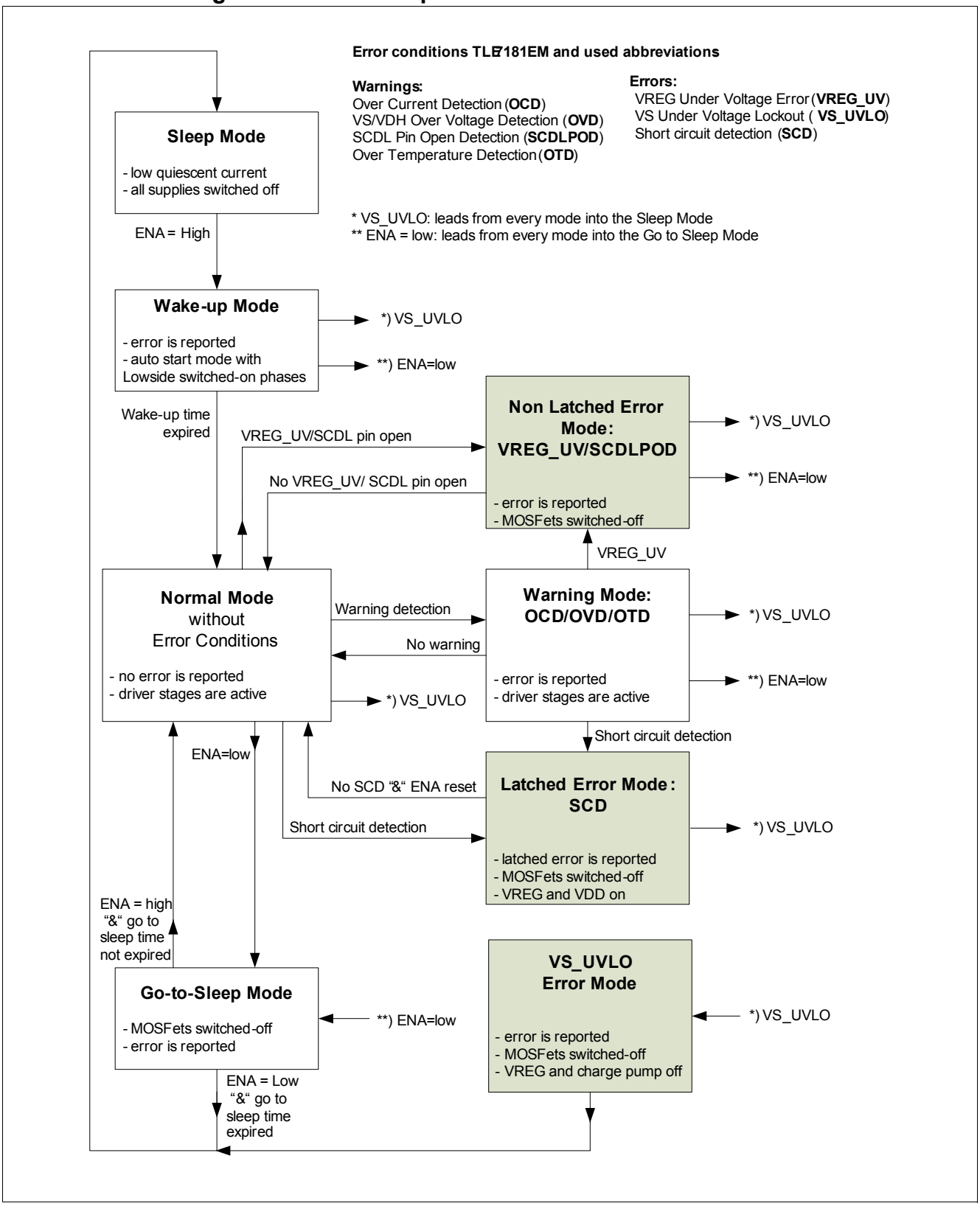


Figure 4 State diagramTLE7181EM

5.2.2 Short Circuit Protection

The TLE7181EM provides a short circuit protection for the external MOSFETs by monitoring the drain-source voltage of the external MOSFETs.

This monitoring of the short circuit detection for a certain external MOSFET is active as soon as the corresponding driver output stage is set to “on” and the dead time and the blanking time are expired.

The blanking time starts when the dead time has expired and assures that the switch on process of the MOSFET is not taken into account. It is recommended to keep the switching times of the MOSFETs below the blanking time.

The short circuit detection level is adjustable in an analog way by the voltage setting at the SCDL pin. There is a 1:1 translation between the voltage applied to the SCDL pin and the drain-source voltage limit. E.g. to trigger the SCD circuit at 1 V drain-source voltage, the SCDL pin must be set to 1 V. The drain-source voltage limit can be chosen between 0.2 ... 2 V.

If after the expiration of the blanking time the drain source voltage of the observed MOSFET is still higher then the SCDL level, the SCD filter time t_{SCP} starts to run. A capacitor is charged with a current. If the capacitor voltage reaches a specific level (filter time t_{SCP}), the error signal is set and the IC goes into SCDL Error Mode. If the SCD condition is removed before the SC is detected, the capacitor is discharged with the same current. The discharging of the capacitor happens as well when the MOSFET is switched off. It has to be considered that the high side and the low side output of one phase are working with the same capacitor.

5.2.3 SCDL Pin Open Detection

An integrated structure at the SCDL pin assures that in case of an open pin the SCDL voltage is pulled to a medium voltage level. The external MOSFETs are actively switched off and an ERR flag is set. This error is self-clearing.

5.2.4 Vs and VDH Over Voltage Warning

The TLE7181EM has an integrated over voltage warning to minimize risk of destruction of the IC at high supply voltages caused by violation of the maximum ratings. For the over voltage warning the voltage is observed at the pin VS and VDH. If the voltage level has reached, the fixed over voltage threshold V_{OVW} for the filter time $t_{OV,}$ a warning at ERR pin is set and TLE7181EM will go in normal operation with warning.

The over voltage warning is self clearing. If the voltage at pin VS and VDH returns into the specified voltage range, the Error register will be cleared and TLE7181EM returns to normal operation mode.

It is the decision of the user, if and how to react on the over voltage warning.

5.2.5 VS Under Voltage Shutdown

The TLE7181EM has an integrated VS Under Voltage Shutdown, to assure that the behavior of the complete IC is predictable in all supply voltage ranges. As soon as the under voltage threshold V_{UVVR} is reached for a specified filter time the TLE7181EM is in VS_UVLO error mode. The error signal will be set and output stages, voltage regulator and charge pump will be switched off so the IC will go into sleep mode. An enable is necessary to restart the TLE7181EM.

5.2.6 VREG Under Voltage Warning

The TLE7181EM has an integrated under voltage warning detection at VREG. If the supply voltage at VREG reaches the VREG under voltage threshold V_{UVVR}, a warning at ERR pin is set and the TLE7181EM will go into VREG error mode. In case of VREG error mode all output stages will actively switched off to prevent low gate source voltages at the power MOSFETs causing high RDSon. If supply voltage at the VREG pin recovers; the error flag will be cleared and the TLE7181EM will return in normal operation mode.

5.2.7 Over Temperature Warning

The TLE7181EM provides an integrated digital over temperature warning to minimize risk of destruction of the IC at high temperature. The temperature will be detected by a embedded sensor. During over temperature warning the ERR signal is set and the TLE7181EM is in normal operation mode with warning.

The over temperature warning is self clearing. So if temperature is below $T_{j(PW)}$-$dT_{j(OW)}$, the warning will be cleared and TLE7181EM returns to normal operation mode.

It is the decision of the user to react on the over temperature warning.

5.2.8 Over Current Warning

The TLE7181EM offers an integrated over current detection. The output signal of the current sense OpAmp will be monitored. If the output signal reaches the specified voltage threshold V_{OCTH} for a certain time, over current will be detected. After the comparator the filter time t_{OC} is implemented to avoid false triggering caused by overswing of the current sense signal. The ERR pin will be set to low and the TLE7181EM will go into normal operation mode with warning.

The error signal disappears as soon as the current decreases below the over current threshold V_{OCTH}. The error signal disappears as well when the current commutates from the low side MOSFET to the associated high side MOSFET and is no longer flowing over the shunt resistor.

It is the decision of the user to react on the over current signal by modifying input patterns.

5.2.9 Passive Gxx Clamping

If VS Under Voltage shutdown is detected or the device is in Sleep Mode, a passive clamping is active as long as the voltage at VS or VDH is higher than 3V. Even below 3V it is assured that the MOSFET driver stage will not switch on the MOSFET actively.

The passive clamping means that the BHx and the VREG pin are pulled to GND with specified pull down resistors. Together with the intrinsic diode of the push stage of the output stages which connect the gate output to BHx respectively VREG, this assures that the gate of the external MOSFETs are not floating undefined.

5.2.10 $\overline{\text{ERR}}$ Pin

The TLE7181EM has a status pin to provide diagnostic feedback to the µC. The logical output of this pin is a push pull output stage with an integrated pull-down resistor to GND (see **Figure 5**).

Reset of error registers and Disable

The TLE7181EM can be reset by the enable pin ENA. If the ENA pin is pulled to low for a specified minimum time, the error registers are cleared. ERR output is still set to low. After the next rising edge at ENA pin ERR pin will be set to high and no error condition is applied.

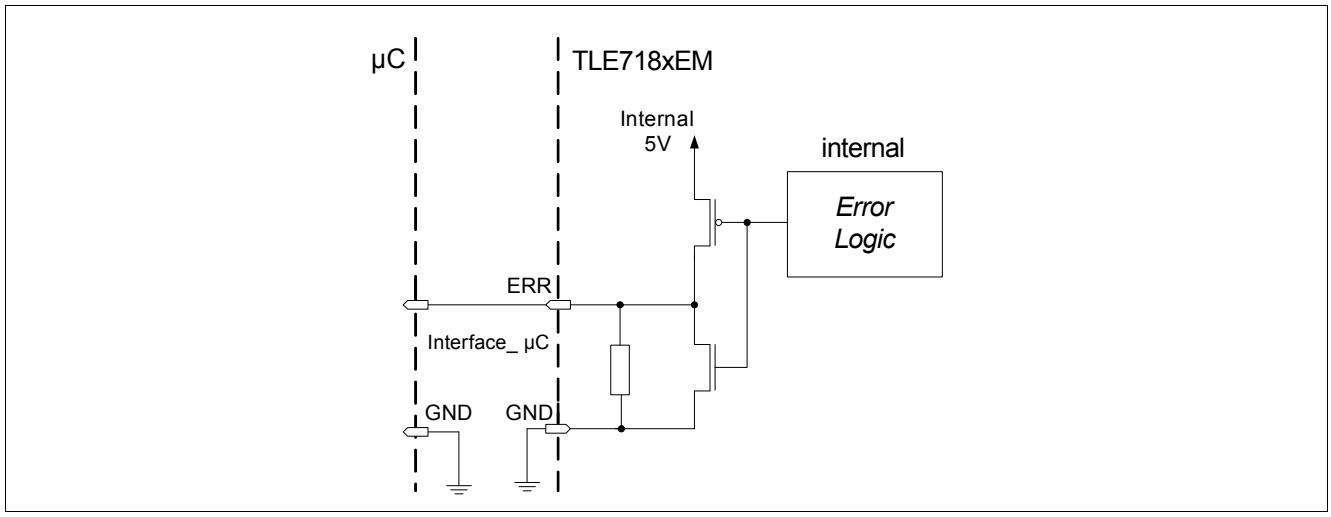


Figure 5 Structure of $\overline{\text{ERR}}$ output

Table 4 Overview of error condition

$\overline{\text{ERR}}$	Driver conditions	Driver action	Restart
High	no errors	Fully functional	–
Low	Over temperature	Warning only	Self clearing
Low	Over voltage VS/VDH	Warning only	Self clearing
Low	Over current OPAMP	Warning only	Self clearing
Low	Under voltage error VREG	All MOSFETs actively switched off	Self clearing
Low	Under voltage shutdown based on VS	MOSFET, charge pump, Vreg switched off	Self clearing restart when enable high[1)]
Low	SCDL open pin	All MOSFETs actively switched off	Self clearing
Low	Short circuit detection	All MOSFETs actively switched off	Reset at ENA needed
Low	Go to sleep mode	All MOSFETs actively switched off	immediate restart when ENA goes high
Low	Wake up mode	start up	–

1) When SC detected, reset with ENA necessary

Table 5 Prioritization of Errors

Priority	Errors and Warnings
0	Under voltage lockout at Vs (VS_UVLO)
1	Short circuit detection error (SCD) SCDL pin open warning (SCDLPOD)
2	Under voltage detection VREG (UV_VREG) Over voltage detection warning (OVD) Over temperature warning (OTD) Over current warning (OCD)

5.2.11 Electrical Characteristics

Electrical Characteristics - Protection and diagnostic functions

V_S = 7.0 to 34V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Short circuit protection							
5.2.1	Short circuit protection detection level input range	V_{SCDL}	0.2	–	2.0	V	programmed by SCDL pin
5.2.2	Short circuit protection detection accuracy	A_{SCP1}	-50	–	+50	%	0.2V≤ V_{SCDL}≤0.3V
5.2.3	Short circuit protection detection accuracy	A_{SCP2}	-30	–	+30	%	0.3V≤ V_{SCDL}≤1.2V
5.2.4	Short circuit protection detection accuracy	A_{SCP3}	-10	–	+10	%	1.2V≤ V_{SCDL}≤2.0V
5.2.5	Filter time of short circuit protection	$t_{SCP(off)}$	2.5	3.5	4.5	µs	–
5.2.6	Filter time and blanking time of short circuit protection	t_{SCPBT}	4	6	8	µs	–
5.2.7	Internal pull-up resistor SCDL to 3V	R_{SCDL}	180	300	475	kΩ	–
5.2.8	SCDL open pin detection level	V_{SCPOP}	2.1	–	3.2	V	–
5.2.9	Filter time of SCDL open pin detection	t_{SCPOP}	1.5	2.5	3.5	µs	–
5.2.10	SCDL open pin detection level hysteresis[1)]	V_{SCOPH}	–	0.3	–	V	–
Over- and under voltage monitoring							
5.2.11	Over voltage warning at Vs and/or VDH	V_{OVW}	34.5	36.5	38.5	V	V_{VS} and/or V_{VDH} increasing
5.2.12	Over voltage warning hysteresis for Vs and/or VDH	V_{OVWhys}	2.1	3.1	4.1	V	–
5.2.13	Over voltage warning filter time for Vs and/or VDH	t_{OV}	13	19	25	µs	–
5.2.14	Under voltage shutdown at Vs	V_{UVVR}	4.5	5.0	5.5	V	V_{VS} decreasing
5.2.15	Under voltage shutdown filter time for VS[1)]	t_{UVLO}	–	20	–	µs	–
5.2.16	Under voltage warning at VREG	V_{UVVR}	5.5	6.0	6.5	V	V_{VS} decreasing
5.2.17	Under voltage diagnosis filter time for VREG	t_{UVVR}	10	–	30	µs	–
5.2.18	Under voltage hysteresis at VREG	V_{UWRhys}	–	0.5	–	V	–
Temperature monitoring							
5.2.19	Over temperature warning	$T_{j(PW)}$	160	170	180	°C	–
5.2.20	Hysteresis for over temperature warning	$dT_{j(OW)}$	10	–	20	°C	–
Over current detection							
5.2.21	Over current detection level	V_{OCTH}	4.5	–	4.99	V	–

Electrical Characteristics - Protection and diagnostic functions (cont'd)

V_S = 7.0 to 34V, T_j = -40 to +150°C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.2.22	Filter time for over current detection	t_{OC}	2.3	–	4.3	µs	–
$\overline{\text{ERR}}$ pin[2]							
5.2.23	$\overline{\text{ERR}}$ output voltage	V_{ERR}	4.6	–	–	V	V_{VS}=7V;
5.2.24	Rise time $\overline{\text{ERR}}$ (20 - 80% of internal 5V)	$t_{f(ERR)}$	–	–	3	µs	C_{LOAD}=1nF;
5.2.25	Internal pull-down resistor $\overline{\text{ERR}}$ to GND	$R_{f(ERR)}$	60	100	170	kΩ	–

1) Not subject to production test, specified by design.
2) $\overline{\text{ERR}}$ pin and Reset & Enable functional between V_{VS}=6 ... 7V, but characteristics might be out of specified range

5.3 Shunt Signal Conditioning

The TLE7181EM incorporates a fast and precise operational amplifier for conditioning and amplification of the current sense shunt signal. The gain of the OpAmp is adjustable by external resistors within a range higher than 5. The usage of higher gains in the application might be limited by required settling time and band width.

It is recommended to apply a small offset to the OpAmp, to avoid operation in the lower rail at low currents.

The output of the OpAmp ISO is not short-circuit proof.

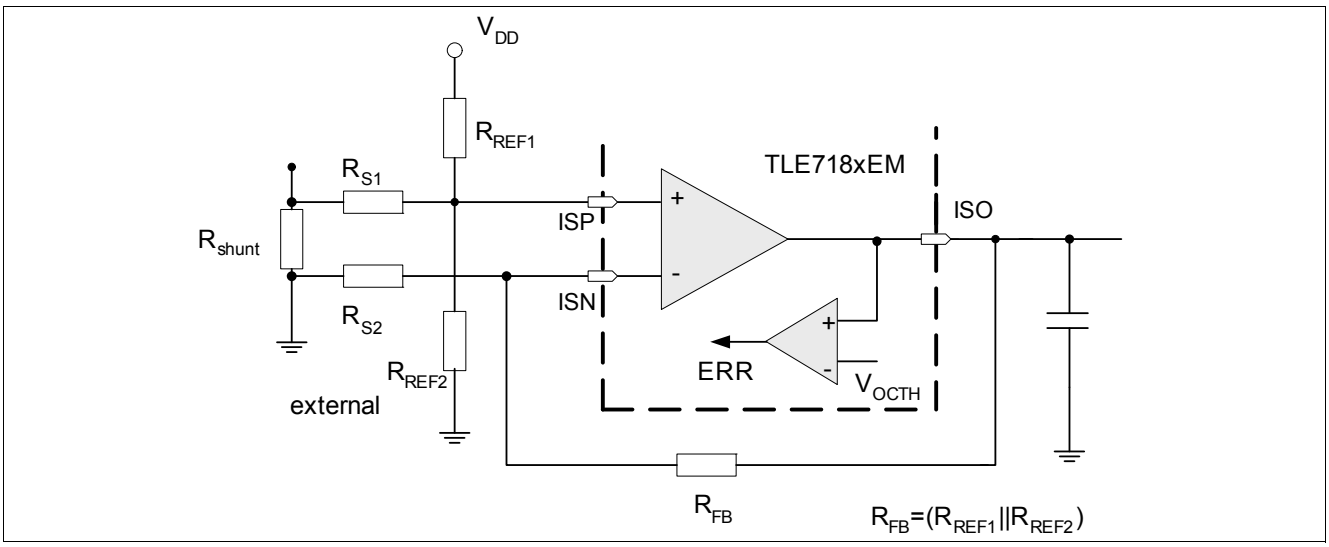


Figure 6 Shunt Signal Conditioning Block Diagram and Over Current Limitation

Over current warning see **Chapter 5.2.8**.

5.3.1 Electrical Characteristics

Electrical Characteristics - Current sense signal conditioning

V_S = 7.0 to 36V, T_j = -40 to +150°C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.1	Series resistors	R_S	100	500	1000	Ω	–
5.3.2	Feedback resistor Limited by the output voltage dynamic range	R_{fb}	2000	7500	–	Ω	–
5.3.3	Resistor ratio (gain ratio)	$R_{fb/RS}$	5	–	–	–	–
5.3.4	Steady state differential input voltage range across VIN	$V_{IN(ss)}$	-400	–	400	mV	–
5.3.5	Input differential voltage (ISP - ISN)	V_{IDR}	-800	–	800	mV	–
5.3.6	Input voltage (Both Inputs - GND) (ISP - GND) or (ISN -GND)	V_{LL}	-800	–	2000	mV	–
5.3.7	Input offset voltage of the I-DC link OpAmp, including temperature drift	V_{IO}	–	–	+/-2	mV	R_S=500Ω; V_{CM}=0V; V_{ISO}=1.65V;
5.3.8	Input bias current (ISN,ISP to GND)	I_{IB}	-300	–	–	µA	V_{CM}=0V; V_{ISO}=open
5.3.9	Low level output voltage of ISO	V_{OL}	-0.1	–	0.2	V	I_{OH}=3mA

Electrical Characteristics - Current sense signal conditioning (cont'd)

V_S = 7.0 to 36V, T_j = -40 to +150°C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.3.10	High level output voltage of ISO	V_{OH}	4.75	–	5.2	V	I_{OH}=-3mA
5.3.11	Output short circuit current	I_{SCOP}	5	–	–	mA	–
5.3.12	Differential input resistance[1)]	R_I	100	–	–	kΩ	–
5.3.13	Common mode input capacitance[1)]	C_{CM}	–	–	10	pF	10kHz
5.3.14	Common mode rejection ratio at DC CMRR = 20*Log((Vout_diff/Vin_diff) * (Vin_CM/Vout_CM))	C_{MRR}	80	100	–	dB	–
5.3.15	Common mode suppression[2)] with CMS = 20*Log(Vout_CM/Vin_CM) Freq =100kHz Freq = 1MHz Freq = 10MHz	C_{MS}	–	 62 43 23	–	dB	V_{IN}=360mV* sin(2*π*freq*t); R_s=500Ω; R_{fb}=7500Ω
5.3.16	Slew rate	$d_{V/dt}$	–	10	–	V/µs	Gain≥ 5; R_L=1.0kΩ; C_L=500pF
5.3.17	Large signal open loop voltage gain (DC)	A_{OL}	80	100	–	dB	–
5.3.18	Unity gain bandwidth[1)]	G_{BW}	10	20	–	MHz	R_L=1kΩ; C_L=100pF
5.3.19	Phase margin [1)]	F_M	–	50	–	°	Gain≥ 5; R_L=1kΩ; C_L=100pF
5.3.20	Gain margin [1)]	A_M	–	12	–	dB	R_L=1kΩ; C_L=100pF
5.3.21	Bandwidth	B_{WG}	0.7	1.3	–	MHz	Gain=15; R_L=1kΩ; C_L=500pF; R_s=500Ω
5.3.22	Output settle time to 98%	t_{set1}	–	1	1.8	µs	Gain=15; R_L=1kΩ; C_L=500pF; 0.3<V_{ISO}< 4.8V; R_s=500Ω
5.3.23	Output settle time to 98%[1)]	t_{set2}	–	4.6	–	µs	Gain=75; R_L=1kΩ; C_L=500pF; 0.3<V_{ISO}< 4.8V; R_s=500Ω

1) Not subjected to production test; specified by design

2) Without considering any offsets such as input offset voltage, internal mismatch and assuming no tolerance error in external resistors.

6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This is the description how the IC is used in its environment…

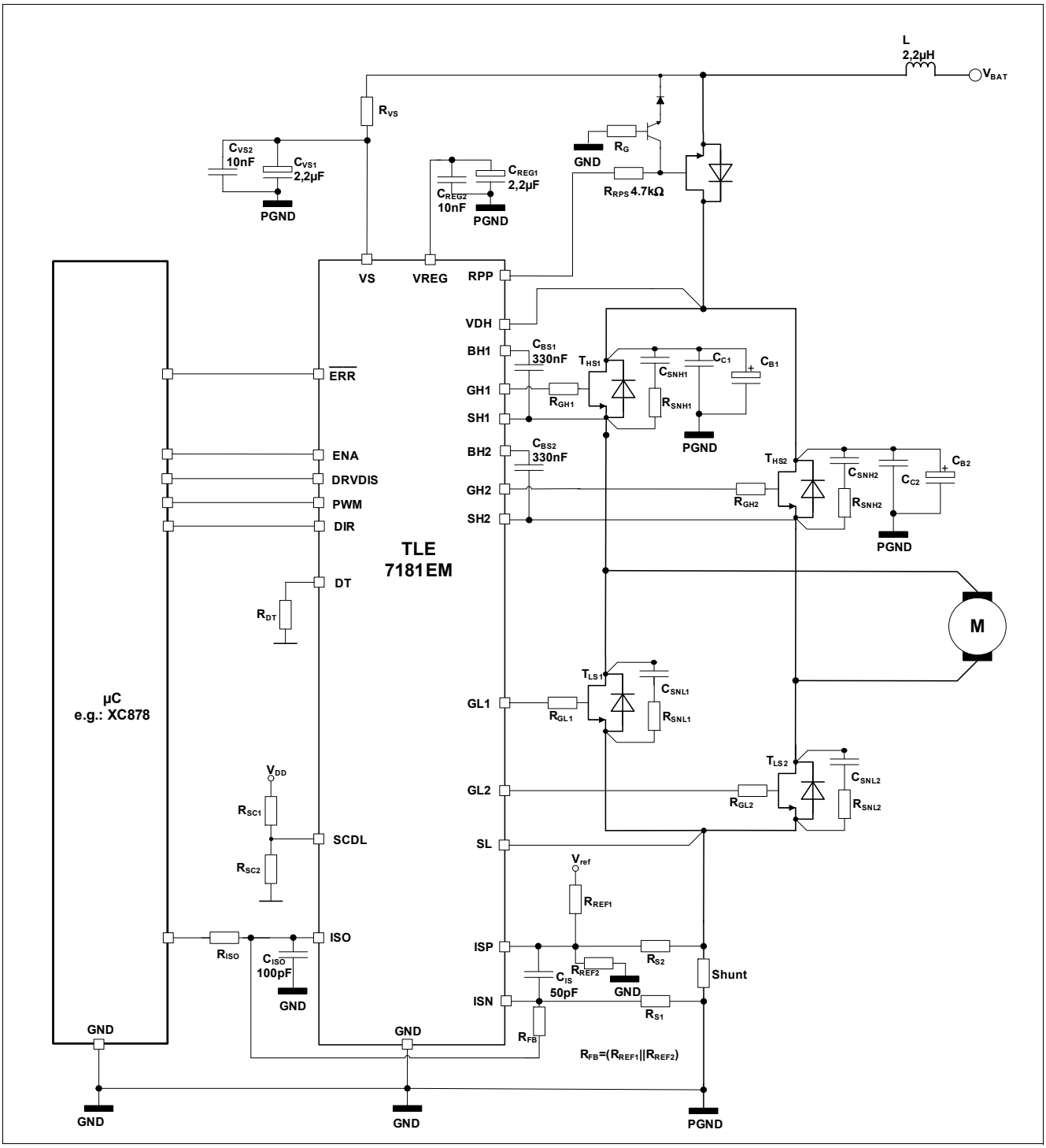


Figure 7 Application Diagram 1: DC-Brush motor controlled by TLE7181EM

Note: This are very simplified examples of an application circuit. The function must be verified in the real application.

6.1 Layout Guide Lines

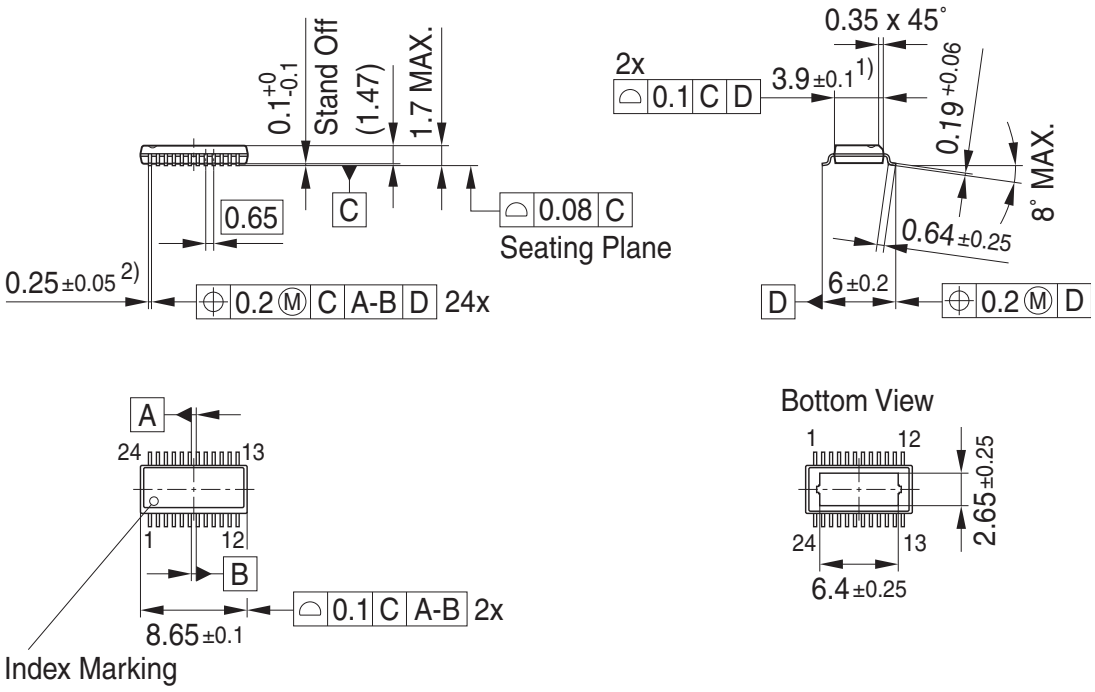
Please refer also to the simplified application example.

- Two separated bulk capacitors C_B should be used - one per half bridge
- Two separated ceramic capacitors C_C should be used - one per half bridge
- Each of the two bulk capacitors C_B and each of the two ceramic capacitors C_C should be assigned to one of the half bridges and should be placed very close to it
- The components within one half bridge should be placed close to each other: high side MOSFET, low side MOSFET, bulk capacitor C_B and ceramic capacitor C_C (C_B and C_C are in parallel) and the shunt resistor form a loop that should be as small and tight as possible. The traces should be short and wide
- The connection between the source of the high side MOSFET and the drain of the low side MOSFET should be as low inductive and as low resistive as possible.
- VDH is the sense pin used for short circuit detection; VDH should be routed (via Rvdh) to the common point of the drains of the high side MOSFETs to sense the voltage present on drain high side
- SL is the sense pin used for short circuit detection; SL should be routed o the common point of the source of the low side MOSFETs to sense the voltage present on source low side
- Additional R-C snubber circuits (R and C in series) can be placed to attenuate/suppress oscillations during switching of the MOSFETs, there may be one or two snubber circuits per half bridge, R (several Ohm) and C (several nF) must be low inductive in terms of routing and packaging (ceramic capacitors)
- if available the exposed pad on the backside of the package should be connected to GND

6.2 Further Application Information

- For further information you may contact **http://www.infineon.com/**

7 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Does not include dambar protrusion of 0.13 max.

PG-SSOP-24-4-PO V01

Figure 8 PG-SSOP-24-4

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

8 Revision History

Revision	Date	Changes
1.1	2010-09-30	Datasheet Max rating of current at RPP pin increased
1.0	2010-09-29	Datasheet Thermal resistance of package adjusted Output rise time adjusted Pull up and pull down resistor values adapted Dead time values centered Go to sleep time modified Filter time of short circuit detection adjusted SCDL pin open detection description improved Overview of error condition table improved Filter time and blanking time of short circuit detection adjusted SCDL open pin detection level added Filter time of SCDL open pin detection adjusted Over voltage warning at Vs and/or VDH centered Over voltage warning hysteresis for Vs and/or VDH centered Over voltage warning filter time for Vs and/or VDH centered ERR output voltage added OpAmp bandwidth adjusted
0.8	2010-08-31	Preliminary Datasheet
0.7	2009-11-19	Target data sheet
0.6	2008-30-10	Target data sheet

Edition 2010-09-30

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

单击下面可查看定价，库存，交付和生命周期等信息

>>Infineon Technologies(英飞凌)

>>点击查看相关商品