MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ P6

600V CoolMOS™ P6 Power Transistor
IPL60R650P6S

Data Sheet

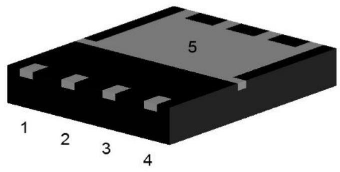
Rev. 2.0
Final

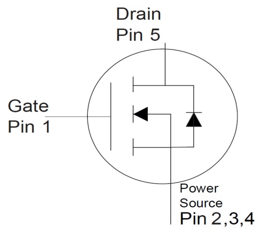
Power Management & Multimarket

1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. CoolMOS™ P6 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The offered devices provide all benefits of a fast switching SJ MOSFET while not sacrificing ease of use. Extremely low switching and conduction losses make switching applications even more efficient, more compact, lighter and cooler.

ThinPAK 5x6





Features

- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Very high commutation ruggedness
- Easy to use/drive
- Pb-free plating, Halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

Applications

PFC stages, hard switching PWM stages and resonant switching PWM stages for e.g. PC Silverbox, Adapter, LCD & PDP TV, Lighting, Server, Telecom and UPS.

Please note: For MOSFET paralleling the use of ferrite beads on the gate or seperate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j,max}$	650	V
$R_{DS(on),max}$	0.65	Ω
$Q_{g,typ}$	12	nC
$I_{D,pulse}$	16.5	A
E_{oss}@400V	1.8	µJ
Body diode di/dt	500	A/µs

Type / Ordering Code	Package	Marking	Related Links
IPL60R650P6S	ThinPAK 5x6 SMD	60P6650	see Appendix A

Table of Contents

2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D	- -	- -	6.7 4.2	A	T_C = 25°C T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$	-	-	16.5	A	T_C=25°C
Avalanche energy, single pulse	E_{AS}	-	-	133	mJ	I_D =1.3A; V_{DD} = 50V
Avalanche energy, repetitive	E_{AR}	-	-	0.20	mJ	I_D =1.3A; V_{DD} = 50V
Avalanche current, repetitive	I_{AR}	-	-	1.3	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	V_{DS} =0...480V
Gate source voltage	V_{GS}	-20 -30	- -	20 30	V	static; AC (f>1 Hz)
Power dissipation (non FullPAK)	P_{tot}	-	-	56.8	W	T_C=25°C
Operating and storage temperature	T_j, T_{stg}	-40	-	150	°C	-
Continuous diode forward current	I_S	-	-	5.8	A	T_C=25°C
Diode pulse current[2]	$I_{S,pulse}$	-	-	16.2	A	T_C = 25°C
Reverse diode dv/dt[3]	dv/dt	-	-	15	V/ns	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C
Maximum diode commutation speed[3]	di_f/dt	-	-	500	A/µs	V_{DS} =0...400V, I_{SD}<=I_S, T_j=25°C

3 Thermal characteristics

Table 3 Thermal characteristics (non FullPAK)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	2.2	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	35	62	°C/W	Device on 40mm*40mm*1.5 epoxy PCB FR4 with 6cm^2 (one layer 70µm thick) copper area for drain connection and cooling. PCB is vertical without blown air.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	reflow MSL1

[1] Limited by $T_{j\,max}$. Maximum duty cycle D=0.75
[2] Pulse width t_p limited by $T_{j,max}$
[3] V_{DClink}=400V; $V_{DS,peak}$<$V_{(BR)DSS}$; identical low side and high side switch with identical R_G

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	V_{GS}=0V, I_D=1mA
Gate threshold voltage	$V_{(GS)th}$	3.50	4	4.50	V	V_{DS}=V_{GS}, I_D=0.2mA
Zero gate voltage drain current	I_{DSS}	- -	- 10	1 -	µA	V_{DS}=600V, V_{GS}=0V, T_j=25°C V_{DS}=600V, V_{GS}=0V, T_j=150°C
Gate-source leakage curent	I_{GSS}	-	-	100	nA	V_{GS}=20V, V_{DS}=0V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.59 1.52	0.65 -	Ω	V_{GS}=10V, I_D=2.4A, T_j=25°C V_{GS}=10V, I_D=2.4A, T_j=150°C
Gate resistance	R_G	-	11	-	Ω	f=1 MHz, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	557	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Output capacitance	C_{oss}	-	28	-	pF	V_{GS}=0V, V_{DS}=100V, f=1MHz
Effective output capacitance, energy related[1]	$C_{o(er)}$	-	23	-	pF	V_{GS}=0V, V_{DS}=0...480V
Effective output capacitance, time related[2]	$C_{o(tr)}$	-	88	-	pF	I_D=constant, V_{GS}=0V, V_{DS}=0...480V
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=3A, R_G=6.8Ω
Rise time	t_r	-	7	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=3A, R_G=6.8Ω
Turn-off delay time	$t_{d(off)}$	-	33	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=3A, R_G=6.8Ω
Fall time	t_f	-	14	-	ns	V_{DD}=400V, V_{GS}=13V, I_D=3A, R_G=6.8Ω

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	3	-	nC	V_{DD}=480V, I_D=3A, V_{GS}=0 to 10V
Gate to drain charge	Q_{gd}	-	5	-	nC	V_{DD}=480V, I_D=3A, V_{GS}=0 to 10V
Gate charge total	Q_g	-	12	-	nC	V_{DD}=480V, I_D=3A, V_{GS}=0 to 10V
Gate plateau voltage	$V_{plateau}$	-	6.1	-	V	V_{DD}=480V, I_D=3A, V_{GS}=0 to 10V

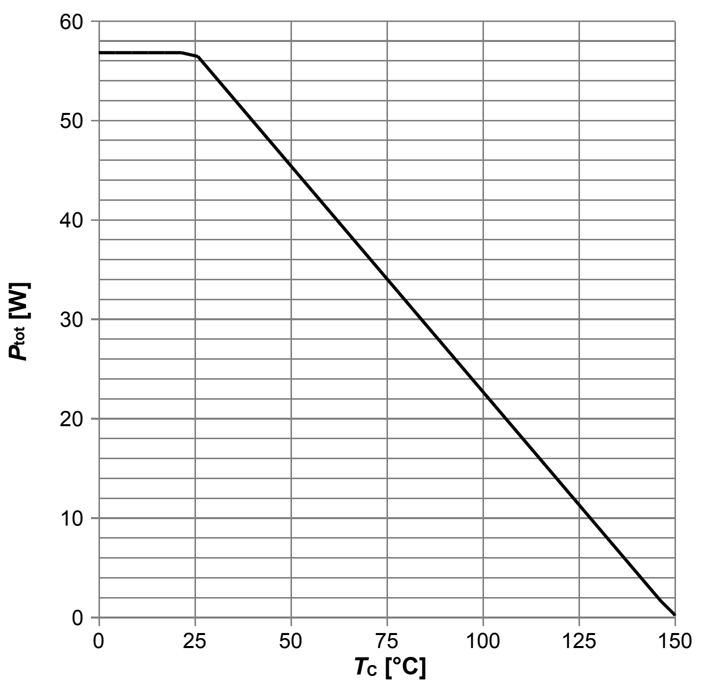
[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	V_{GS}=0V, I_F=3A, T_j=25°C
Reverse recovery time	t_{rr}	-	196	-	ns	V_R=400V, I_F=3A, di_F/dt=100A/µs
Reverse recovery charge	Q_{rr}	-	1.7	-	µC	V_R=400V, I_F=3A, di_F/dt=100A/µs
Peak reverse recovery current	I_{rrm}	-	17	-	A	V_R=400V, I_F=3A, di_F/dt=100A/µs

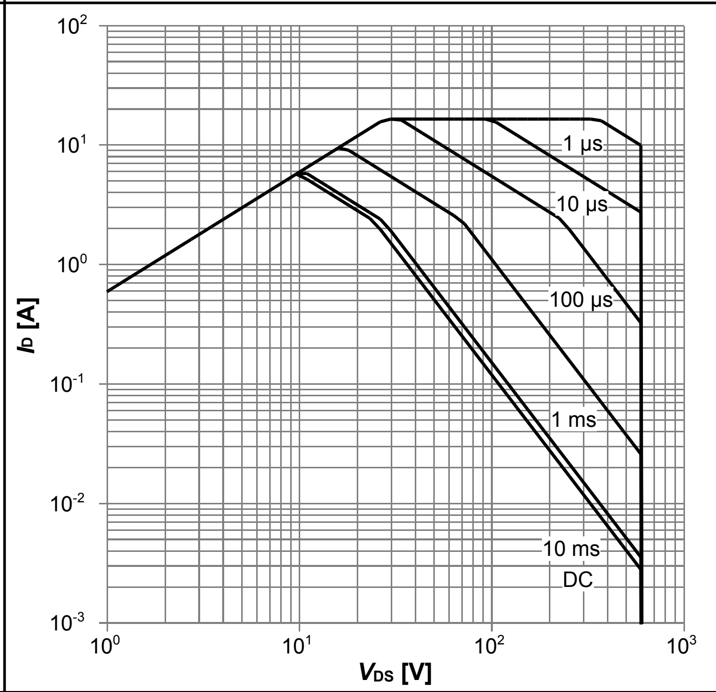
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



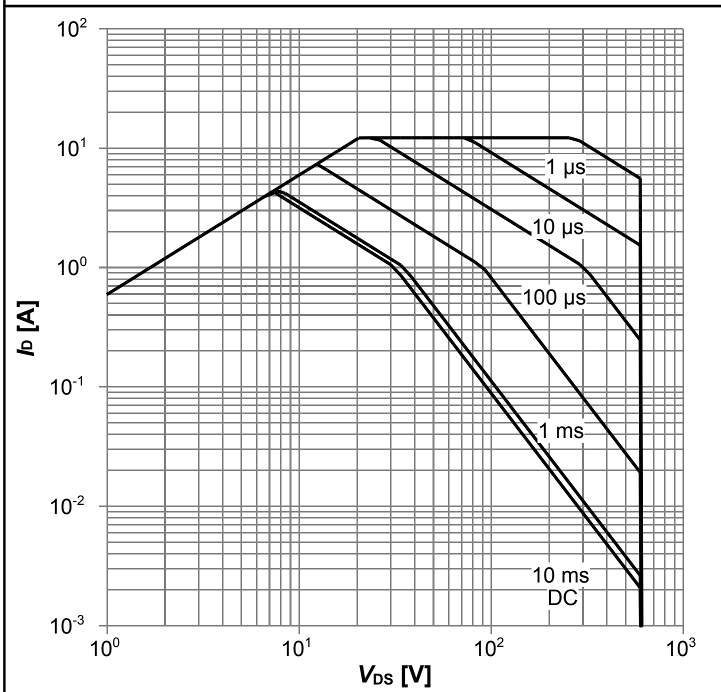
P_{tot}=f(T_C)

Diagram 2: Safe operating area



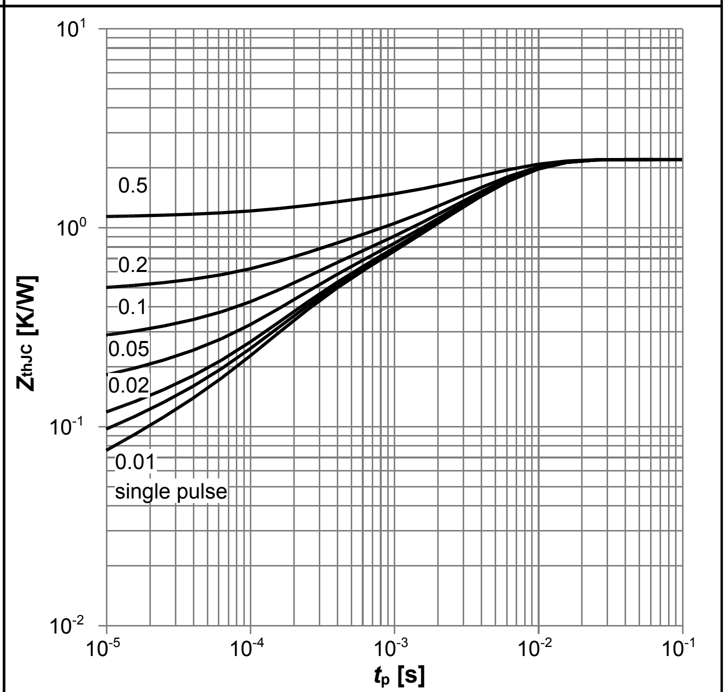
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 3: Safe operating area



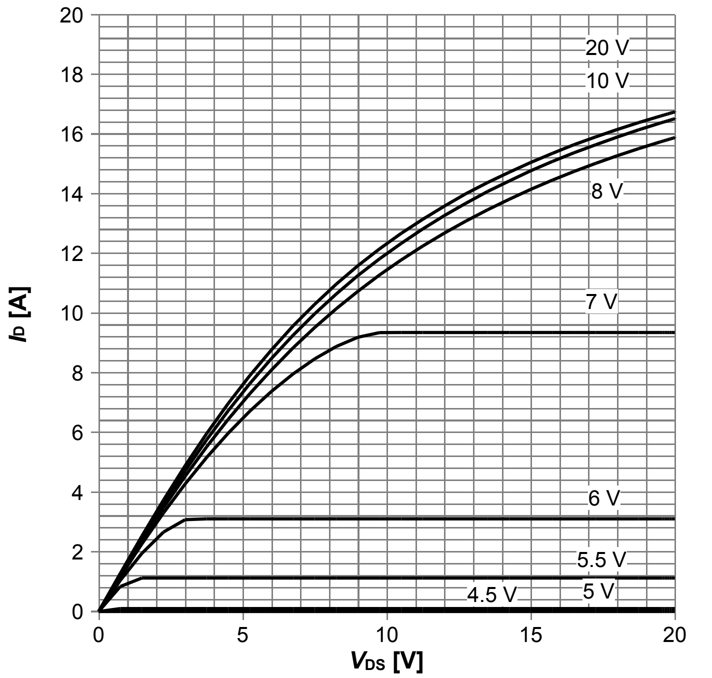
I_D=f(V_{DS}); T_C=80 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



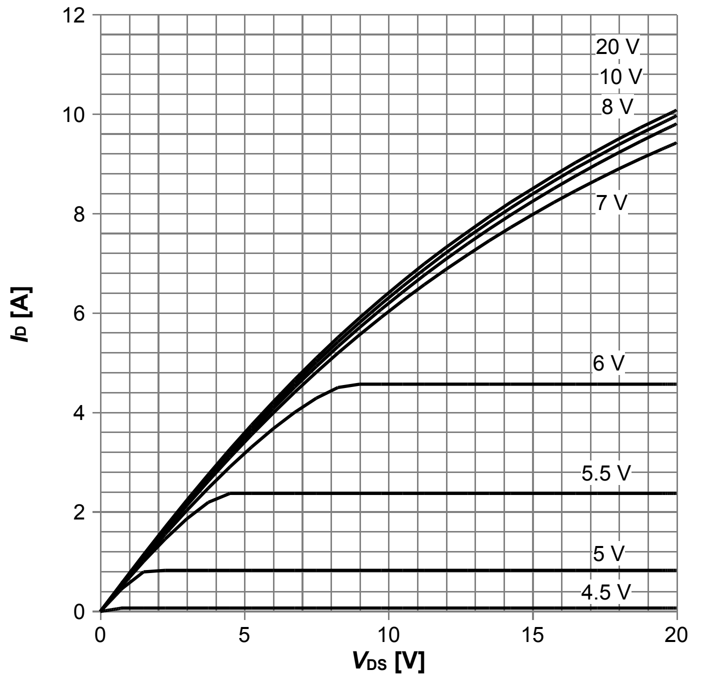
Z_{thJC} =f(t_P); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



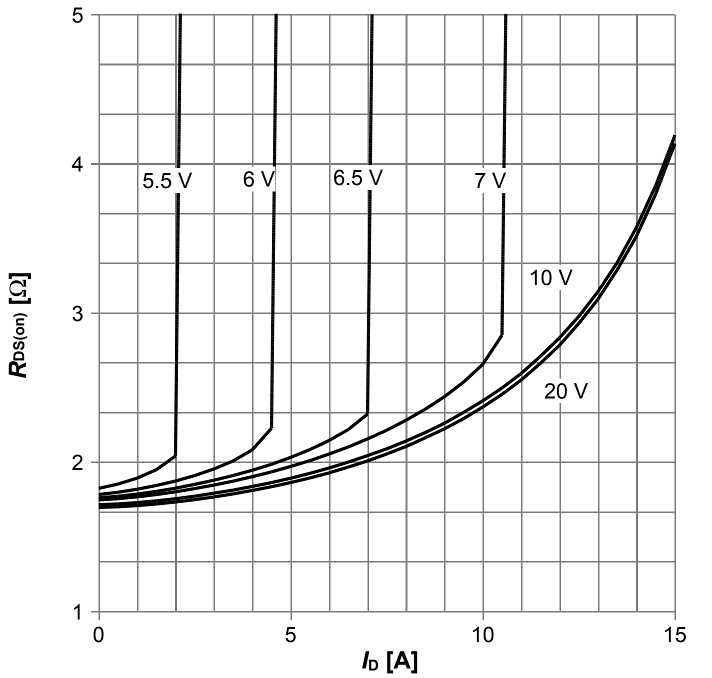
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. output characteristics



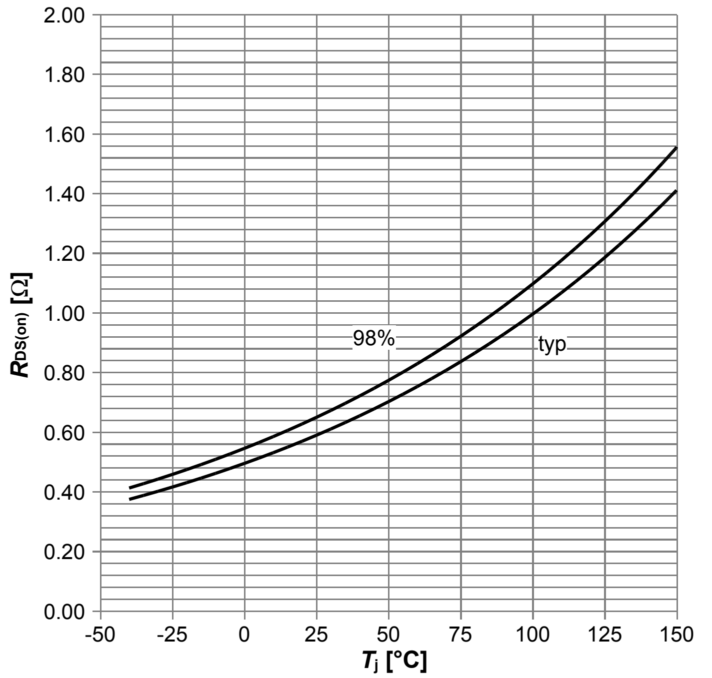
I_D=f(V_{DS}); T_j=125 °C; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



$R_{DS(on)}$=f(I_D); T_j=125 °C; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



$R_{DS(on)}$=f(T_j); I_D=3 A; V_{GS}=10 V

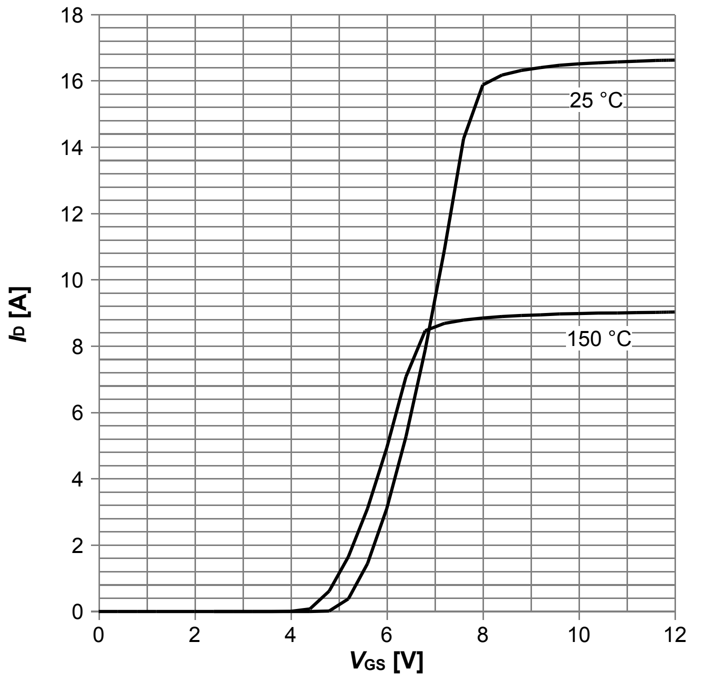
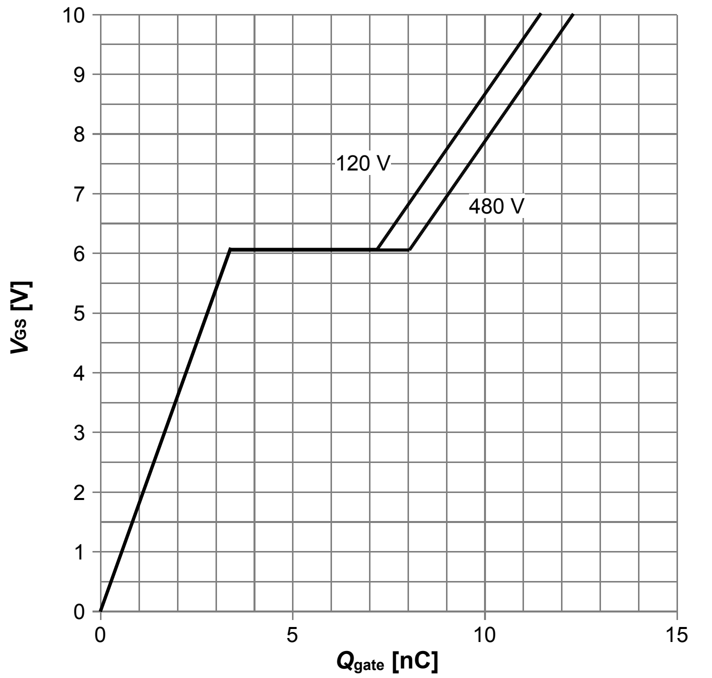
Diagram 9: Typ. transfer characteristics	Diagram 10: Typ. gate charge
	
I_D=f(V_{GS}); V_{DS}=20V; parameter: T_j	V_{GS}=f(Q_{gate}); I_D=3 A pulsed; parameter: V_{DD}

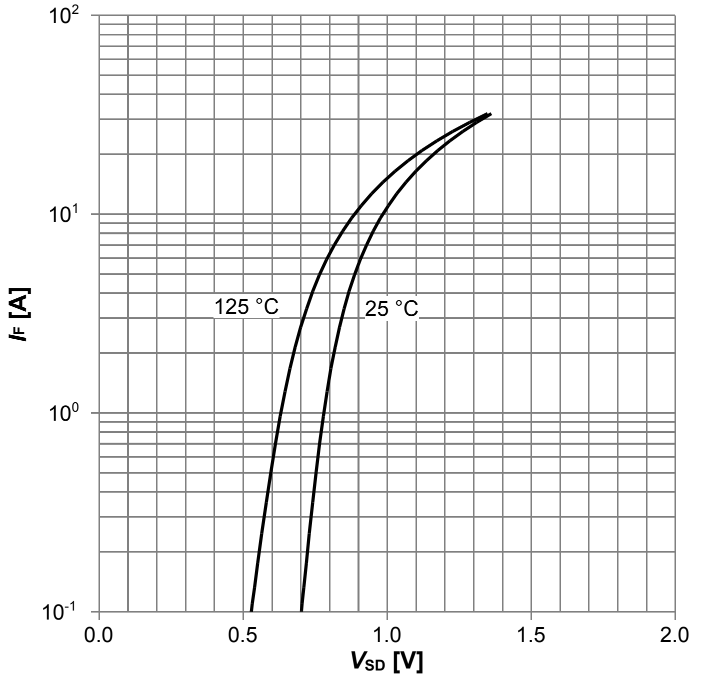
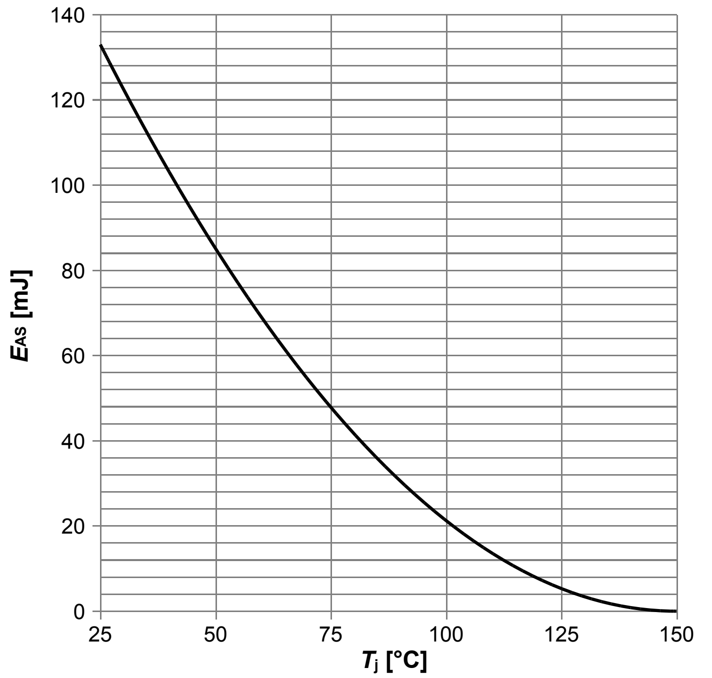
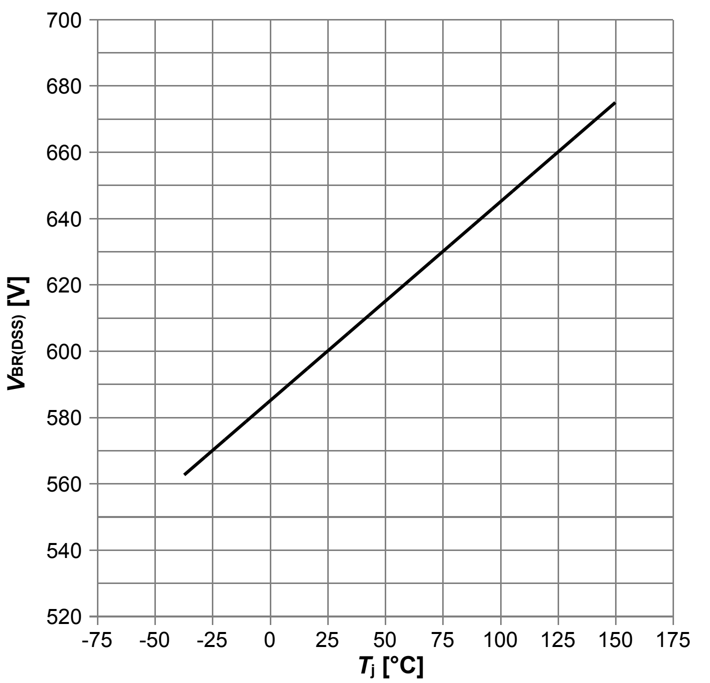
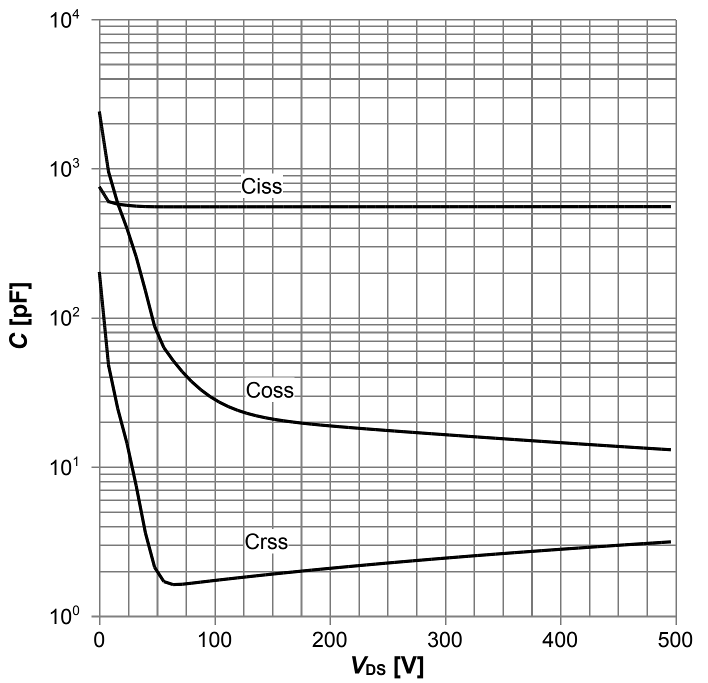
Diagram 11: Forward characteristics of reverse diode	Diagram 12: Avalanche energy
	
I_F=f(V_{SD}); parameter: T_j	E_{AS}=f(T_j); I_D=1.3 A; V_{DD}=50 V

Diagram 13: Drain-source breakdown voltage



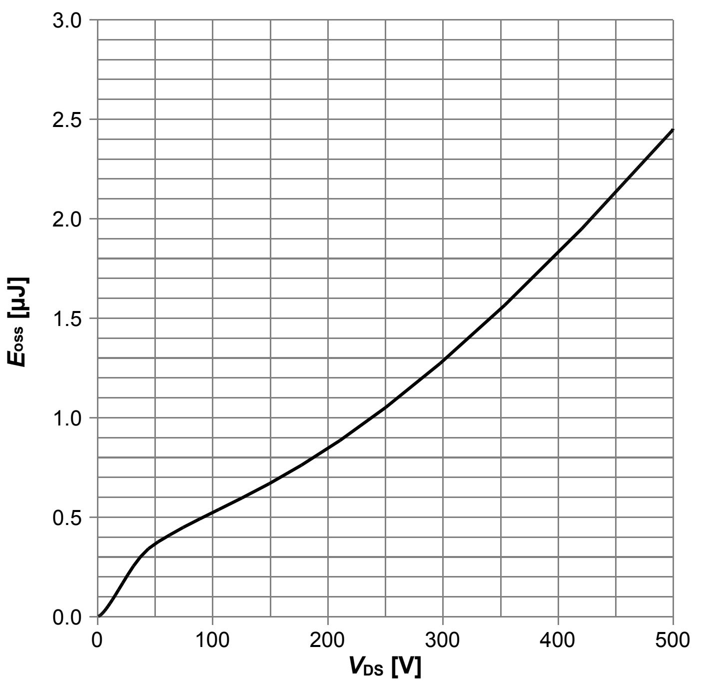
$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Diagram 14: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 15: Typ. Coss stored energy



E_{oss}=f(V_{DS})

6 Test Circuits

Table 8 Diode characteristics

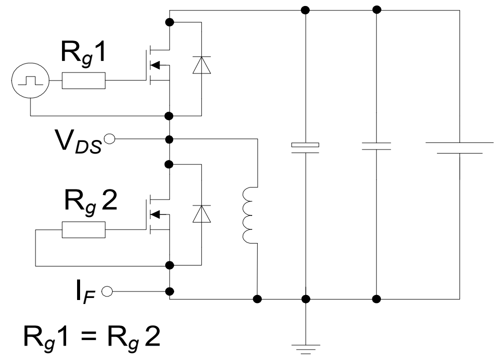
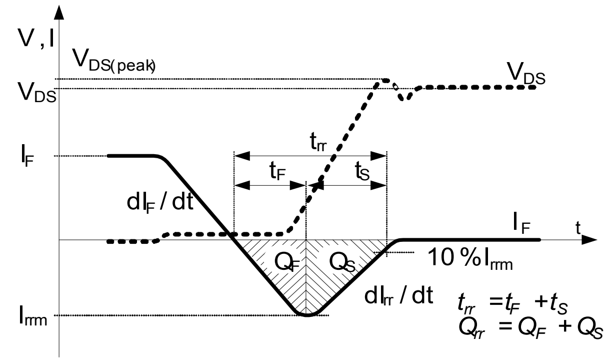
Test circuit for diode characteristics	Diode recovery waveform
	

Table 9 Switching times

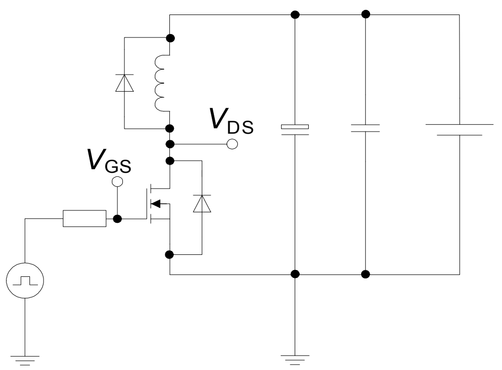
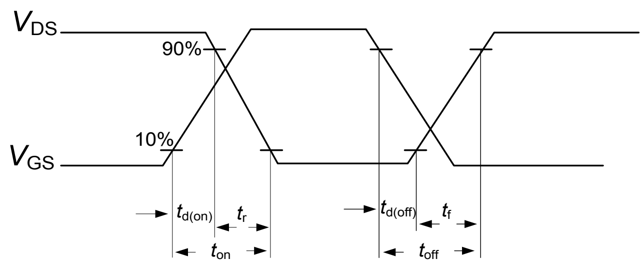
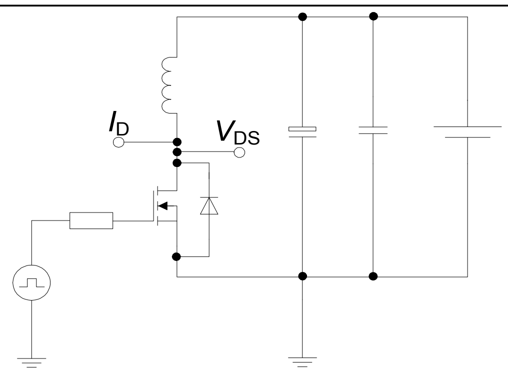
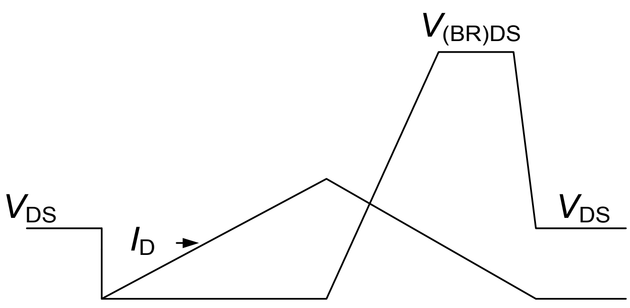
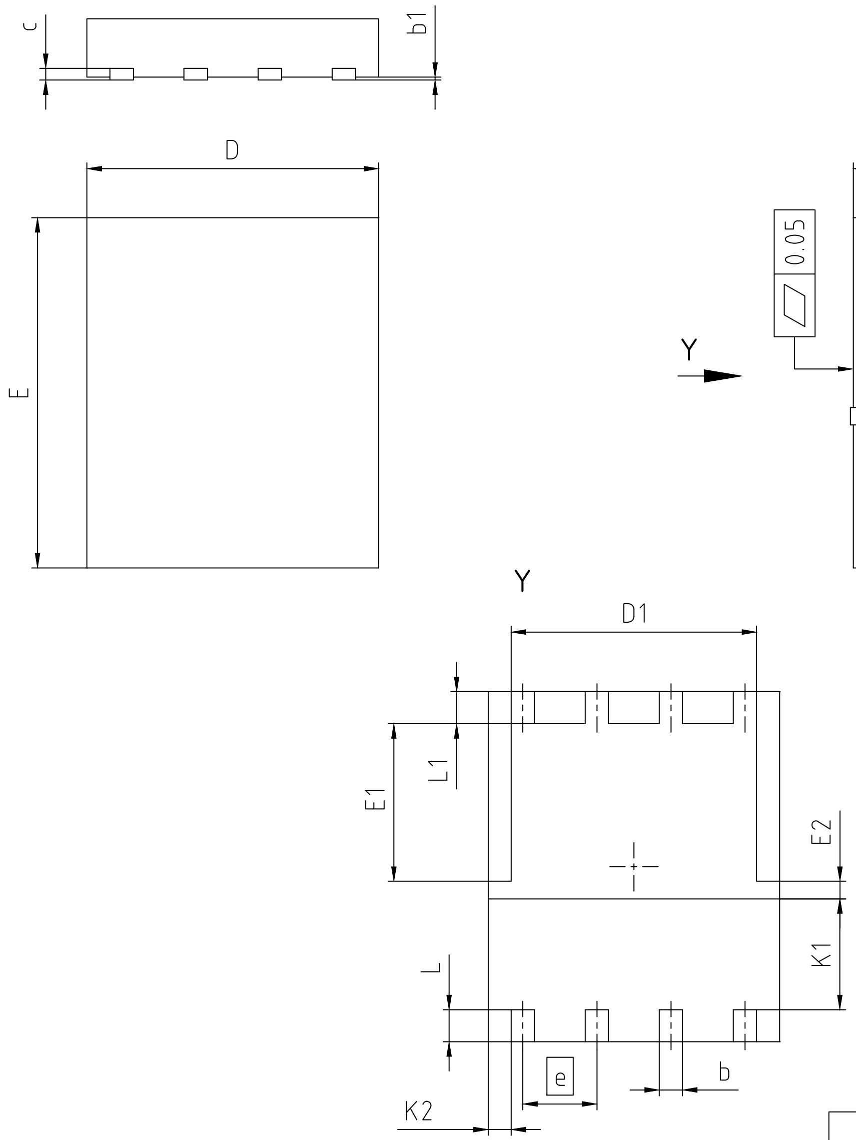
Switching times test circuit for inductive load	Switching times waveform
	

Table 10 Unclamped inductive load

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.90	1.10	0.035	0.043
b	0.30	0.50	0.012	0.020
b1	0.00	0.05	0.000	0.002
c	0.10	0.30	0.004	0.012
D	4.90	5.10	0.193	0.201
D1	4.11	4.31	0.162	0.170
E	5.90	6.10	0.232	0.240
E1	2.60	2.80	0.102	0.110
E2	0.20	0.40	0.008	0.016
e	1.27 (BSC)		0.05 (BSC)	
K1	1.80	2.00	0.071	0.079
K2	0.30	0.50	0.012	0.020
L	0.45	0.65	0.018	0.026
L1	0.45	0.65	0.018	0.026
N	8		8	

DOCUMENT NO.
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SCALE 0 1 2mm

EUROPEAN PROJECTION

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REVISION
01

Figure 1 Outline ThinPAK 5x6 SMD, dimensions in mm/inches

8 Appendix A

Table 11 Related Links

- **IFX CoolMOS Webpage:** www.infieon.com
- **IFX Design tools:** www.infineon.com

Revision History

IPL60R650P6S

Revision: 2014-07-08, Rev. 2.0

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.0	2014-07-08	Release of final version

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