

IGBT Chip in NPT-technology

FEATURES:

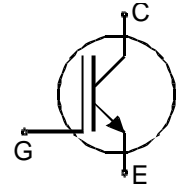
- 1200V NPT technology 180µm chip
- low turn-off losses
- short tail current
- positive temperature coefficient
- easy paralleling
- integrated gate resistor

This chip is used for:

- power module
BSM50GD120DLC

Applications:

- drives



Chip Type	V _{CE}	I _{CN}	Die Size	Package	Ordering Code
SIGC81T120R2CL	1200V	50A	9.08 X 8.98 mm ²	sawn on foil	Q67041- A4700-A001

MECHANICAL PARAMETER:

Raster size	9.08 X 8.98	mm ²
Emitter pad size	8 x (2.6 x 1.78)	
Gate pad size	1.46 x 0.8	
Area total / active	81.5 / 63.5	
Thickness	180	µm
Wafer size	150	mm
Flat position	90	grd
Max.possible chips per wafer	167 pcs	
Passivation frontside	Photoimide	
Emitter metallization	3200 nm Al Si 1%	
Collector metallization	1400 nm Ni Ag –system suitable for epoxy and soft solder die bonding	
Die bond	electrically conductive glue or solder	
Wire bond	Al, <500µm	
Reject Ink Dot Size	Ø 0.65mm ; max 1.2mm	
Recommended Storage Environment	store in original container, in dry nitrogen, < 6 month at an ambient temperature of 23°C	

MAXIMUM RATINGS:

Parameter	Symbol	Value	Unit
Collector-emitter voltage, $T_j=25\text{ }^\circ\text{C}$	V_{CE}	1200	V
DC collector current, limited by T_{jmax}	I_C	¹⁾	A
Pulsed collector current, t_p limited by T_{jmax}	I_{Cpuls}	150	A
Gate emitter voltage	V_{GE}	± 20	V
Operating junction and storage temperature	T_j, T_{stg}	-55 ... +150	$^\circ\text{C}$

¹⁾ depending on thermal properties of assembly

STATIC CHARACTERISTICS (tested on chip), $T_j=25\text{ }^\circ\text{C}$, unless otherwise specified:

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0V, I_C=3mA$	1200			V
Collector-emitter saturation voltage	$V_{CE(sat)}$	$V_{GE}=15V, I_C=50A$	1.8	2.2	2.6	
Gate-emitter threshold voltage	$V_{GE(th)}$	$I_C=2mA, V_{GE}=V_{CE}$	4.5	5.5	6.5	
Zero gate voltage collector current	I_{CES}	$V_{CE}=1200V, V_{GE}=0V$			6.2	μA
Gate-emitter leakage current	I_{GES}	$V_{CE}=0V, V_{GE}=20V$			300	nA
Integrated gate resistor	R_{Gint}			5		Ω

ELECTRICAL CHARACTERISTICS (tested at component):

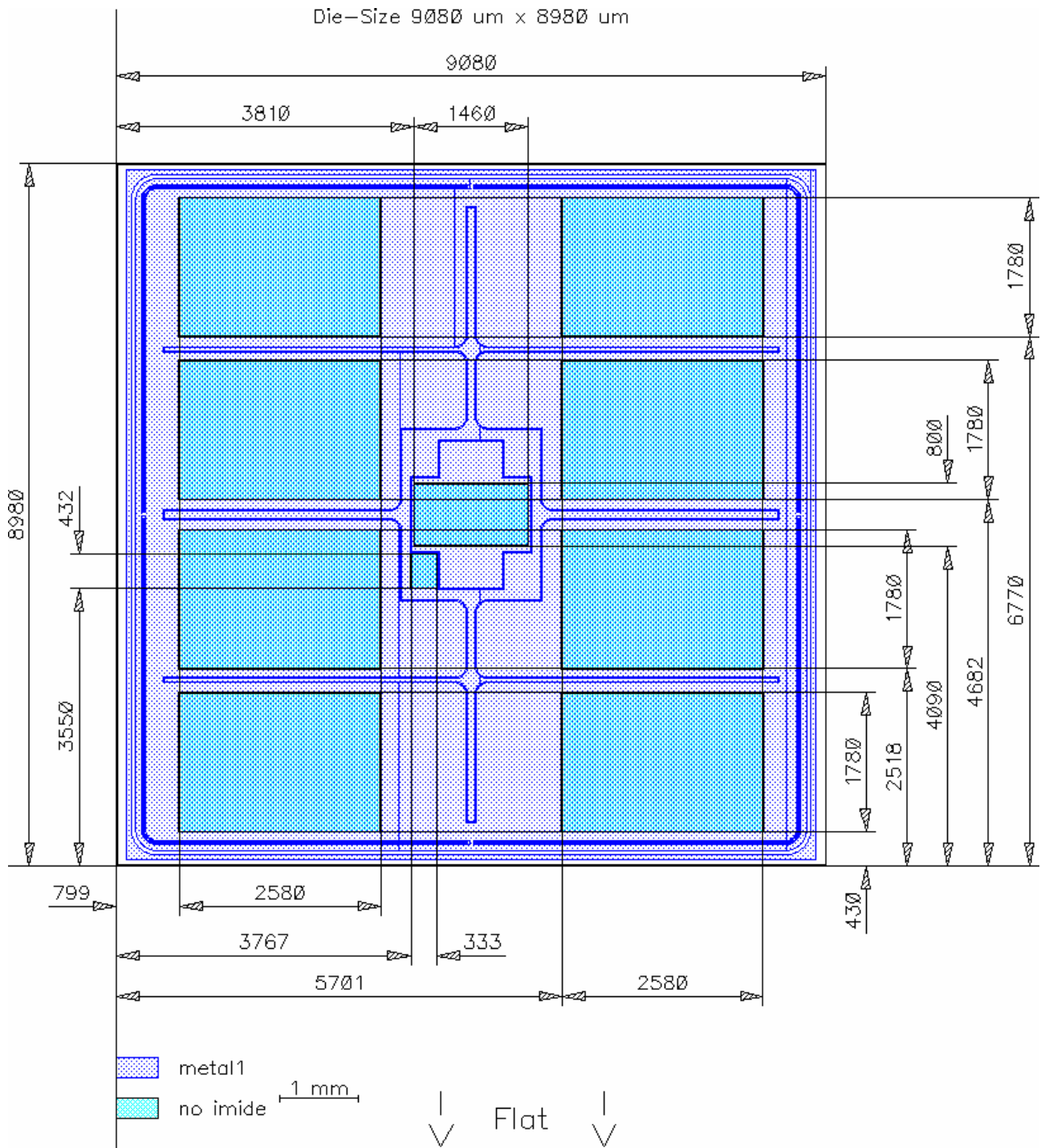
Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Input capacitance	C_{iss}	$V_{CE}=25V,$	-	3.3	-	nF
Output capacitance	C_{oss}	$V_{GE}=0V,$	-	-	-	
Reverse transfer capacitance	C_{riss}	$f=1\text{MHz}$	-	0.21	-	

SWITCHING CHARACTERISTICS (tested at component), Inductive Load

Parameter	Symbol	Conditions ¹⁾	Value			Unit
			min.	typ.	max.	
Turn-on delay time	$t_{d(on)}$	$T_j=125\text{ }^\circ\text{C}$	-	60	-	ns
Rise time	t_r	$V_{CC}=600V,$	-	50	-	
Turn-off delay time	$t_{d(off)}$	$I_C=50A,$	-	300	-	
Fall time	t_f	$V_{GE}=\pm 15V,$ $R_G=15\Omega$	-	70	-	

¹⁾ values also influenced by parasitic L- and C- in measurement and package.

CHIP DRAWING:





SIGC81T120R2CL

FURTHER ELECTRICAL CHARACTERISTICS:

This chip data sheet refers to the device data sheet	BSM50GD120DLC	Package Econo 2 short pin
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DESCRIPTION:

AQL 0,65 for visual inspection according to failure catalog

Electrostatic Discharge Sensitive Device according to MIL-STD 883

Test-Normen Villach/Prüffeld

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