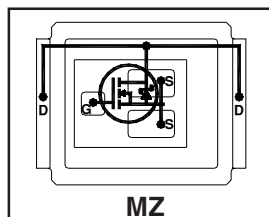


Typical values (unless otherwise specified)

V_{DS}	V_{GS}	$R_{DS(on)}$			
100V max	±20V max	17.5mΩ @ 10V			
$Q_{g\ tot}$	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$
22nC	6.8nC	1.2nC	50nC	11nC	3.9V



- RoHs Compliant ①
- Lead-Free (Qualified up to 260°C Reflow)
- Application Specific MOSFETs
- Ideal for High Performance Isolated Converter Primary Switch Socket
- Optimized for Synchronous Rectification
- Low Conduction Losses
- High Cdv/dt Immunity
- Low Profile (<0.7mm)
- Dual Sided Cooling Compatible ①
- Compatible with existing Surface Mount Techniques ①

Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	MX	MT	MZ			
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Description

The IRF6662PbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.7 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques. Application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6662PbF is optimized for primary side bridge topologies in isolated DC-DC applications, for wide range universal input Telecom applications (36V - 75V), and for secondary side synchronous rectification in regulated DC-DC topologies. The reduced total losses in the device coupled with the high level of thermal performance enables high efficiency and low temperatures, which are key for system reliability improvements, and makes this device ideal for high performance isolated DC-DC converters.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	±20	
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	8.3	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ③	6.6	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ④	47	
I_{DM}	Pulsed Drain Current ⑤	66	
E_{AS}	Single Pulse Avalanche Energy ⑥	39	mJ
I_{AR}	Avalanche Current ⑤	4.9	A

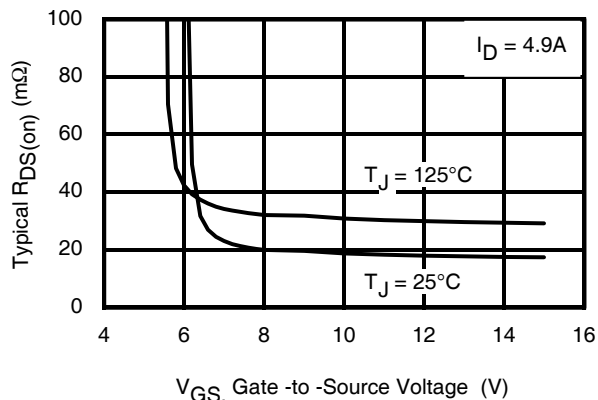


Fig 1. Typical On-Resistance vs. Gate Voltage

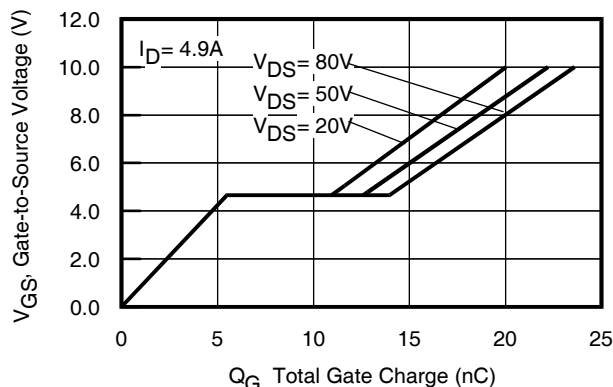


Fig 2. Typical Total Gate Charge vs. Gate-to-Source Voltage

Notes:

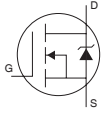
- ① Click on this section to link to the appropriate technical paper.
- ② Click on this section to link to the DirectFET Website.
- ③ Surface mounted on 1 in. square Cu board, steady state.

- ④ T_C measured with thermocouple mounted to top (Drain) of part.
- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑥ Starting $T_J = 25^\circ C$, $L = 3.2mH$, $R_G = 25\Omega$, $I_{AS} = 4.9A$.

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	17.5	22	m Ω	$V_{GS} = 10V, I_D = 8.2A$ ⑦
$V_{GS(th)}$	Gate Threshold Voltage	3.0	3.9	4.9	V	$V_{DS} = V_{GS}, I_D = 100\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-9.7	—	mV/ $^\circ\text{C}$	
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 80V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	11	—	—	S	$V_{DS} = 10V, I_D = 4.9A$
Q_g	Total Gate Charge	—	22	31	nC	$V_{DS} = 50V$ $V_{GS} = 10V$ $I_D = 4.9A$ See Fig. 15
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	4.9	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	1.2	—		
Q_{gd}	Gate-to-Drain Charge	—	6.8	10		
Q_{godr}	Gate Charge Overdrive	—	9.1	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	8.0	—		
Q_{oss}	Output Charge	—	11	—	nC	$V_{DS} = 16V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.2	—	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = 50V, V_{GS} = 10V$ ⑦ $I_D = 4.9A$ $R_G = 6.2\Omega$ See Fig. 17
t_r	Rise Time	—	7.5	—		
$t_{d(off)}$	Turn-Off Delay Time	—	24	—		
t_f	Fall Time	—	5.9	—		
C_{iss}	Input Capacitance	—	1360	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 80V, f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	270	—		
C_{rss}	Reverse Transfer Capacitance	—	61	—		
C_{oss}	Output Capacitance	—	1340	—		
C_{oss}	Output Capacitance	—	160	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	66		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 4.9A, V_{GS} = 0V$ ⑦
t_{rr}	Reverse Recovery Time	—	34	51	ns	$T_J = 25^\circ\text{C}, I_F = 4.9A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	50	75	nC	$di/dt = 100A/\mu s$ ⑦ See Fig. 18

Notes:

- ⑤ Repetitive rating; pulse width limited by max. junction temperature.
- ⑦ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

Absolute Maximum Ratings

	Parameter	Max.	Units
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation ③	2.8	W
$P_D @ T_A = 70^\circ\text{C}$	Power Dissipation ③	1.8	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation ④	89	
T_P	Peak Soldering Temperature	270	°C
T_J	Operating Junction and	-40 to + 150	
T_{STG}	Storage Temperature Range		

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③ ①	—	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ③ ②	12.5	—	
$R_{\theta JA}$	Junction-to-Ambient ⑩ ②	20	—	
$R_{\theta JC}$	Junction-to-Case ④ ①	—	1.4	
$R_{\theta J-PCB}$	Junction-to-PCB Mounted ③	1.0	—	

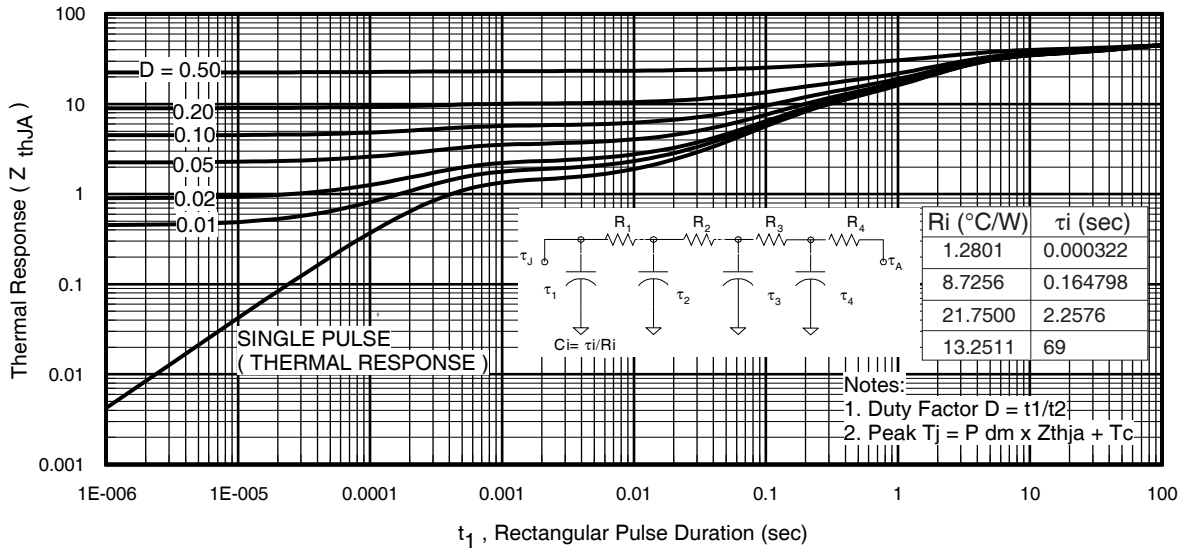
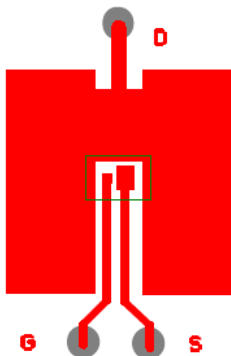


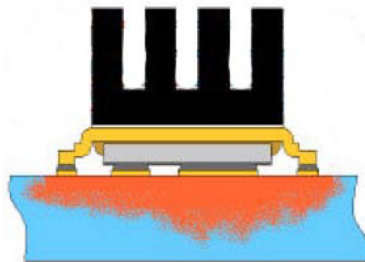
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ①

Notes:

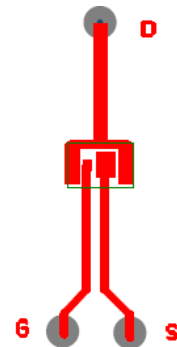
- ③ Used double sided cooling , mounting pad.
- ④ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.
- ① R_{θ} is measured at T_J of approximately 90°C .



③ Surface mounted on 1 in. square Cu (still air).



④ Mounted to a PCB with small clip heatsink (still air)



⑩ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

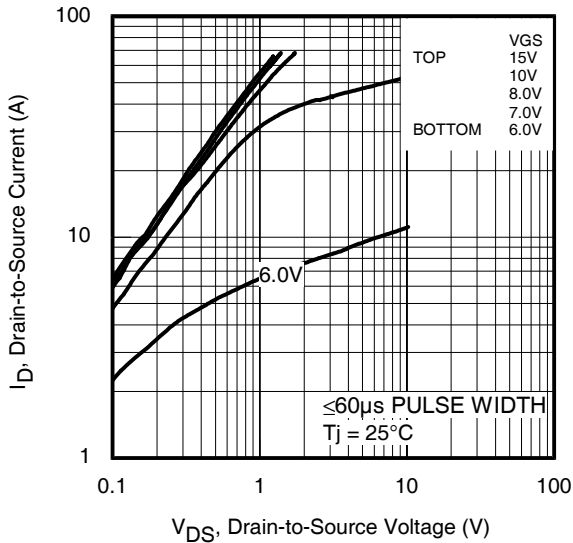


Fig 4. Typical Output Characteristics

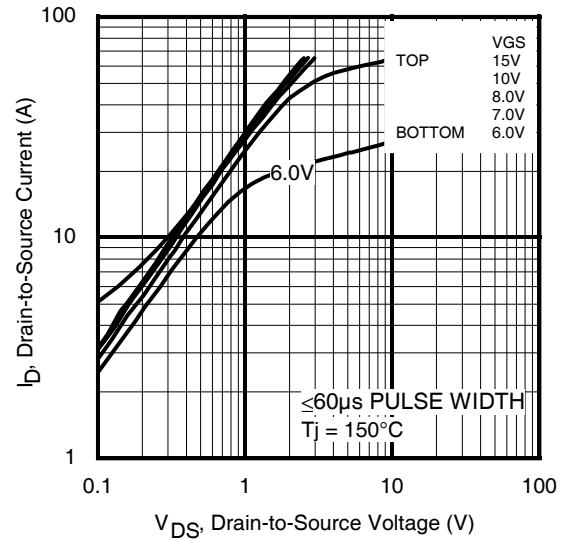


Fig 5. Typical Output Characteristics

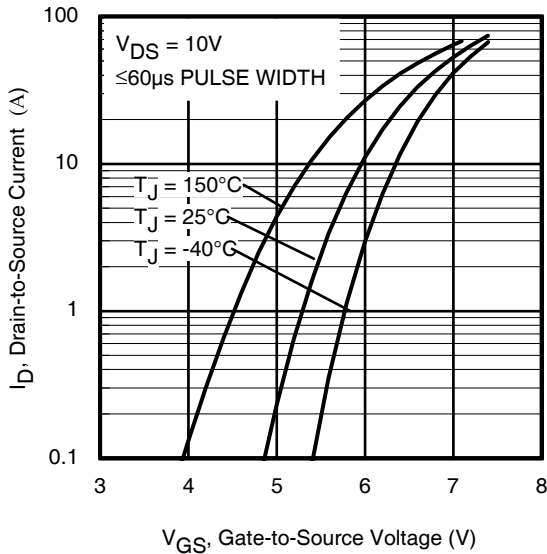


Fig 6. Typical Transfer Characteristics

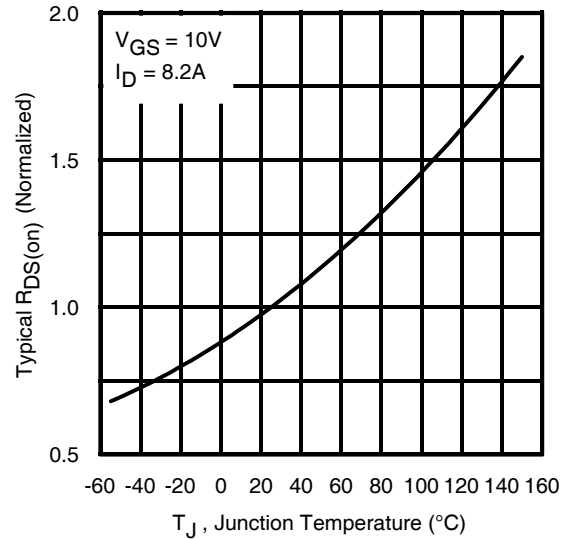


Fig 7. Normalized On-Resistance vs. Temperature

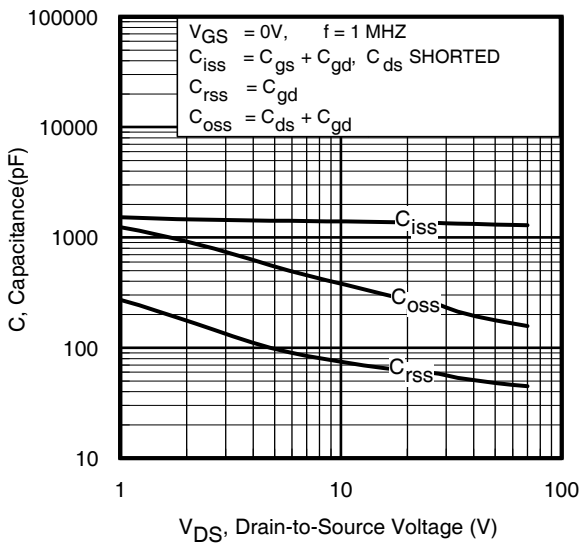


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

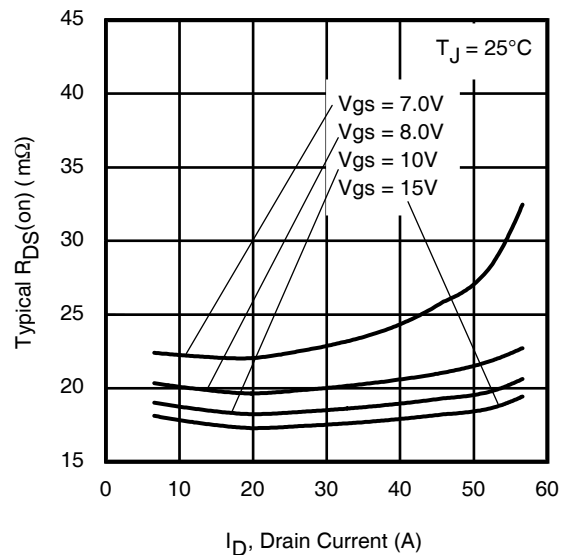


Fig 9. Typical On-Resistance vs. Drain Current

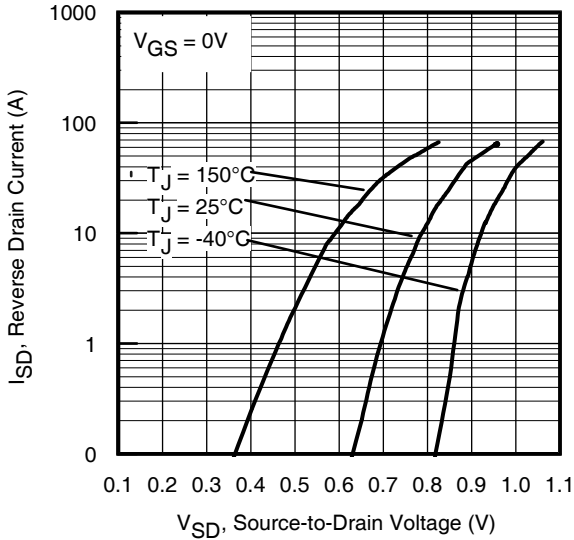


Fig 10. Typical Source-Drain Diode Forward Voltage

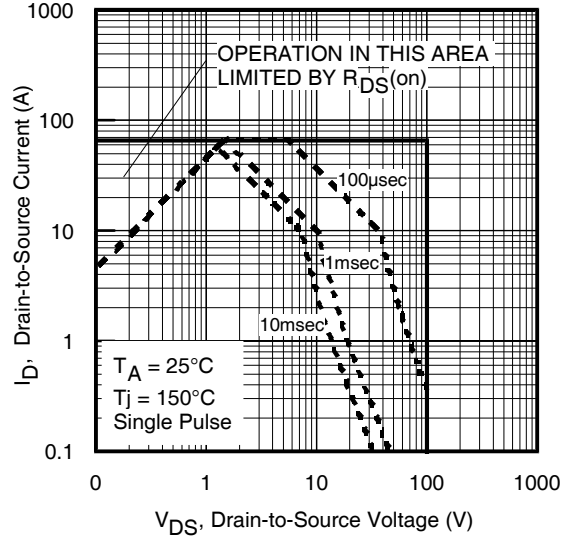


Fig 11. Maximum Safe Operating Area

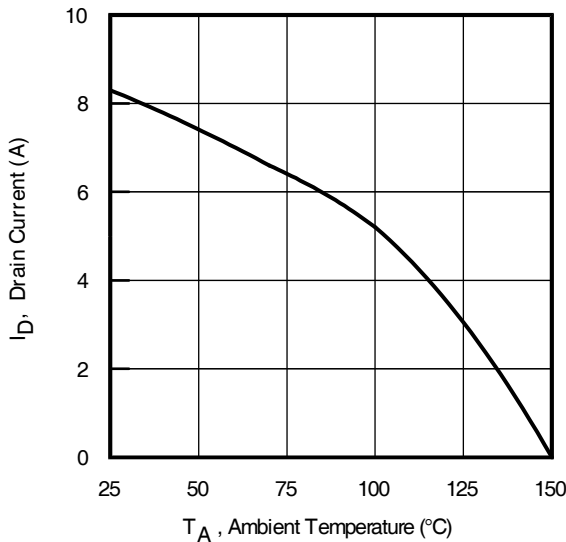


Fig 12. Maximum Drain Current vs. Ambient Temperature

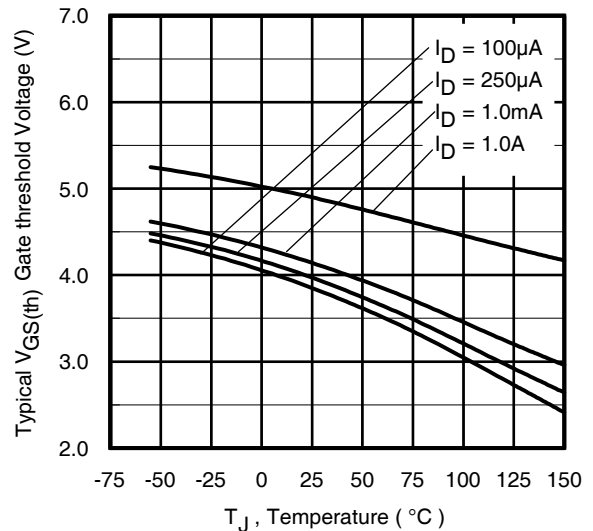


Fig 13. Typical Threshold Voltage vs. Junction Temperature

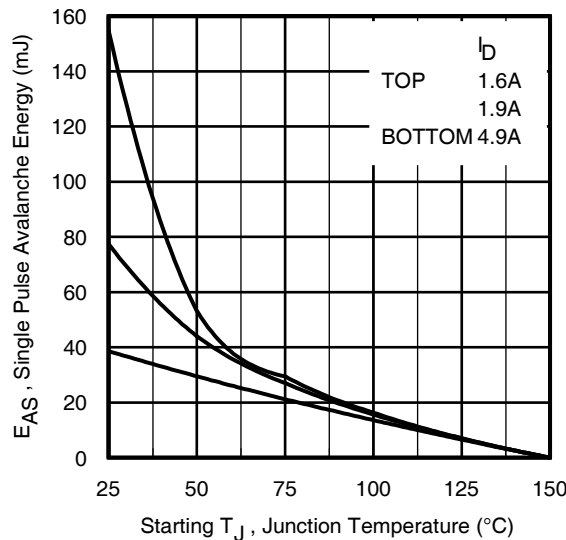


Fig 14. Maximum Avalanche Energy vs. Drain Current

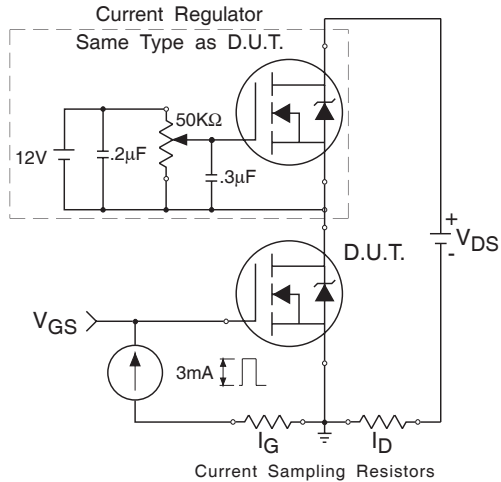


Fig 15a. Gate Charge Test Circuit



Fig 15b. Gate Charge Waveform

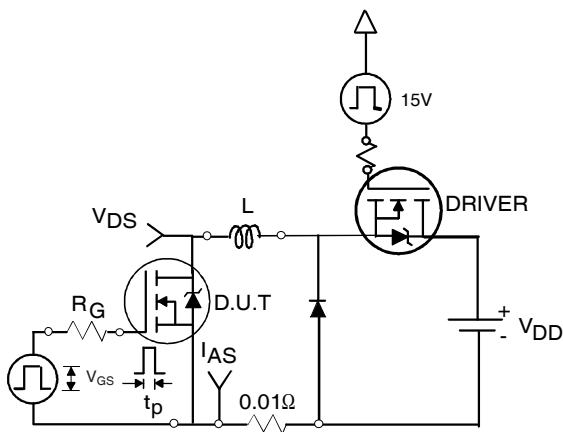


Fig 16a. Unclamped Inductive Test Circuit

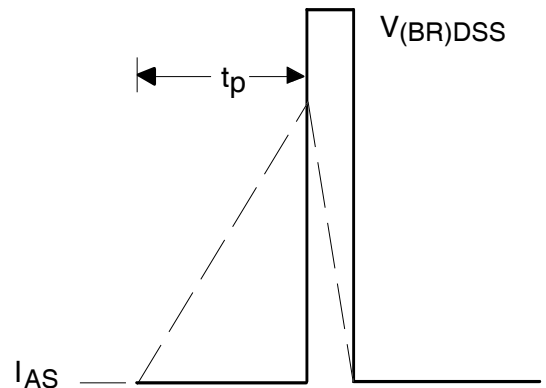


Fig 16b. Unclamped Inductive Waveforms

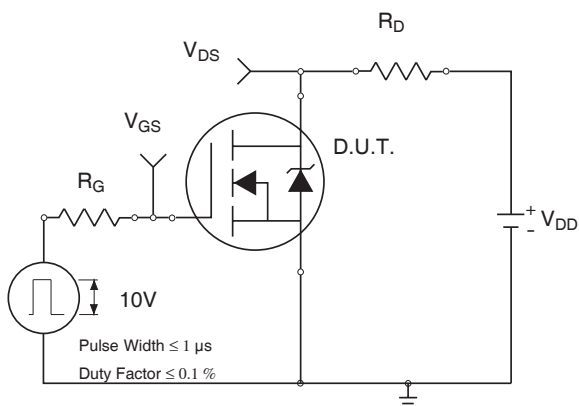


Fig 17a. Switching Time Test Circuit



Fig 17b. Switching Time Waveforms

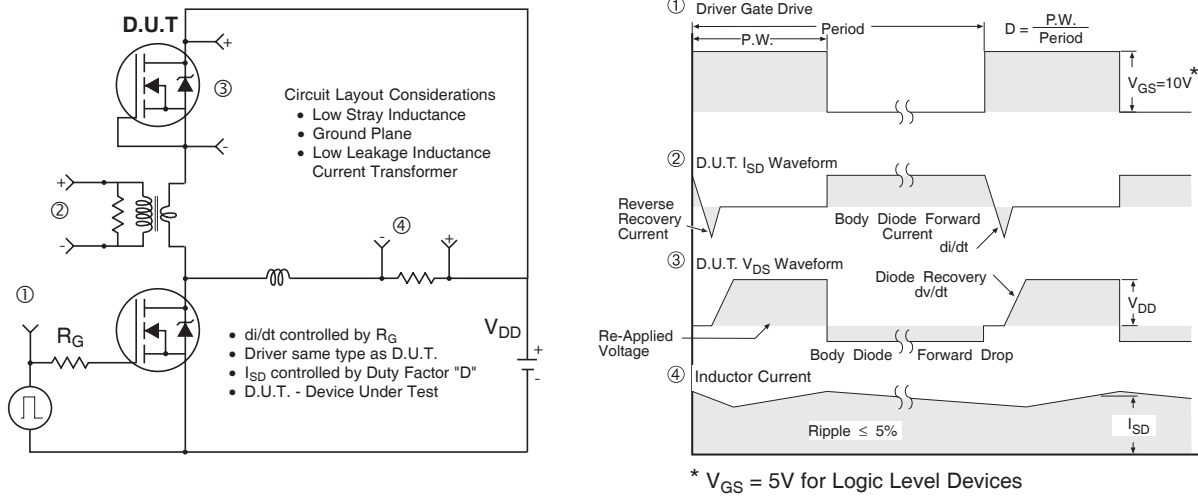
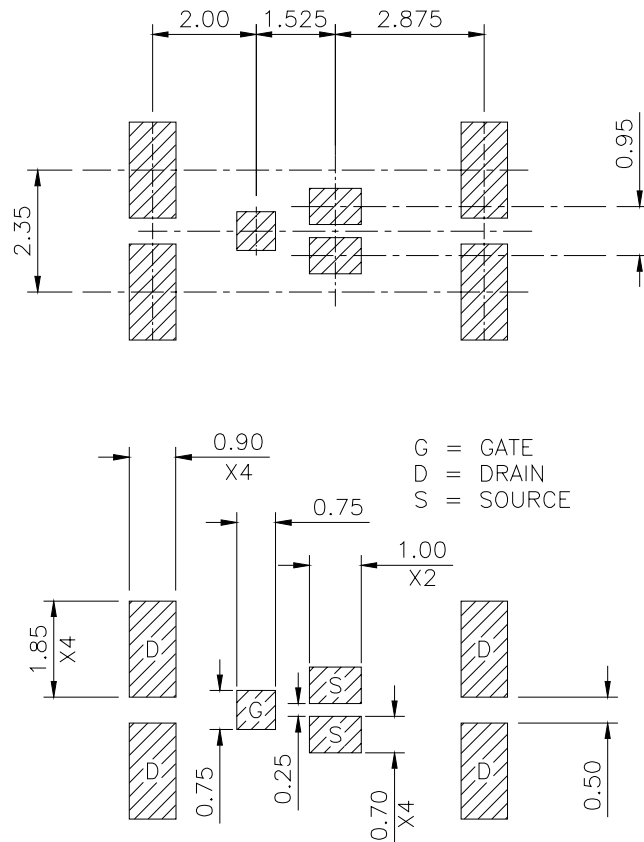


Fig 18. Diode Reverse Recovery Test Circuit for N-Channel HEXFET® Power MOSFETs

DirectFET™ Substrate and PCB Layout, MZ Outline ③ (Medium Size Can, Z-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.

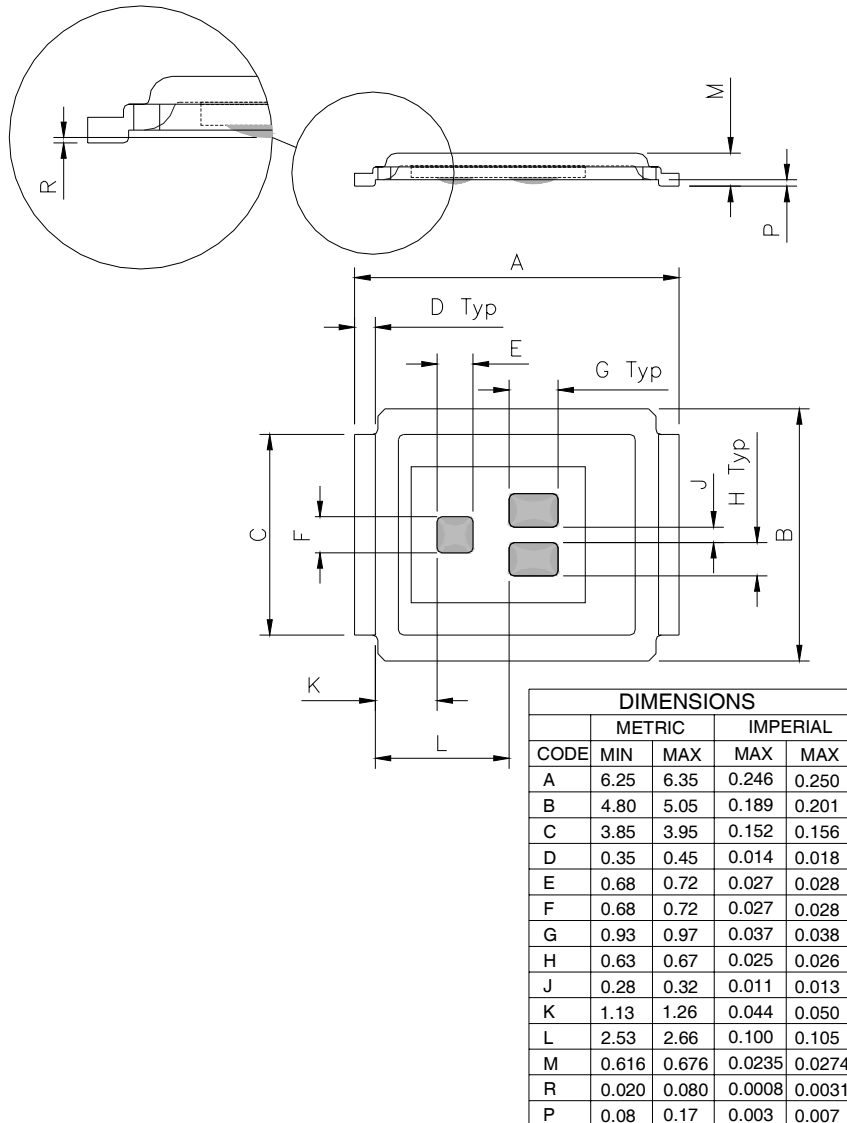


IRF6662PbF

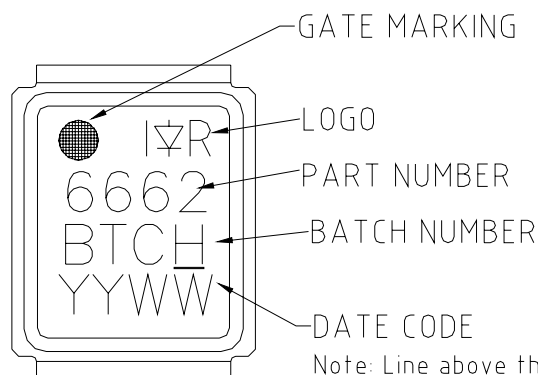
DirectFET™ Outline Dimension, MZ Outline (Medium Size Can, Z-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.

This includes all recommendations for stencil and substrate designs.

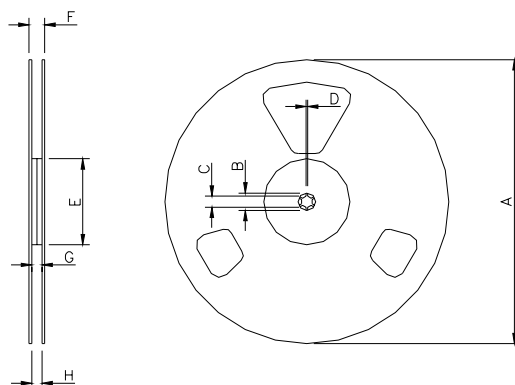


DirectFET™ Part Marking



Note: Line above the last character of the date-code indicates "Lead-Free".

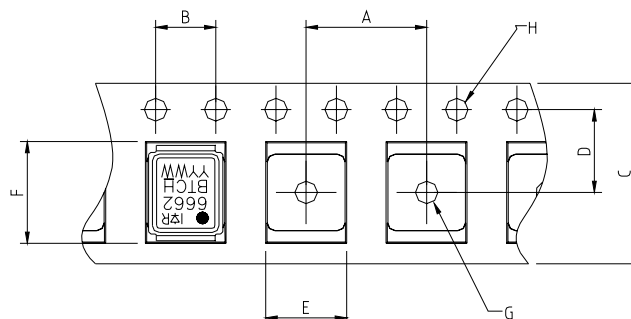
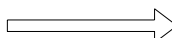
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
 Std reel quantity is 4800 parts. (ordered as IRF6662TRPBF). For 1000 parts on 7" reel, order IRF6662TR1PBF

REEL DIMENSIONS								
STANDARD OPTION (QTY 4800)					TR1 OPTION (QTY 1000)			
CODE	METRIC		IMPERIAL		METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



DIMENSIONS				
CODE	METRIC		IMPERIAL	
	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Consumer market.
 Qualification Standards can be found on IR's Web site.

Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon Technologies\(英飞凌\)](#)