MOSFET

IR MOSFET - StrongIRFET™

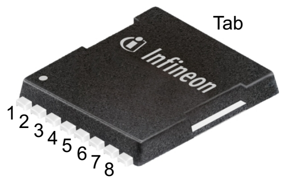
Benefits

- Improved Gate and Avalanche Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Improved I_D rating
- Pb-Free ; RoHS Compliant ; Halogen-Free

Potential applications

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

HSOF



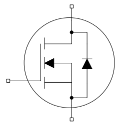


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),typ}$	0.59	mΩ
$R_{DS(on),max}$	0.72	mΩ
I_D (Silicon Limited)	586	A
I_D (Package Limited)	300	A

Type / Ordering Code	Package	Marking	Related Links
IRL40T209	PG-HSOF-8	RL40T209	-

Table of Contents

1 Maximum ratings

at *TC*=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	300 586 347	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=25 °C (silicon limited) V_{GS}=10 V, T_C=100 °C (silicon limited)[1]
Pulsed drain current[1]	$I_{D,pulse}$	-	-	1200	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	875	mJ	I_D=100 A, R_{GS}=50 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	500	W	T_C=25 °C
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom[3]	R_{thJC}	-	-	0.3	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Device on PCB, 6 cm² cooling area[1]	R_{thJA}	-	-	30	°C/W	-
Device on PCB, RTHJA(<10s)	R_{thJA}	-	-	12	°C/W	-

[1] See Diagram 3 for more detailed information
[2] See Diagram 13 for more detailed information
[3] R_{thJC} is measured at T_J approximately 90°C.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=250 µA
Breakdown voltage temperature coefficient	$dV_{(BR)DSS}/dT_j$	-	31	-	mV/°C	I_D=5 mA, referenced to 25 °C
Gate threshold voltage	$V_{GS(th)}$	1	-	2.4	V	V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	- -	- -	1 150	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	-	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	0.59 0.75	0.72 1.10	mΩ	V_{GS}=10 V, I_D=100 A V_{GS}=4.5 V, I_D=50 A
Gate resistance[1)]	R_G	-	2.0	-	Ω	-
Transconductance	g_{fs}	-	380	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=100 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	16000	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	2200	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	1600	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	60	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=30 A, $R_{G,ext}$=2.7 Ω
Rise time	t_r	-	230	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=30 A, $R_{G,ext}$=2.7 Ω
Turn-off delay time	$t_{d(off)}$	-	190	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=30 A, $R_{G,ext}$=2.7 Ω
Fall time	t_f	-	160	-	ns	V_{DD}=20 V, V_{GS}=4.5 V, I_D=30 A, $R_{G,ext}$=2.7 Ω

[1)] Defined by design. Not subject to production test.

Table 6 Gate charge characteristics[1]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	43	-	nC	V_{DD}=20 V, I_D=100 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	26	-	nC	V_{DD}=20 V, I_D=100 A, V_{GS}=0 to 4.5 V
Gate to drain charge[2]	Q_{gd}	-	83	-	nC	V_{DD}=20 V, I_D=100 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	100	-	nC	V_{DD}=20 V, I_D=100 A, V_{GS}=0 to 4.5 V
Gate charge total[2]	Q_g	-	179	269	nC	V_{DD}=20 V, I_D=100 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.6	-	V	V_{DD}=20 V, I_D=100 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	96	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 4.5 V
Output charge[1]	Q_{oss}	-	84	-	nC	V_{DD}=20 V, V_{GS}=0 V

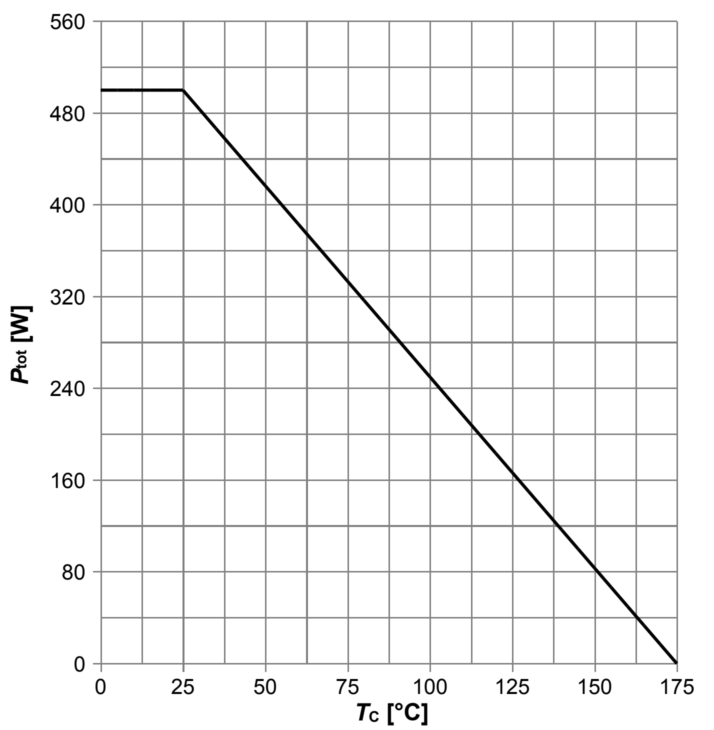
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current[3]	I_S	-	-	300	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	1200	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	-	1.2	V	V_{GS}=0 V, I_F=100 A, T_j=25 °C
Reverse recovery time[2]	t_{rr}	-	52	-	ns	V_R=34 V, I_F=100 A, di_F/dt=100 A/µs, Tj=25 °C
Reverse recovery charge[2]	Q_{rr}	-	79	-	nC	V_R=34 V, I_F=100 A, di_F/dt=100 A/µs, Tj=25 °C

[1] See ”Gate charge waveforms” for parameter definition
[2] Defined by design. Not subject to production test.
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

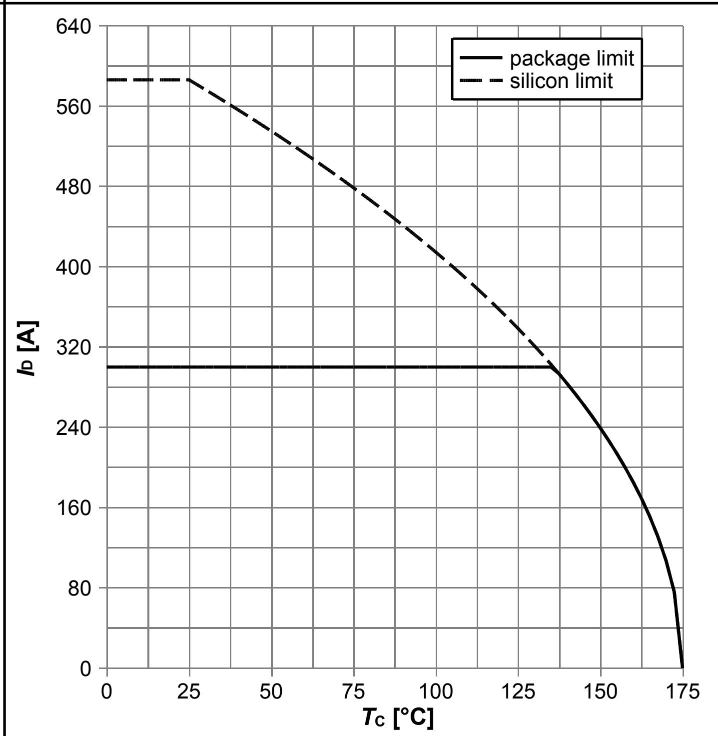
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



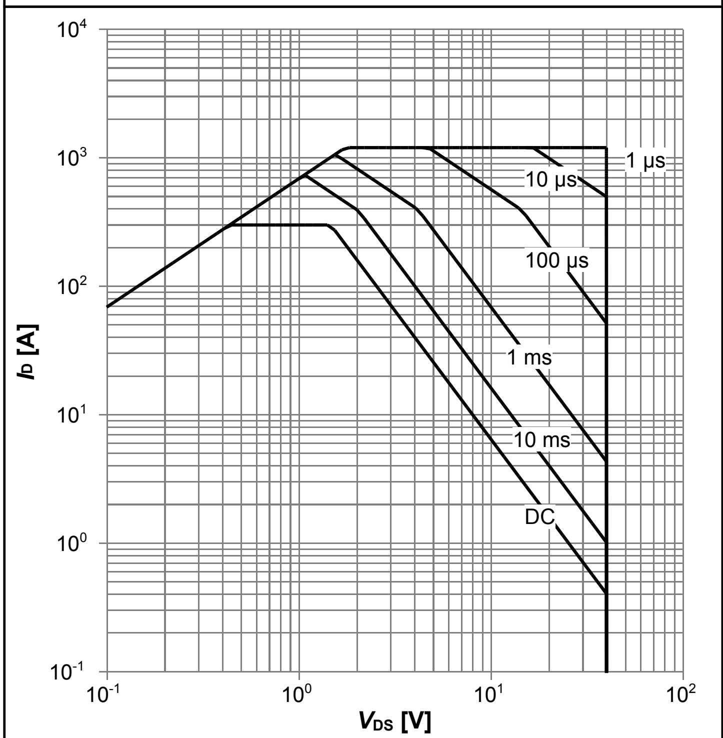
P_{tot}=f(T_C)

Diagram 2: Drain current



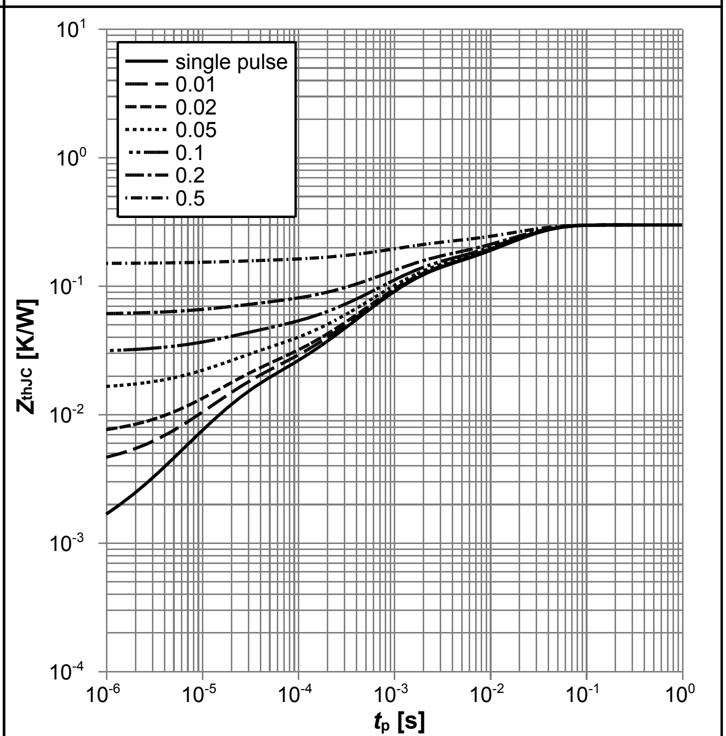
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



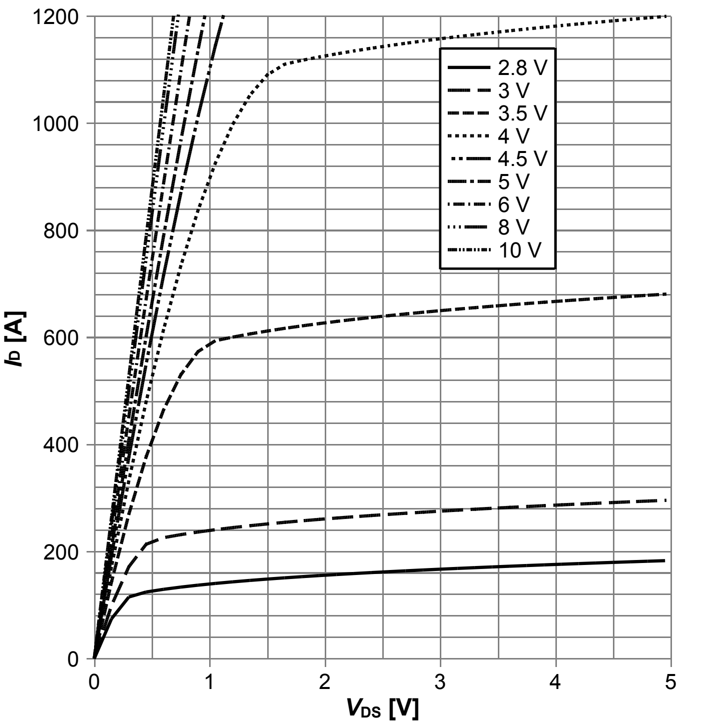
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



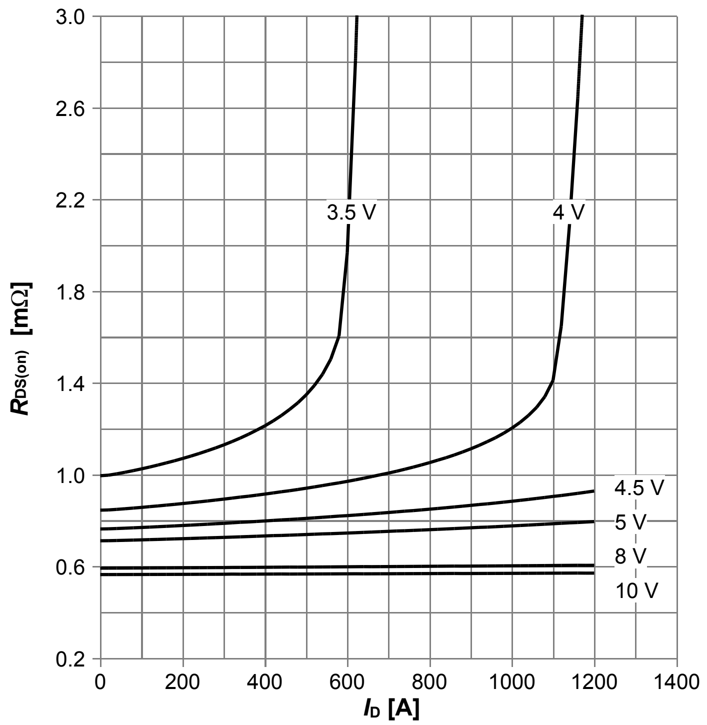
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



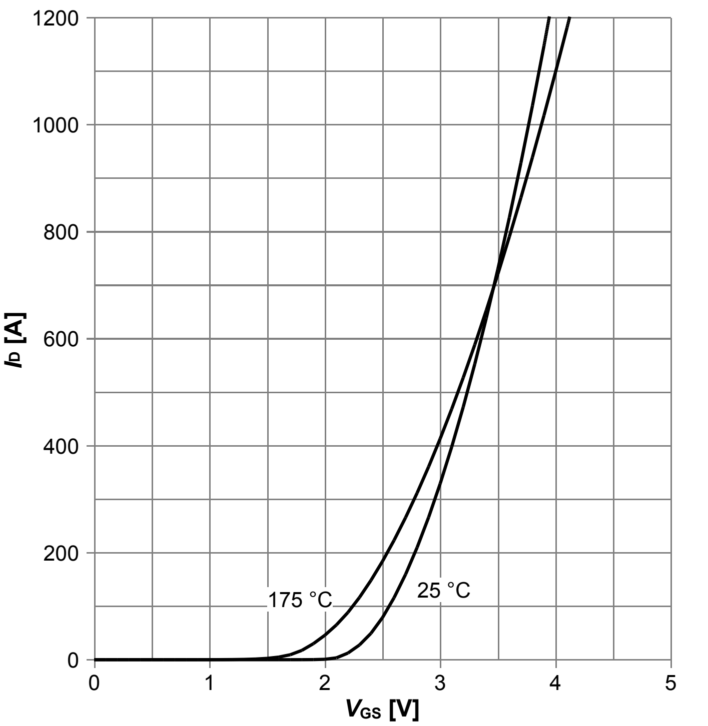
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



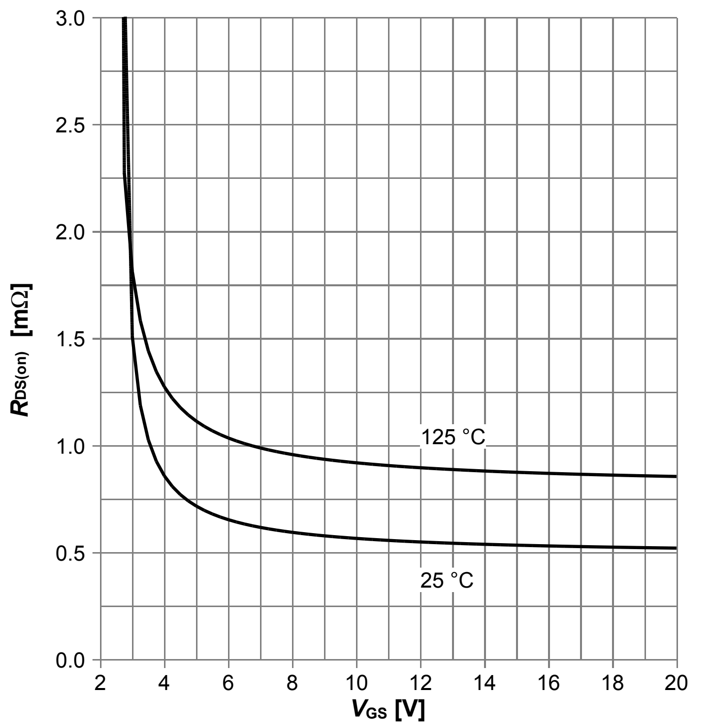
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



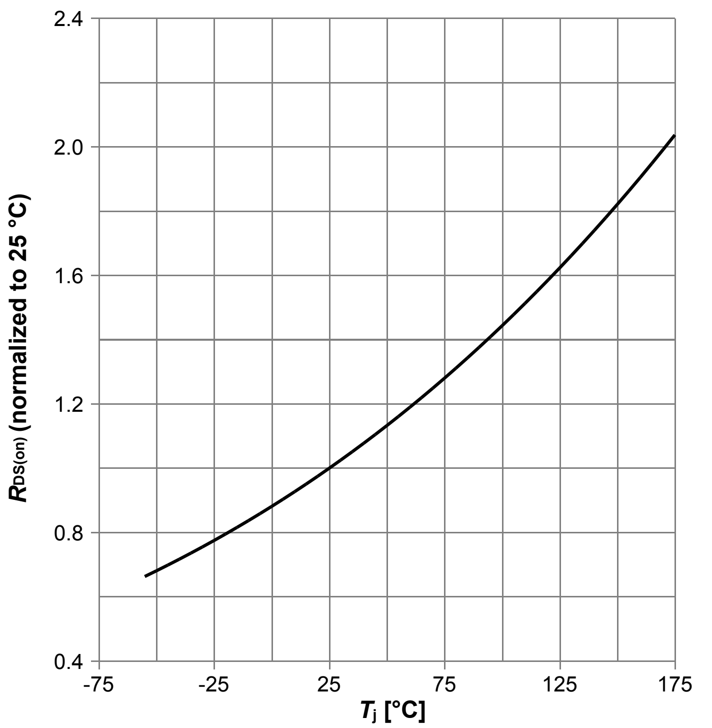
I_D=f(V_{GS}), $|V_{DS}|$>2$|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



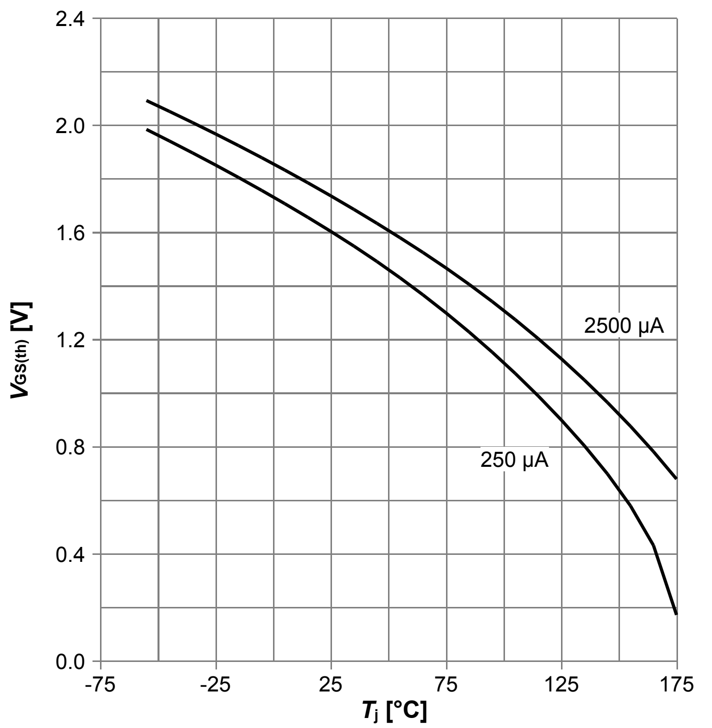
$R_{DS(on)}$=f(V_{GS}), I_D=100 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



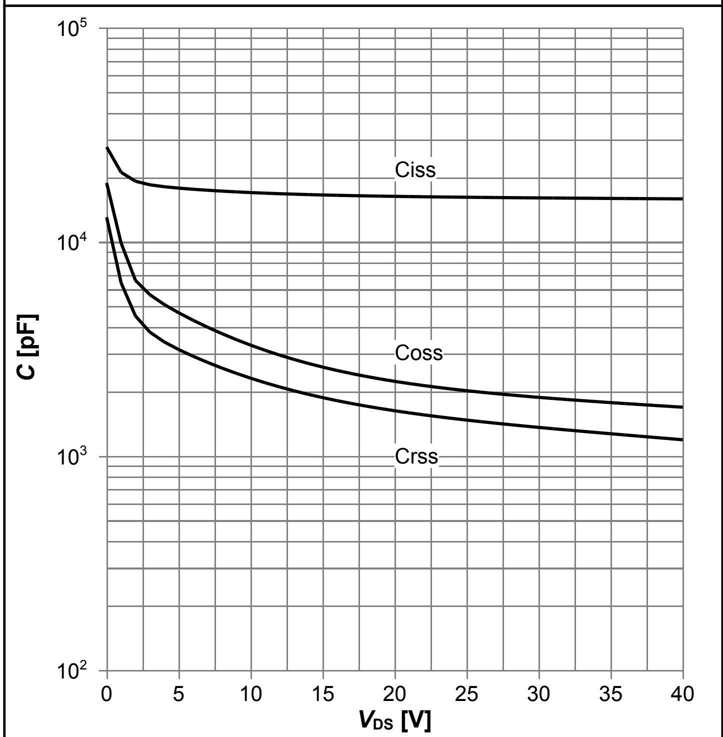
$R_{DS(on)}$=f(T_j), I_D=100 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



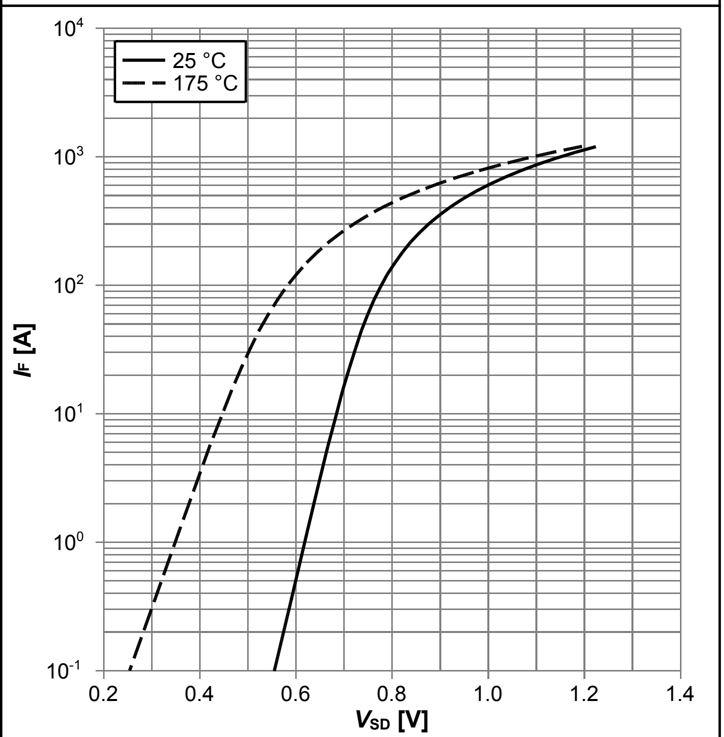
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



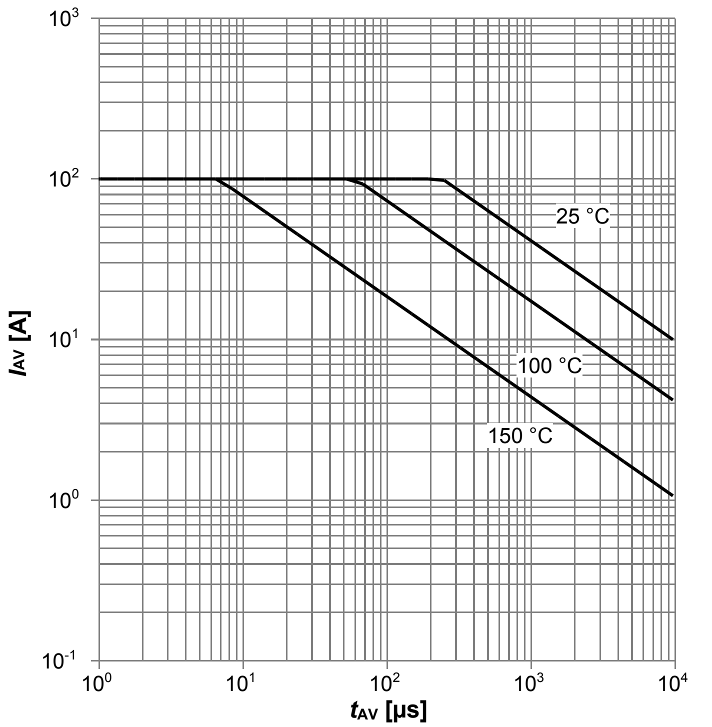
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



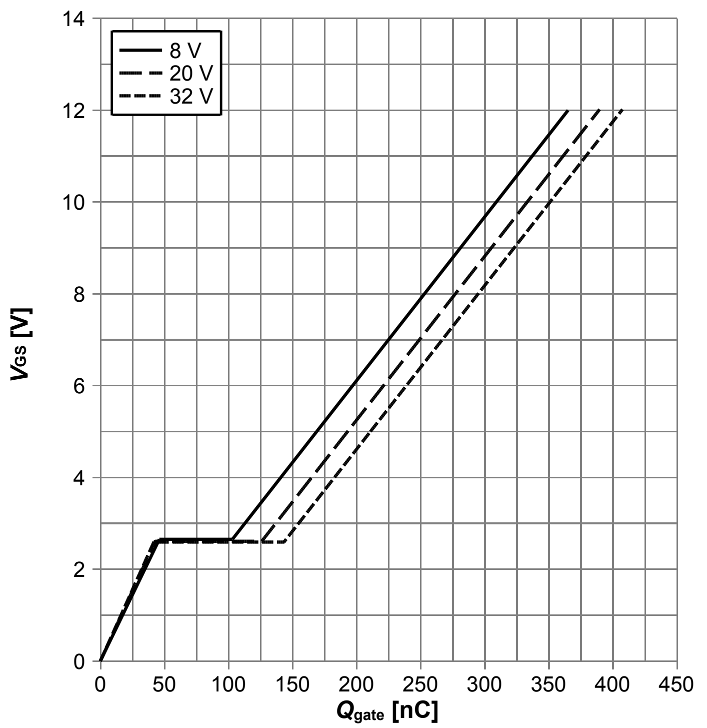
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



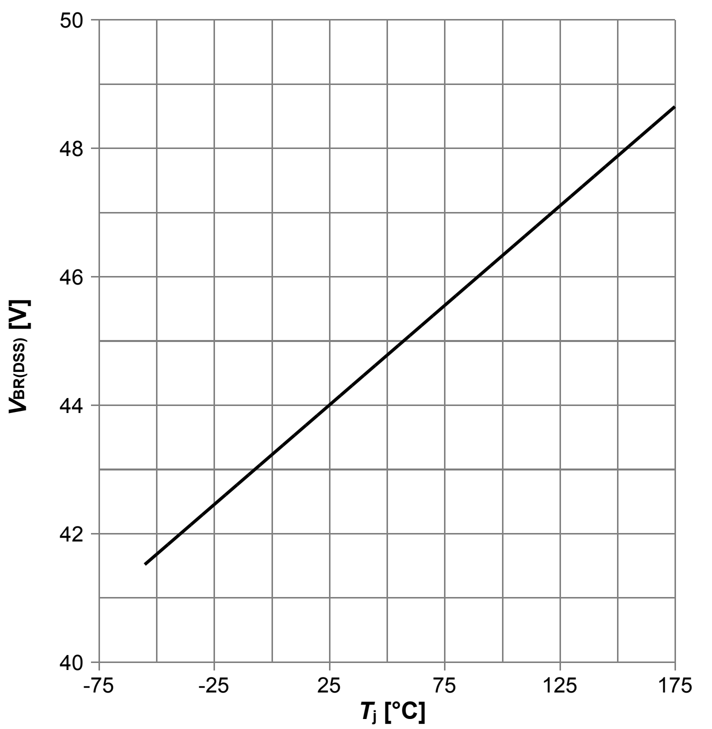
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



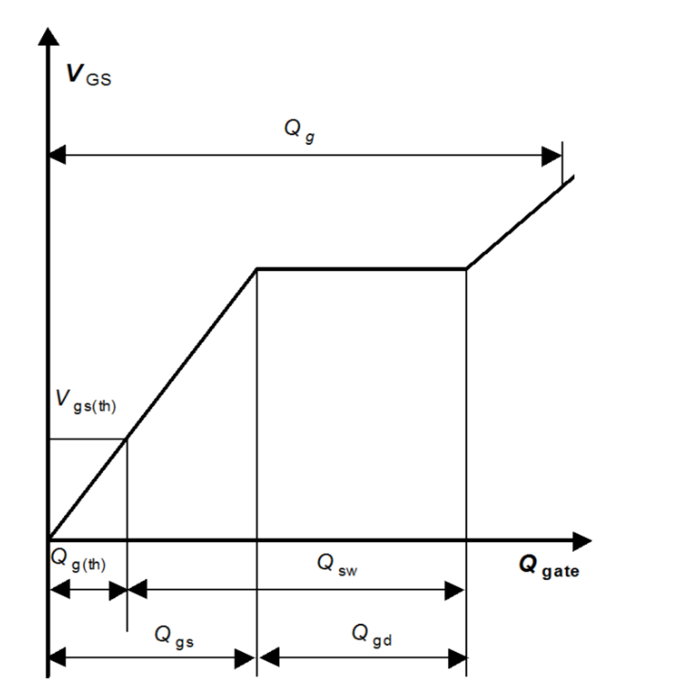
V_{GS}=f(Q_{gate}), I_D=100 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

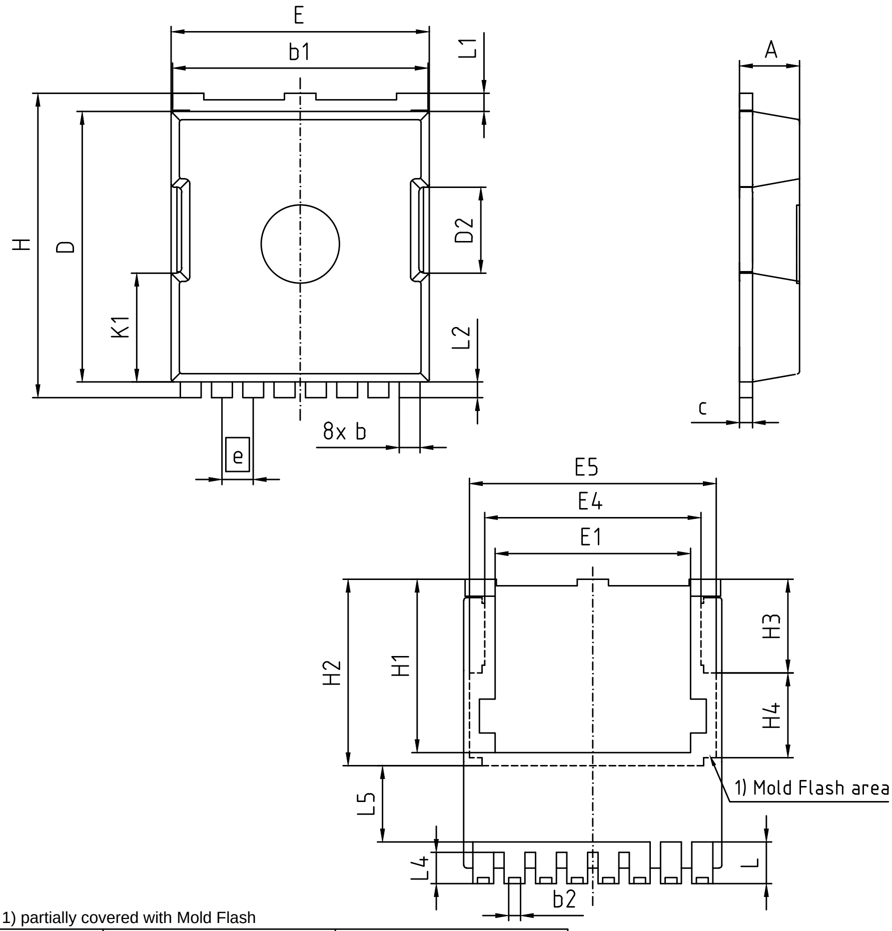


$V_{BR(DSS)}$=f(T_j); I_D=5 mA

Diagram Gate charge waveforms



5 Package Outlines



1) partially covered with Mold Flash

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.20	2.40	0.087	0.094
b	0.70	0.90	0.028	0.035
b1	9.70	9.90	0.382	0.390
b2	0.42	0.50	0.017	0.020
c	0.40	0.60	0.016	0.024
D	10.28	10.58	0.405	0.416
D2	3.30		0.130	
E	9.70	10.10	0.382	0.398
E1	7.50		0.295	
E4	8.50		0.335	
E5	9.46		0.372	
e	1.20 (BSC)		0.047 (BSC)	
H	11.48	11.88	0.452	0.468
H1	6.55	6.75	0.258	0.266
H2	7.15		0.281	
H3	3.59		0.141	
H4	3.26		0.128	
N	8		8	
K1	4.18		0.165	
L	1.40	1.80	0.055	0.071
L1	0.50	0.90	0.020	0.035
L2	0.50	0.70	0.020	0.028
L4	1.00	1.30	0.039	0.051
L5	2.62	2.81	0.103	0.111

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SCALE 0 2 4mm

EUROPEAN PROJECTION

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28-04-2015

REVISION
01

Figure 1 Outline PG-HSOF-8, dimensions in mm/inches

Revision History

IRL40T209

Revision: 2018-05-05, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
1.0	2018-04-24	Release of preliminary version
2.0	2018-05-05	Release of final version

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