PD-95860

IRHLMS797064

RADIATION HARDENED
LOGIC LEVEL POWER MOSFET
THRU-HOLE (Low-Ohmic TO-254AA)

60V, P-CHANNEL
R7 TECHNOLOGY

Low-Ohmic
TO-254AA

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHLMS797064	100 kRads(Si)	0.018Ω	-45A*
IRHLMS793064	300 kRads(Si)	0.018Ω	-45A*

Description

IR HiRel R7 Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

The device is ideal when used to interface directly with most logic gates, linear IC's, micro-controllers, and other device types that operate from a 3.3-5V source. It may also be used to increase the output current of a PWM, voltage comparator or an operational amplifier where the logic level drive signal is available.

Features

- Low R_{DS}(on)
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Ceramic Eyelets
- Electrically Isolated
- Light Weight
- ESD Rating: Class 3B per MIL-STD-750, Method 1020

Absolute Maximum Ratings — Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 4.5V, T_C = 25°C	Continuous Drain Current	-45*	A
I_D @ V_{GS} = 4.5V, T_C = 100°C	Continuous Drain Current	-45*	
I_{DM}	Pulsed Drain Current ①	-180	
P_D @T_C = 25°C	Maximum Power Dissipation	208	W
	Linear Derating Factor	1.67	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	935	mJ
I_{AR}	Avalanche Current ①	-45	A
E_{AR}	Repetitive Avalanche Energy ①	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-6.3	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C
	Lead Temperature	300 (0.063 in. /1.6 mm from case for 10s)	
	Weight	9.3 (Typical)	g

*Current is limited by package
For footnotes refer to the page 2.

2017-06-16

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	——	——	V	V_{GS} = 0V, I_D = -250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	-0.06	——	V/°C	Reference to 25°C, I_D = -1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.018	Ω	V_{GS} = -4.5V, I_D = -45A* ④
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	——	-2.0	V	V_{DS} = V_{GS}, I_D = -250μA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	——	5.5	——	mV/°C	
gfs	Forward Transconductance	-52	——	——	S	V_{DS} = -10V, I_D = -45A ④
I_{DSS}	Zero Gate Voltage Drain Current	——	——	-1.0	μA	V_{DS} = -48V, V_{GS} = 0V
		——	——	-25		V_{DS} = -48V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	——	——	-100	nA	V_{GS} = -10V
	Gate-to-Source Leakage Reverse	——	——	100		V_{GS} = 10V
Q_G	Total Gate Charge	——	——	123	nC	I_D = -45A
Q_{GS}	Gate-to-Source Charge	——	——	62		V_{DS} = -30V
Q_{GD}	Gate-to-Drain ('Miller') Charge	——	——	50		V_{GS} = -4.5V
$t_{d(on)}$	Turn-On Delay Time	——	——	54	ns	V_{DD} = -30V
t_r	Rise Time	——	——	400		I_D = -45A
$t_{d(off)}$	Turn-Off Delay Time	——	——	120		R_G = 2.35Ω
t_f	Fall Time	——	——	138		V_{GS} = -4.5V
Ls +L_D	Total Inductance	——	6.8	——	nH	Measured from Drain lead (6mm/ 0.25 in from package) to Source lead (6mm/0.25 in from package)
C_{iss}	Input Capacitance	——	7540	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	2760	——		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	——	350	——		f = 1.0MHz
R_G	Gate Resistance	——	2.4	——	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	——	——	-45*	A	
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	-180		
V_{SD}	Diode Forward Voltage	——	——	-5.0	V	T_J= 25°C,I_S = -45A, V_{GS}= 0V ④
t_{rr}	Reverse Recovery Time	——	——	120	ns	T_J= 25°C ,I_F = -45A, V_{DD} ≤ −25V
Q_{rr}	Reverse Recovery Charge	——	——	375	μC	di/dt = -100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

* Current is limited by package

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	0.60	°C/W
$R_{\theta CS}$	Case -to-Sink	——	0.21	——	
$R_{\theta JA}$	Junction-to-Ambient (Typical Socket Mount)	——	——	48	

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = -50V, starting T_J = 25°C, L =0.92mH, Peak I_L = -45A, V_{GS} = -10V

③ I_{SD} ≤ -45A, di/dt ≤ -790A/μs, V_{DD} ≤ -60V, T_J ≤ 150°C

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** -10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** -48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, Method 1019, condition A.

Radiation Characteristics

IR HiRel Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 300 kRads(Si) [1]		Units	Test Conditions
		Min.	Max.		
BV_{DSS}	Drain-to-Source Breakdown Voltage	-60	——	V	V_{GS} = 0V, I_D = -250μA
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	-2.0	V	V_{DS} = V_{GS}, I_D = -250μA
I_{GSS}	Gate-to-Source Leakage Forward	——	-100	nA	V_{GS} = -10V
I_{GSS}	Gate-to-Source Leakage Reverse	——	100	nA	V_{GS} = 10V
I_{DSS}	Zero Gate Voltage Drain Current	——	1.0	μA	V_{DS} = -48V, V_{GS} = 0V
$R_{DS(on)}$	Static Drain-to-Source On-State ④ Resistance (TO-3)	——	0.019	Ω	V_{GS} = -4.5V, I_D = -45A
$R_{DS(on)}$	Static Drain-to-Source On--State ④ Resistance (Low Ohmic TO-254AA)	——	0.018	Ω	V_{GS} = -4.5V, I_D = -45A
V_{SD}	Diode Forward Voltage	——	-5.0	V	V_{GS} = 0V, I_D = -45A

1. Part numbers IRHLMS797064 and IRHLMS793064

IR HiRel radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area

LET (MeV/(mg/cm²))	Energy (MeV)	Range (μm)	V_{DS} (V)					
			@VGS=0V	@VGS=2V	@VGS=3V	@VGS=4V	@VGS=5V	@VGS=6V
32.4	679	83.3	-60	-60	-60	-60	-60	-60
61.7	584	48.7	-60	-60	-60	-60	——	——
92.3	1156	65.1	-40	——	——	——	——	——

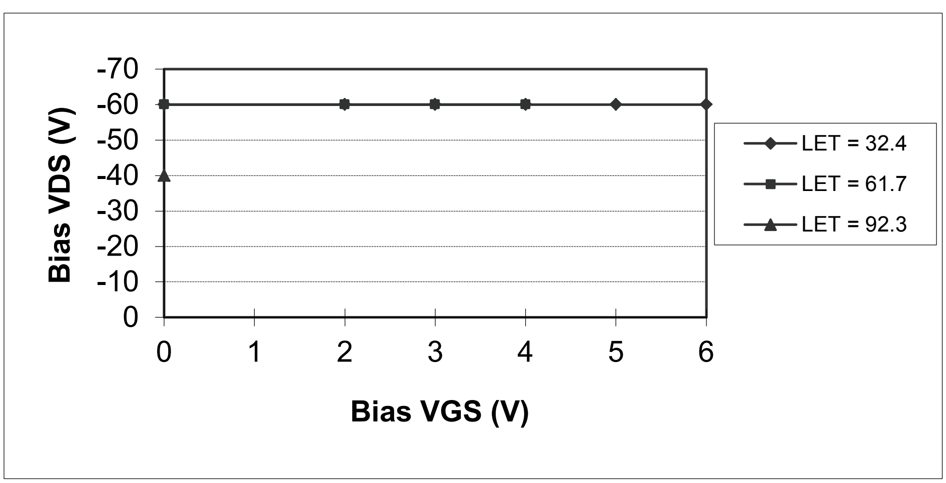


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the page 2.

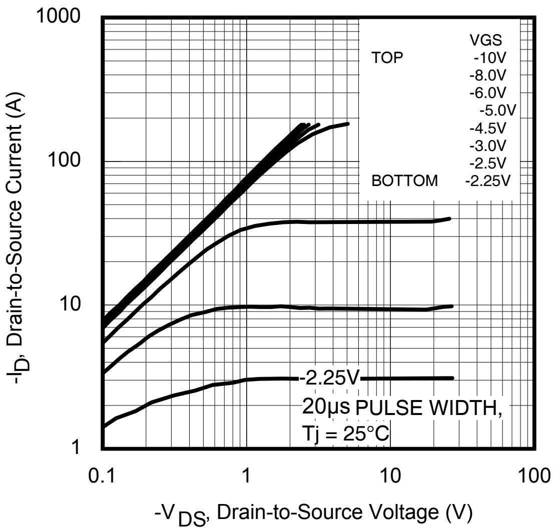


Fig 1. Typical Output Characteristics

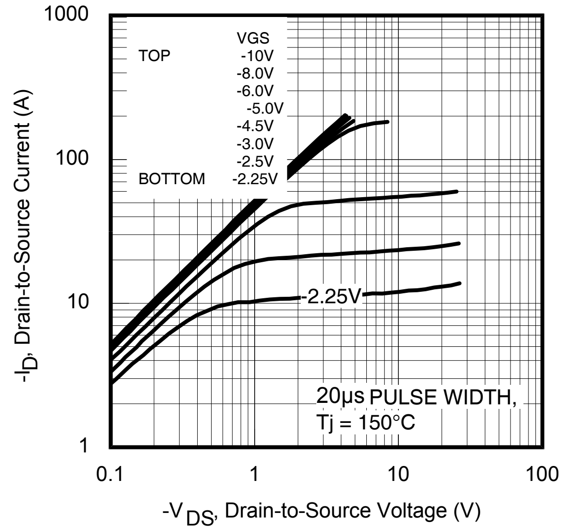


Fig 2. Typical Output Characteristics

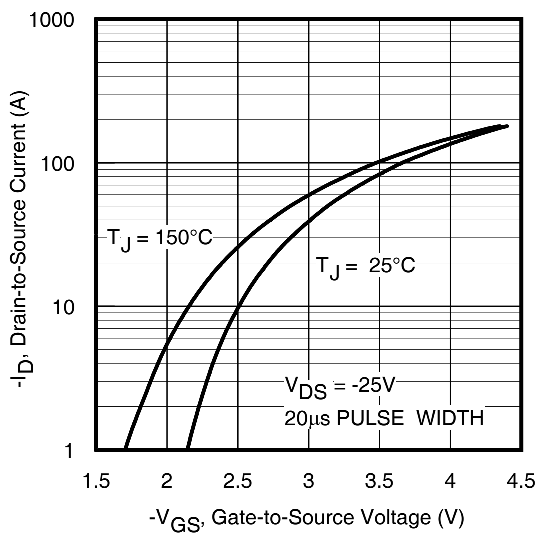


Fig 3. Typical Transfer Characteristics

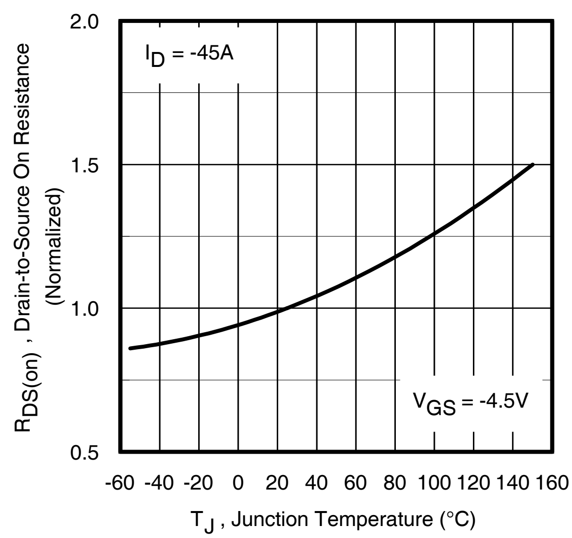


Fig 4. Normalized On-Resistance Vs. Temperature

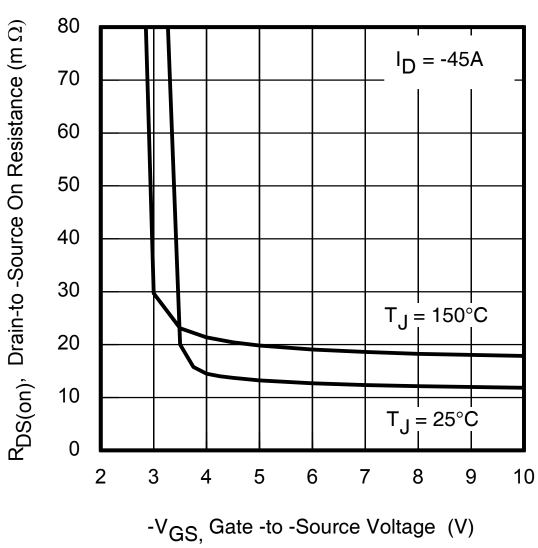


Fig 5. Typical On-Resistance Vs Gate Voltage

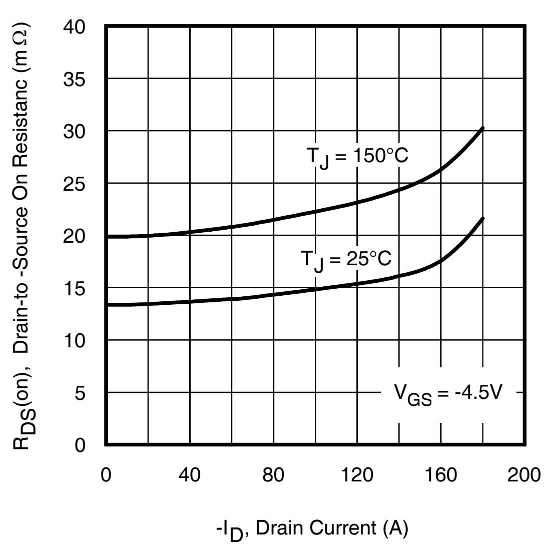


Fig 6. Typical On-Resistance Vs Drain Current

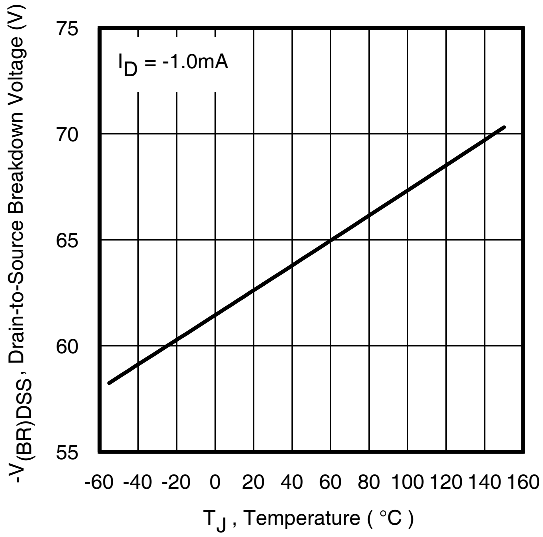


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

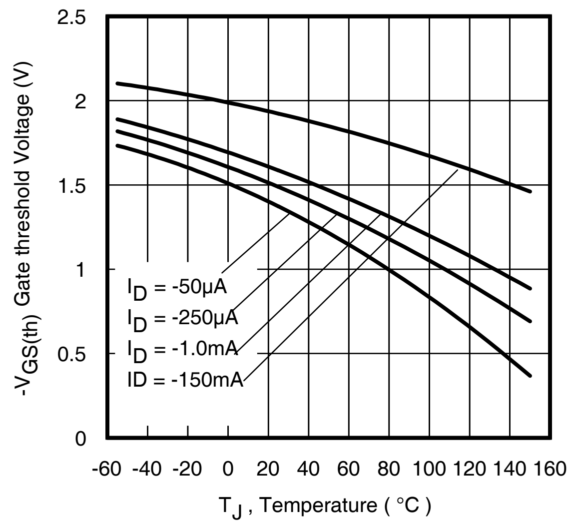


Fig 8. Typical Threshold Voltage Vs Temperature

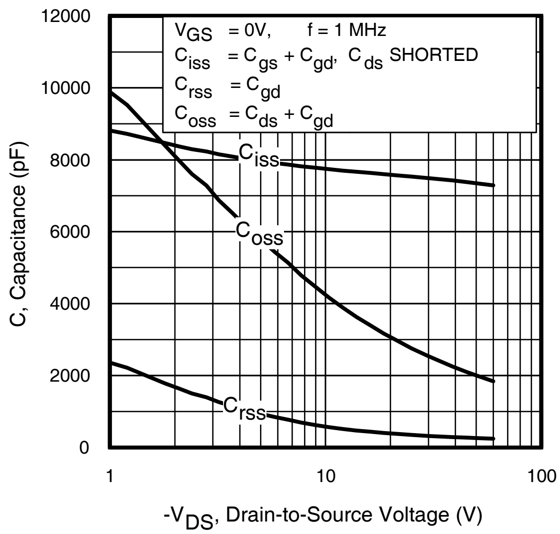


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

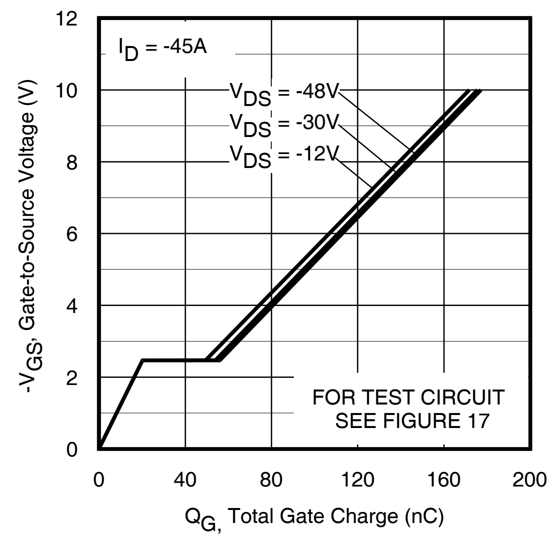


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

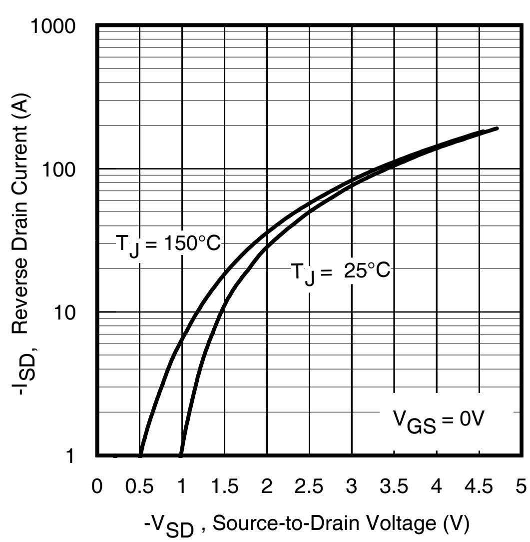


Fig 11. Typical Source-Drain Diode Forward Voltage

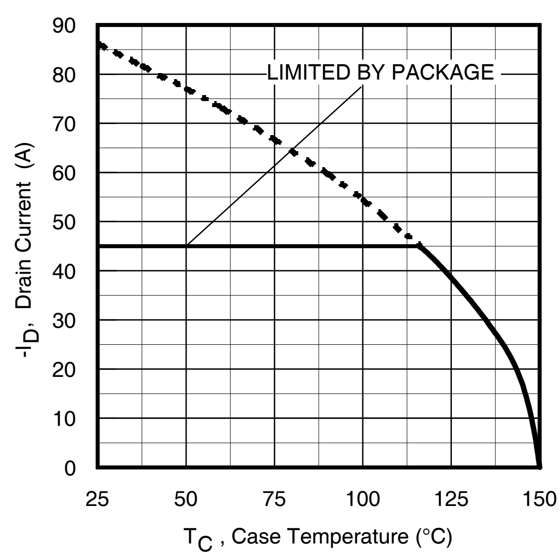


Fig 12. Maximum Drain Current Vs.Case Temperature

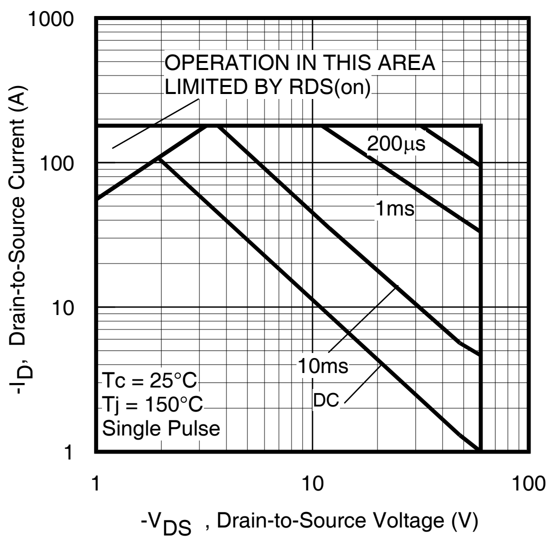


Fig 13. Maximum Safe Operating Area

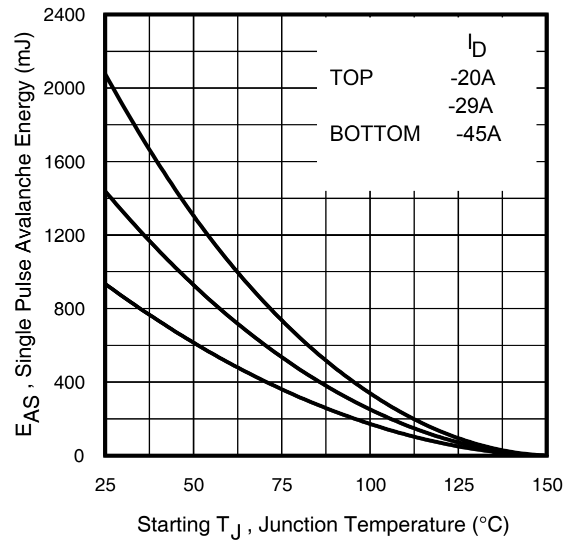


Fig 14. Maximum Avalanche Energy Vs. Drain Current

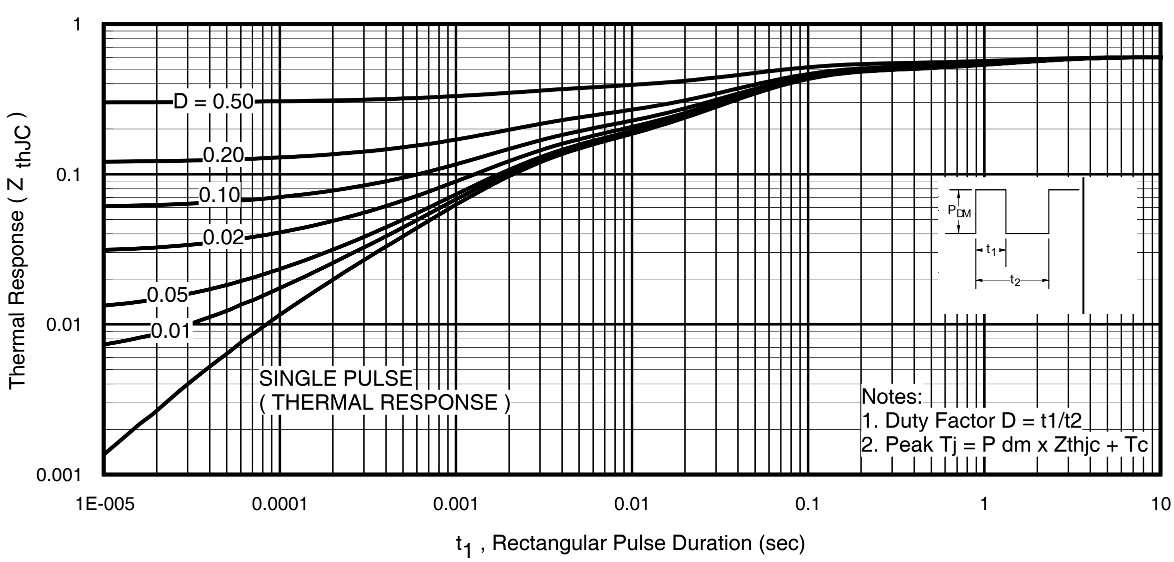


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Case

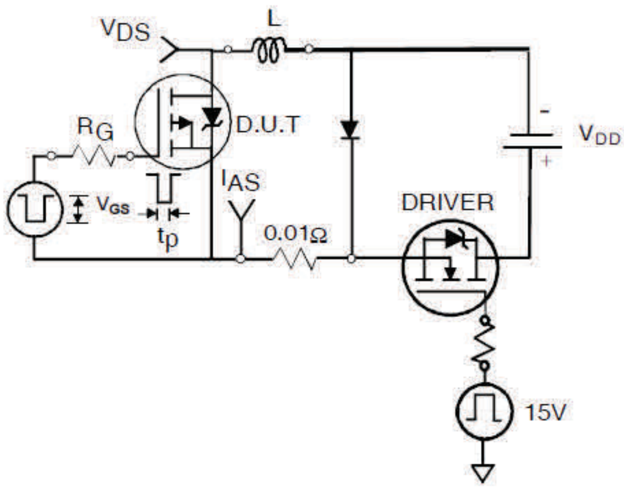


Fig 16a. Unclamped Inductive Test Circuit

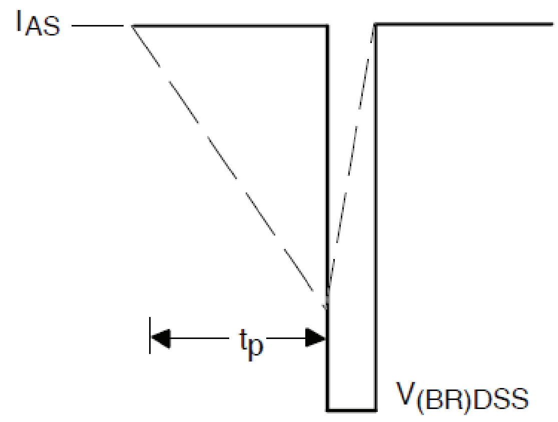


Fig 16b. Unclamped Inductive Waveforms

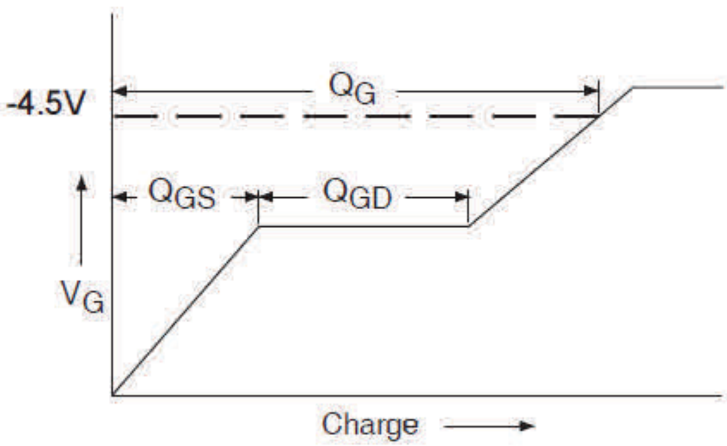


Fig 17a. Gate Charge Waveform

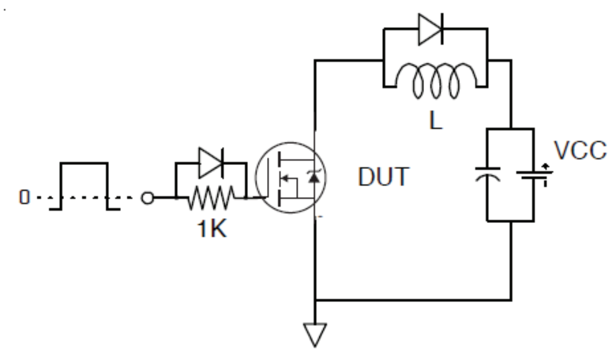


Fig 17b. Gate Charge Test Circuit

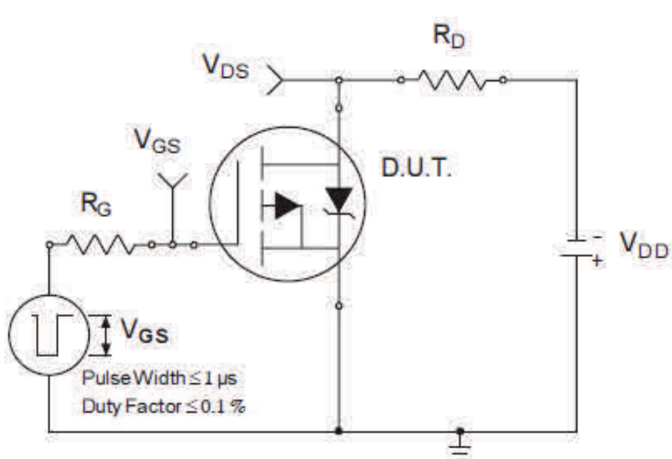


Fig 18a. Switching Time Test Circuit

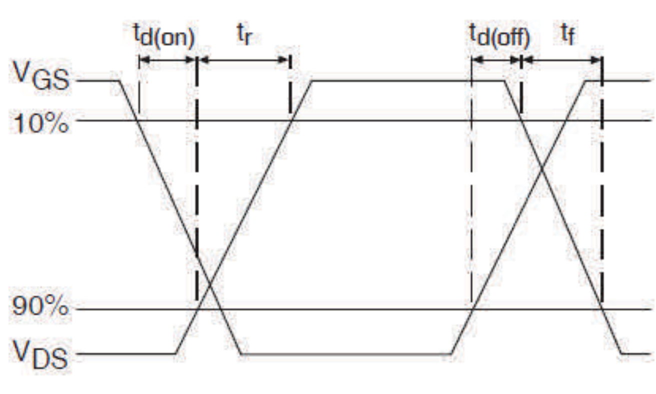
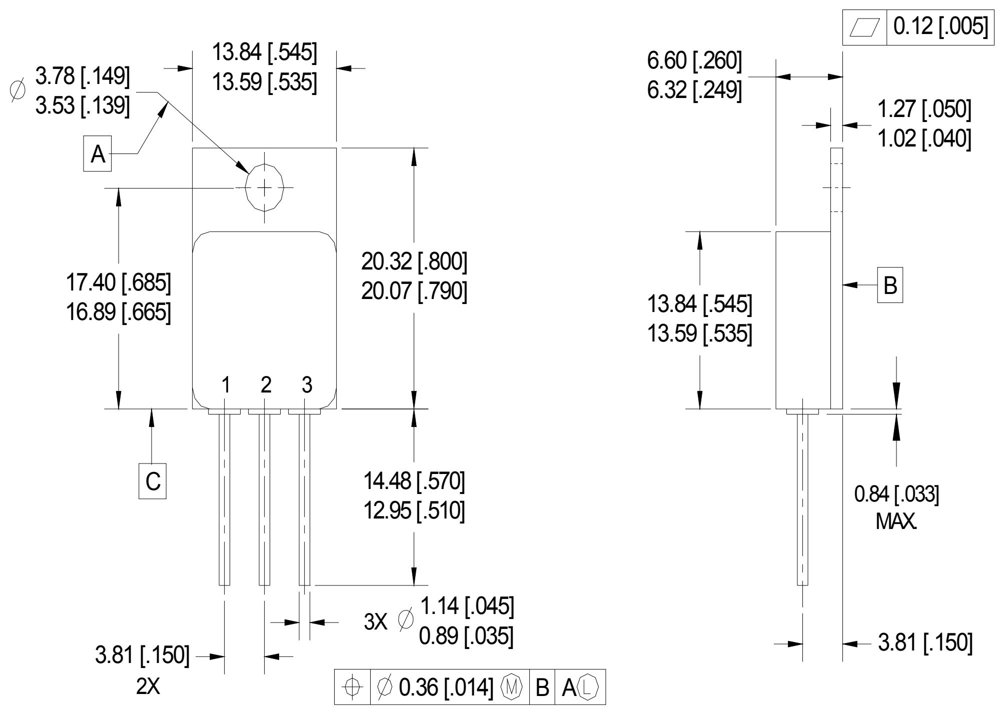


Fig 18b. Switching Time Waveforms

Case Outline and Dimensions - Low-Ohmic TO-254AA



NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-254AA.

PIN ASSIGNMENTS

1 = DRAIN
2 = SOURCE
3 = GATE

BERYLLIA WARNING PER MIL-PRF-19500

Package containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.

An Infineon Technologies Company

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