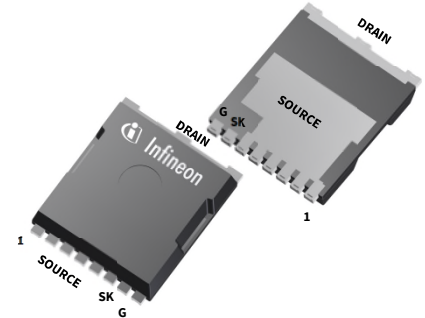


IGT60R042D1

600V CoolGaN™ enhancement-mode Power Transistor

Features

- Enhancement mode transistor – Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- Qualified for industrial applications according to JEDEC Standards (JESD47 and JESD22)



Benefits

- Improves system efficiency
- Improves power density
- Enables higher operating frequency
- System cost reduction savings
- Reduces EMI

Gate	8
Drain	drain contact
Kelvin Source	7
Source	1,2,3,4,5,6

Applications

Industrial, telecom, datacenter SMPS based on the half-bridge topology (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC).

For other applications: review CoolGaN™ reliability white paper and contact Infineon regional support

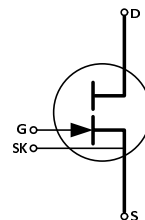


Table 1 Key Performance Parameters at T_j = 25 °C

Parameter	Value	Unit
V _{DS,max}	600	V
R _{DS(on),max}	42	mΩ
Q _{G,typ}	8.8	nC
I _{D,pulse}	90	A
Q _{oss @ 400 V}	62	nC
Q _{rr}	0	nC



Table 2 Ordering Information

Type / Ordering Code	Package	Marking	Related links
IGT60R042D1	PG-HSOF-8-3	60R042D1	see Appendix A

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1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact your local Infineon sales office.

Table 3 Maximum ratings

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Drain Source Voltage, continuous ¹	$V_{DS,max}$	-	-	600	V	$V_{GS} = 0\text{ V}$
Drain source destructive breakdown voltage ²	$V_{DS,bd}$	800	-	-	V	$V_{GS} = 0\text{ V}$, $I_{DS} = 19.8\text{ mA}$
Drain source voltage, pulsed ²	$V_{DS,pulse}$	-	-	750	V	$T_j = 25\text{ °C}$; $V_{GS} \leq 0\text{ V}$; ≤ 1 hour of total time
		-	-	650	V	$T_j = 125\text{ °C}$, $V_{GS} \leq 0\text{ V}$; ≤ 1 hour of total time
Switching surge voltage, pulsed ²	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse} = 750\text{ V}$; turn on $I_{D,pulse} = 43\text{ A}$; $T_j = 105\text{ °C}$; $f \leq 100\text{ kHz}$, $t \leq 100\text{ secs}$ (10 million pulses)
Continuous current, drain source	I_D	-	-	23	A	$T_C = 125\text{ °C}$; $T_j = T_{j,max}$
Pulsed current, drain source ^{3 4}	$I_{D,pulse}$	-	-	90	A	$T_C = 25\text{ °C}$; $I_G = 83.8\text{ mA}$; See Figure 3;
Pulsed current, drain source ^{4 5}	$I_{D,pulse}$	-	-	45	A	$T_C = 125\text{ °C}$; $I_G = 83.8\text{ mA}$; See Figure 4;
Gate current, continuous ^{4 5 6}	$I_{G,avg}$	-	-	64	mA	$T_j = -55\text{ °C}$ to 150 °C ;
Gate current, pulsed ^{4 6}	$I_{G,pulse}$	-	-	3200	mA	$T_j = -55\text{ °C}$ to 150 °C ; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$
Gate source voltage, continuous ⁶	V_{GS}	-10	-	-	V	$T_j = -55\text{ °C}$ to 150 °C ;
Gate source voltage, pulsed ⁶	$V_{GS,pulse}$	-25	-	-	V	$T_j = -55\text{ °C}$ to 150 °C ; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	-	-	205	W	$T_C = 25\text{ °C}$
Operating temperature	T_j	-55	-	150	°C	
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions.
Drain-source voltage slew-rate	dV/dt			200	V/ns	

¹ All devices are 100% tested at $I_{DS} = 19.8\text{ mA}$ to assure $V_{DS} \geq 800\text{ V}$

² Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation

³ Limits derived from product characterization, parameter not measured during production

⁴ Ensure that average gate drive current, $I_{G,avg}$ is $\leq 64\text{ mA}$. Please see figure 27 for $I_{G,avg}$, $I_{G,pulse}$ and I_G details

⁵ Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application

⁶ We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for details

2 Thermal characteristics

Table 4 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	0.61	°C/W	
Thermal resistance, junction-ambient	R_{thJA}	-	-	62	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction-ambient for SMD version	R_{thJA}	-	35	45	°C/W	Device on 40mm*40mm* 1.5mm epoxy PCB FR4 with 6cm ² (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL1

3 Electrical characteristics

at $T_j = 25\text{ °C}$, unless specified otherwise

Table 5 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 0.7	1.2 1.0	1.6 1.4	V	$I_{DS} = 4.19\text{ mA}; V_{DS} = 10\text{ V}; T_j = 25\text{ °C}$ $I_{DS} = 4.19\text{ mA}; V_{DS} = 10\text{ V}; T_j = 125\text{ °C}$
Gate-Source reverse clamping voltage	$V_{GS, clamp}$	-	-	-8	V	$I_{GSS} = -1\text{ mA}$
Drain-Source leakage current	I_{DSS}	-	1.6 32	160 -	μA	$V_{DS} = 600\text{ V}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C}$ $V_{DS} = 600\text{ V}; V_{GS} = 0\text{ V}; T_j = 150\text{ °C}$
Drain-Source leakage current at application conditions ¹	I_{DSSapp}	-	96	-	μA	$V_{DS} = 400\text{ V}; V_{GS} = 0\text{ V}; T_j = 125\text{ °C}$
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.033 0.064	0.042 -	Ω	$I_G = 83.8\text{ mA}; I_D = 12\text{ A}; T_j = 25\text{ °C}$ $I_G = 83.8\text{ mA}; I_D = 12\text{ A}; T_j = 150\text{ °C}$
Gate resistance	$R_{G,int}$	-	0.51	-	Ω	LCR impedance measurement; $f = f_{res}$; open drain; $T_j = 25\text{ °C}$

Table 6 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	649	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V};$ $f = 1\text{ MHz}$
Output capacitance	C_{oss}	-	97	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V};$ $f = 1\text{ MHz}$
Reverse Transfer capacitance	C_{rss}	-	1.35	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 400\text{ V};$ $f = 1\text{ MHz}$
Effective output capacitance, energy related ²	$C_{o(er)}$	-	115	-	pF	$V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ³	$C_{o(tr)}$	-	155	-	pF	$V_{GS} = 0\text{ V}; V_{DS} = 0\text{ to }400\text{ V};$ $I_D = \text{const}$
Output charge	Q_{oss}	-	62	-	nC	$V_{DS} = 0\text{ to }400\text{ V}$
Turn- on delay time	$t_{d(on)}$	-	13	-	ns	see Figure 23
Turn- off delay time	$t_{d(off)}$	-	19	-	ns	see Figure 23
Rise time	t_r	-	8	-	ns	see Figure 23
Fall time	t_f	-	11	-	ns	see Figure 23

¹ Parameter represents end of use leakage in applications

² $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

³ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 7 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	8.8	-	nC	$I_{GS} = 0$ to 16 mA; $V_{DS} = 400$ V; $I_D = 12$ A

Table 8 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2	2.5	V	$V_{GS} = 0$ V; $I_{SD} = 12$ A
Pulsed current, reverse	$I_{S,pulse}$	-	-	90	A	$I_G = 83.8$ mA
Reverse recovery charge	Q_{rr}^1	-	0	-	nC	$I_S = 12$ A, $V_{DS} = 400$ V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

¹ Excluding Q_{oss}
Final Data Sheet

4 Electrical characteristics diagrams

at $T_j = 25\text{ }^\circ\text{C}$, unless specified otherwise

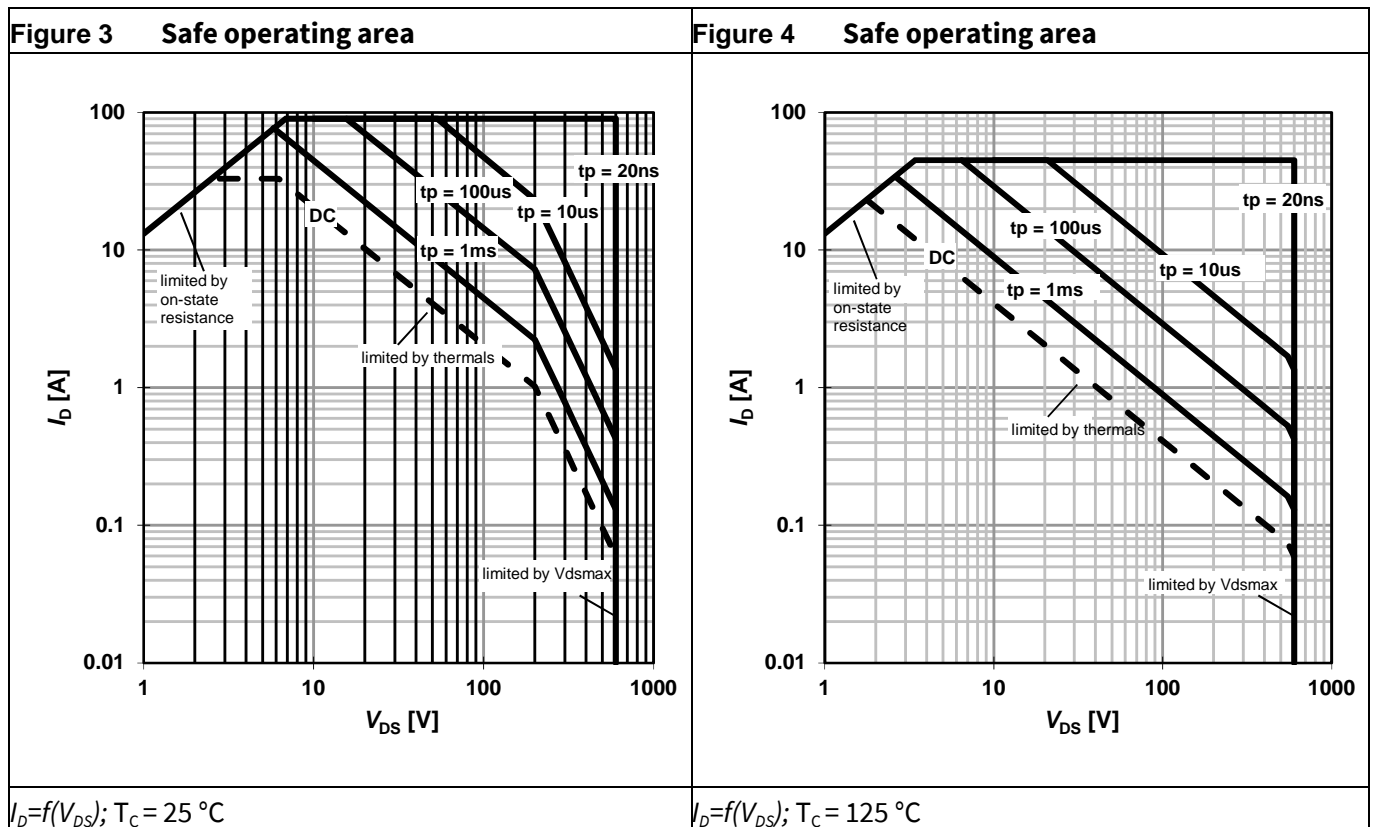
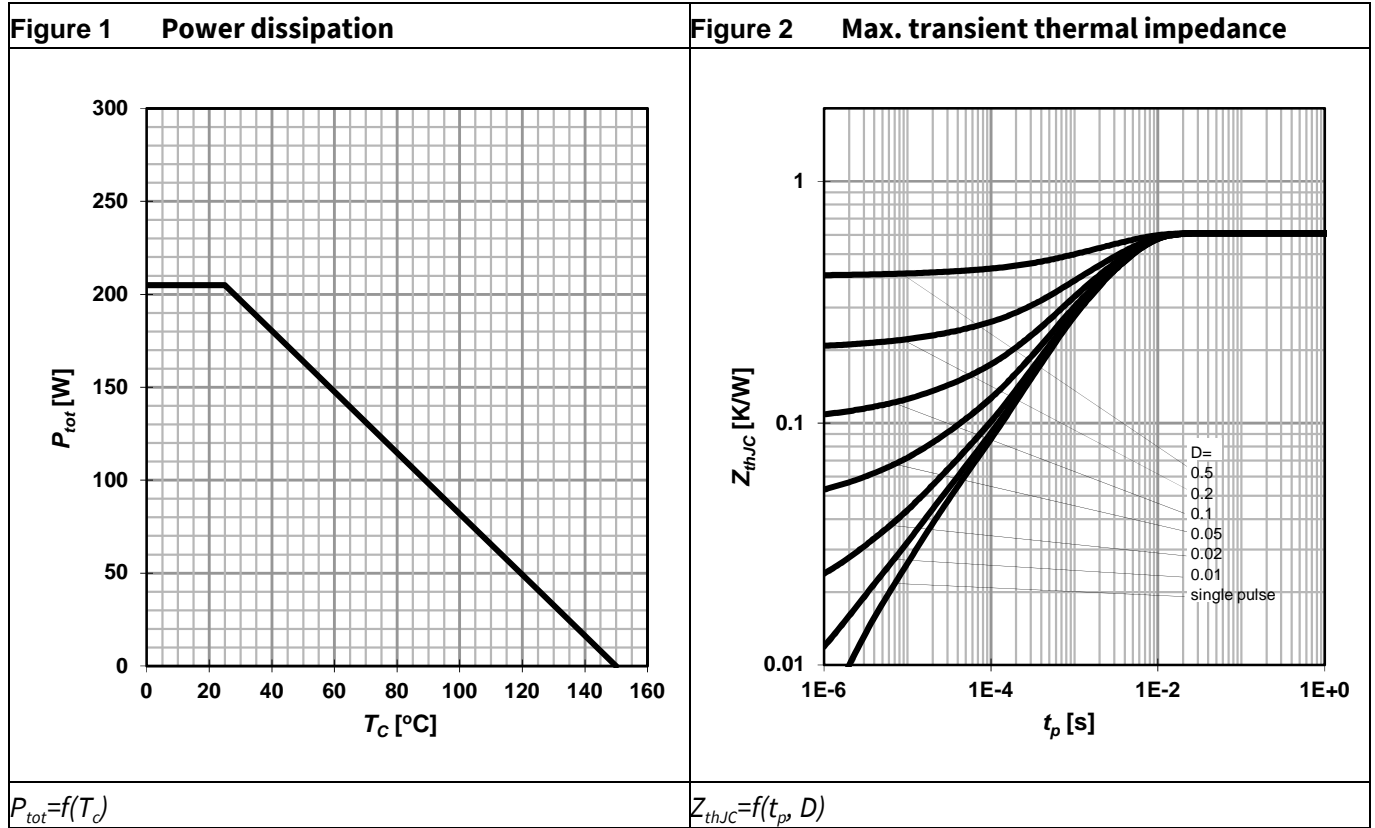
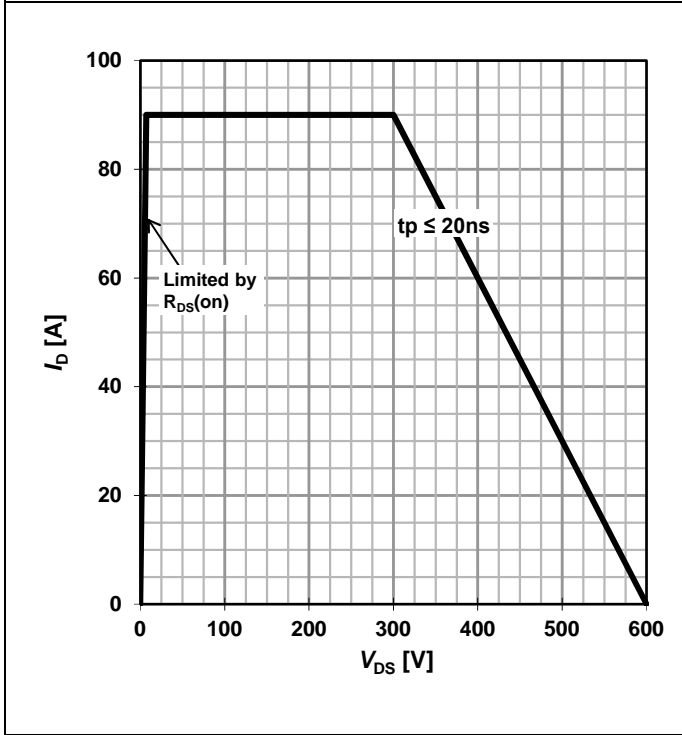
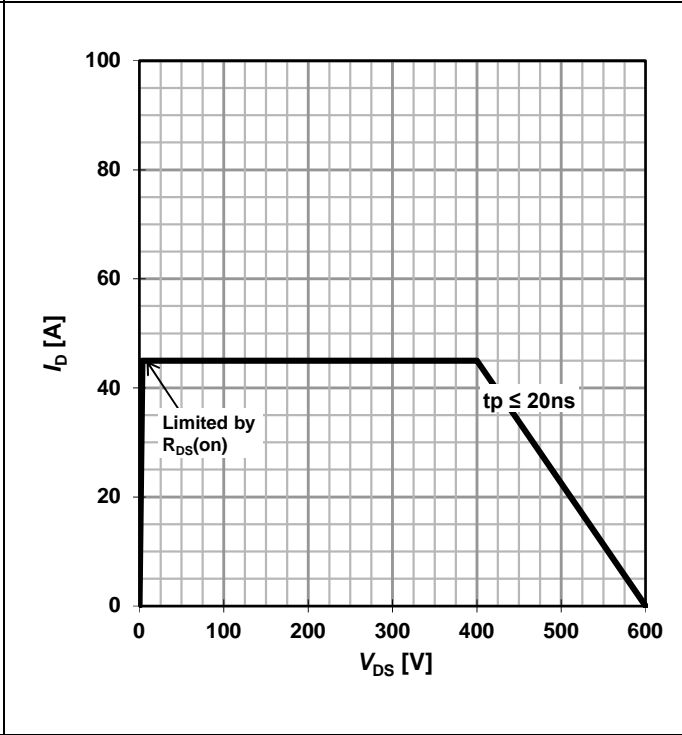


Figure 5 Repetitive safe operating area¹



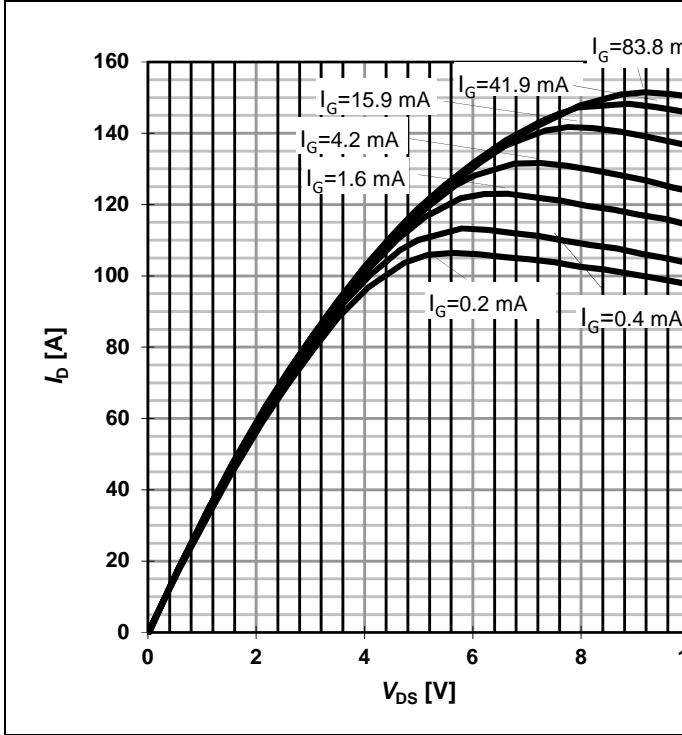
$T_c = 25\text{ °C}; T_j \leq 150\text{ °C}$

Figure 6 Repetitive safe operating area¹



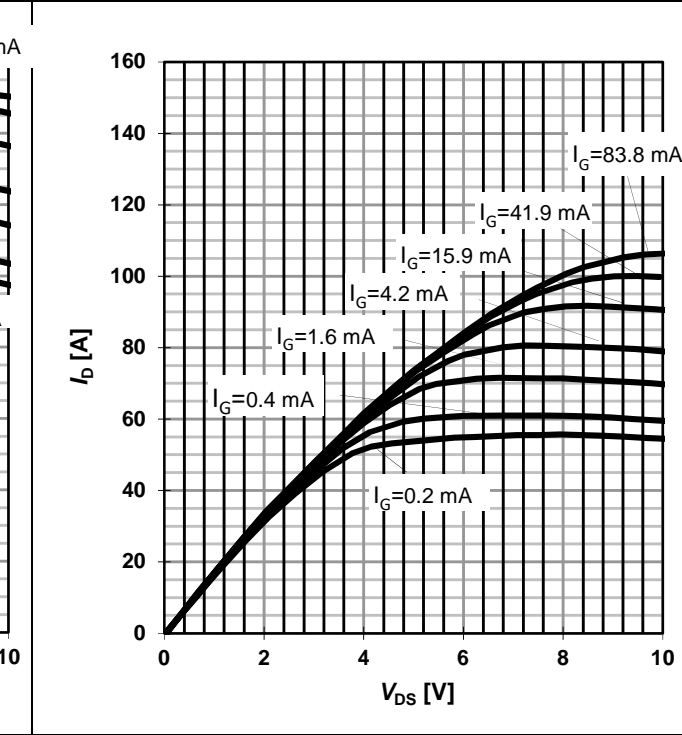
$T_c = 125\text{ °C}; T_j \leq 150\text{ °C}$

Figure 7 Typ. output characteristics



$I_D = f(V_{DS}, I_G); T_j = 25\text{ °C}$

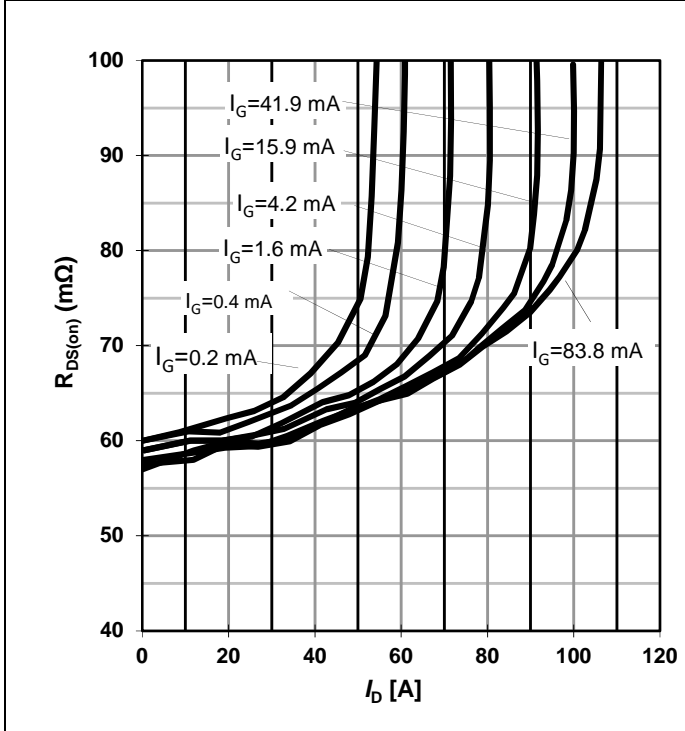
Figure 8 Typ. output characteristics



$I_D = f(V_{DS}, I_G); T_j = 125\text{ °C}$

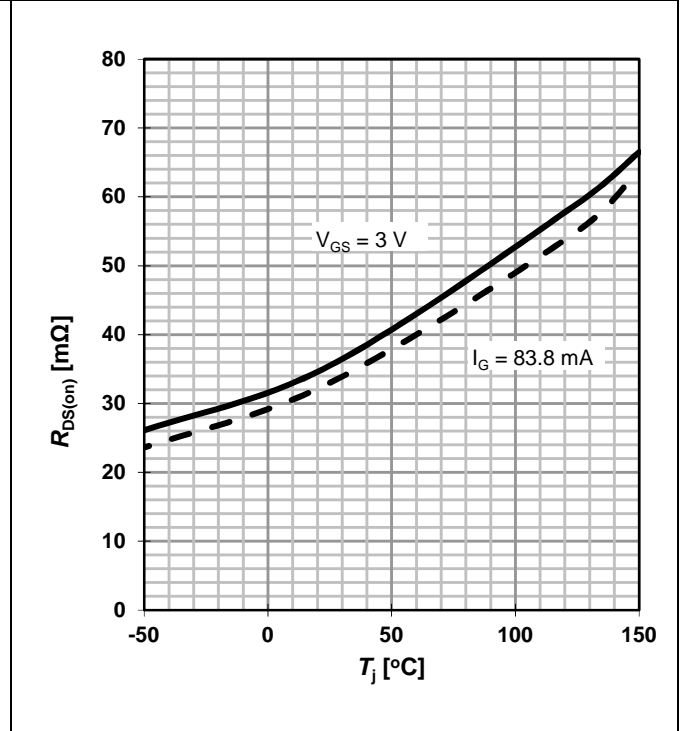
¹ Parameter is influenced by rel-requirements. Please contact the local Infineon Sales Office to get an assessment of your application.

Figure 9 Typ. Drain-source on-state resistance



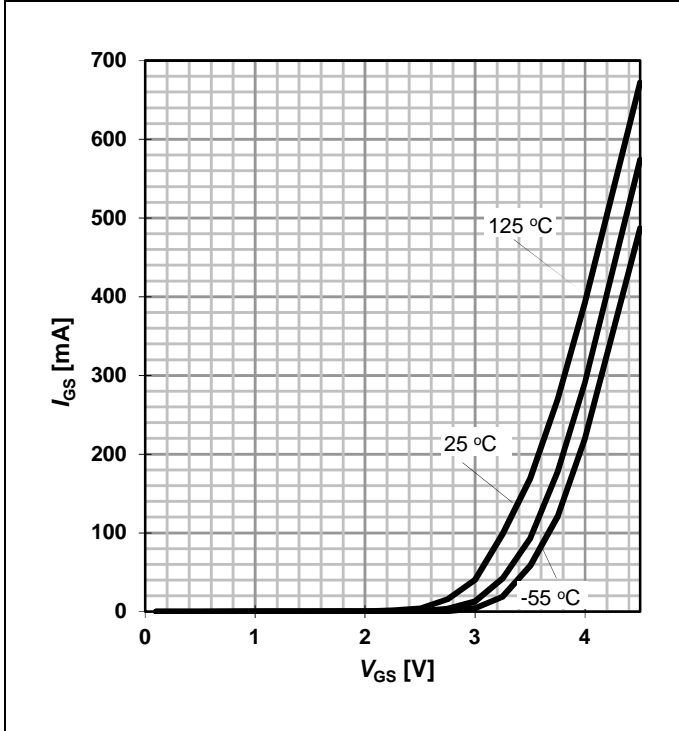
$R_{DS(on)} = f(I_D, I_G); T_j = 125^\circ\text{C}$

Figure 10 Drain-source on-state resistance



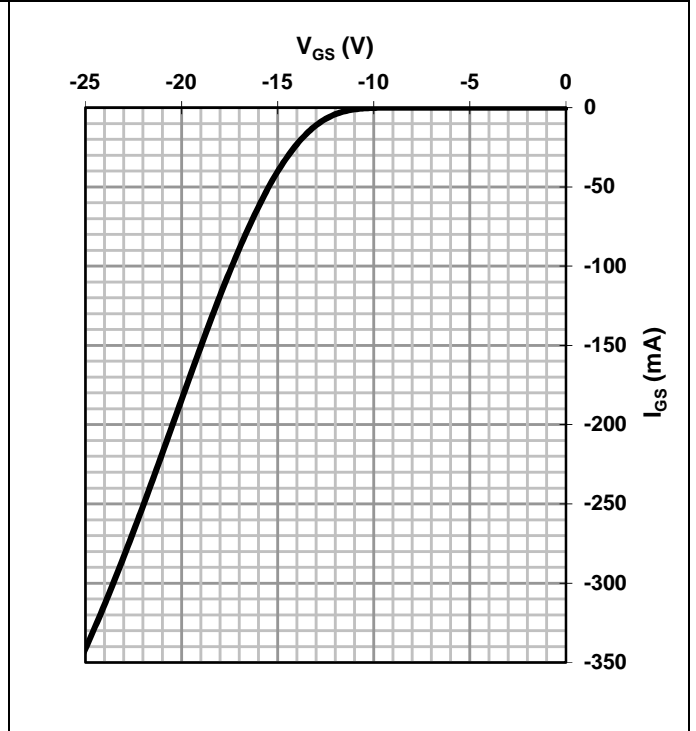
$R_{DS(on)} = f(T_j); I_D = 12$ A

Figure 11 Typ. gate characteristics forward



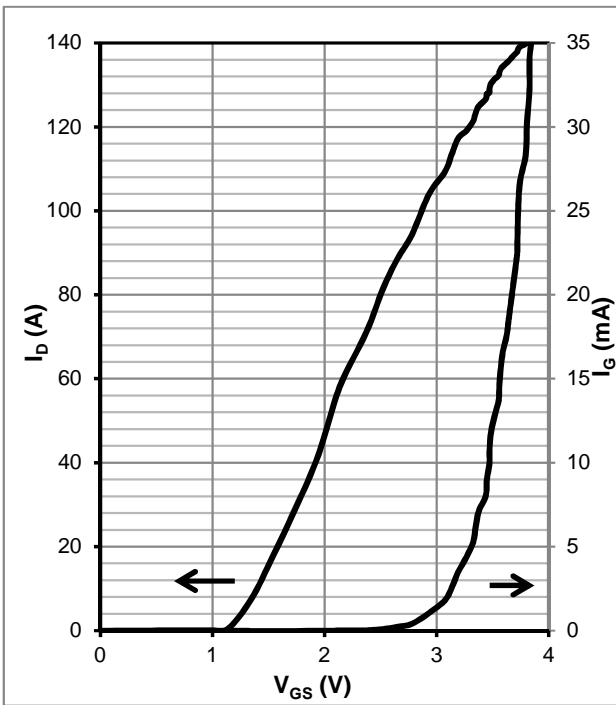
$I_{GS} = f(V_{GS}, T_j);$ open drain

Figure 12 Typ. gate characteristics reverse



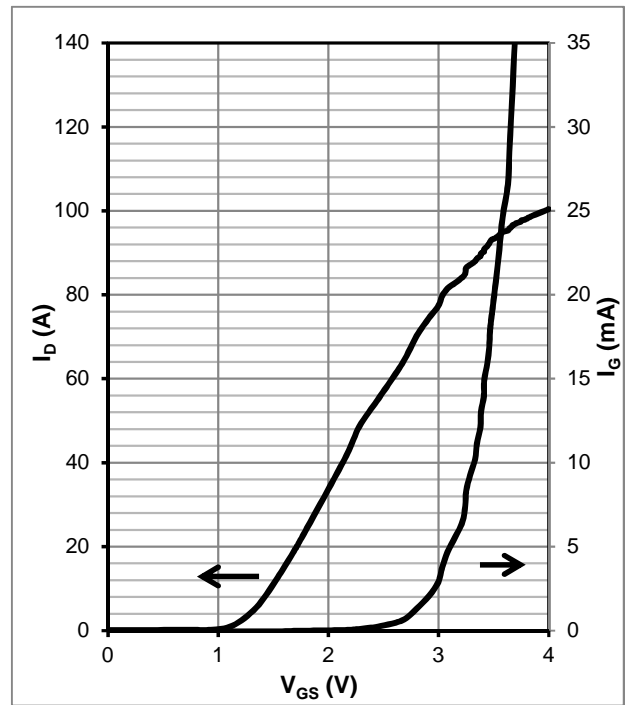
$I_{GS} = f(V_{GS}); T_j = 25^\circ\text{C}$

Figure 13 Typ. transfer characteristics



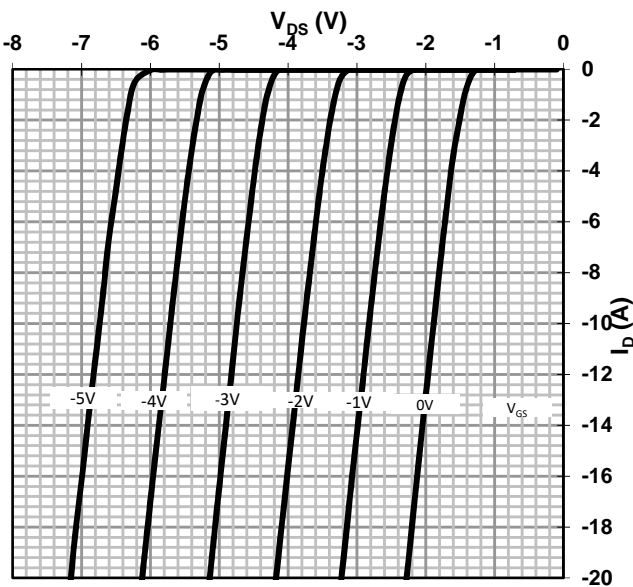
$I_D, I_G = f(V_{GS}); V_{DS} = 8 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

Figure 14 Typ. transfer characteristics



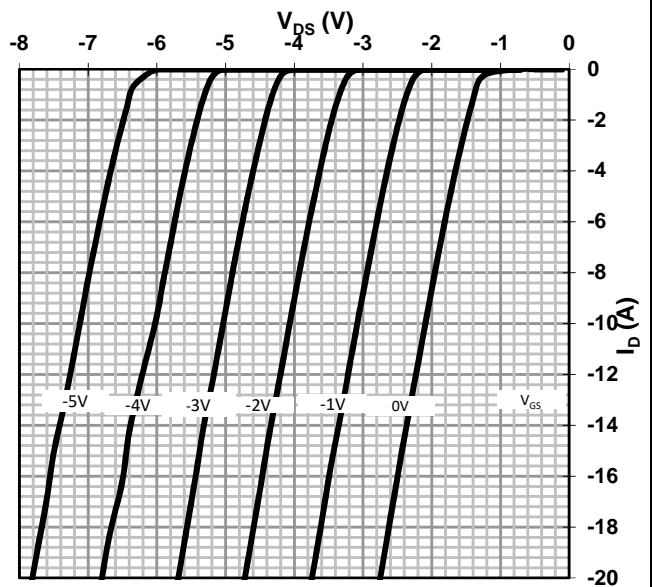
$I_D, I_G = f(V_{GS}); V_{DS} = 8 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$

Figure 15 Typ. channel reverse characteristics



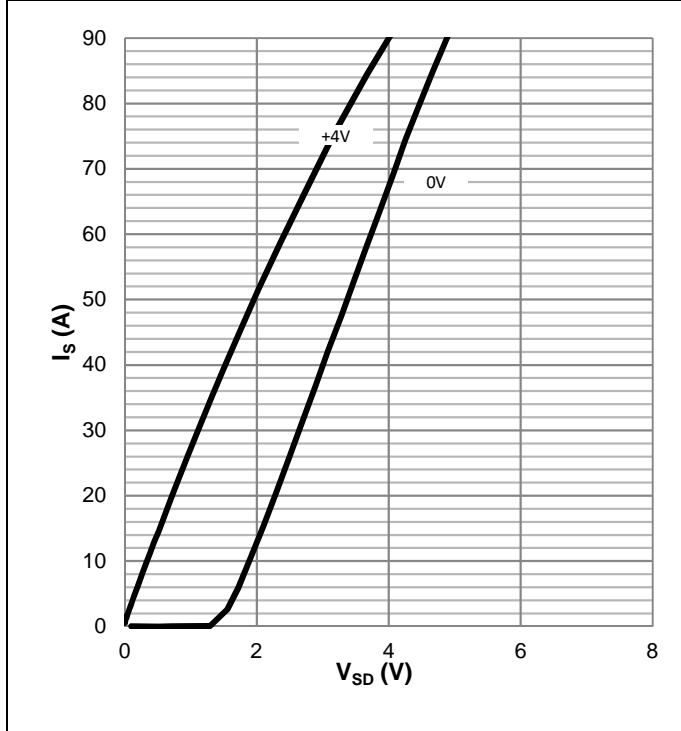
$V_{DS} = f(I_D, V_{GS}); T_j = 25 \text{ }^\circ\text{C}$

Figure 16 Typ. channel reverse characteristics



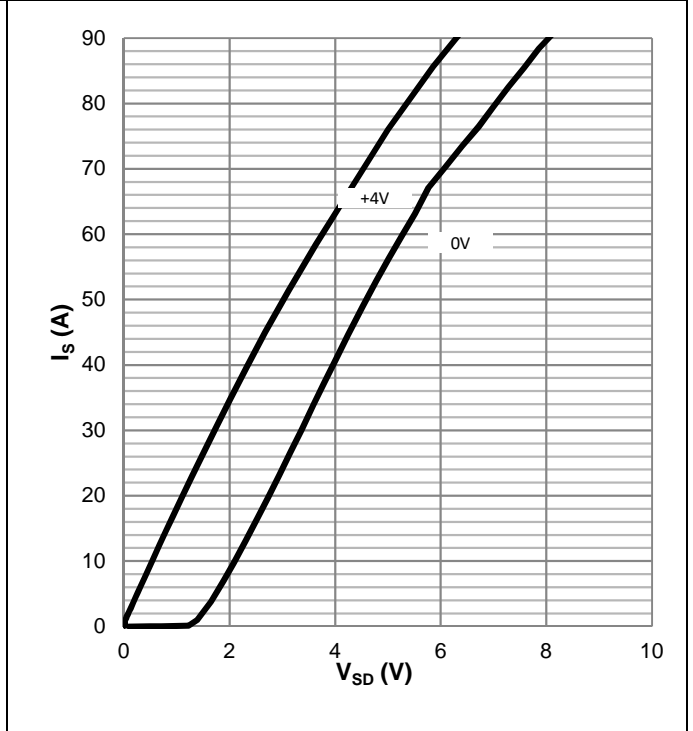
$V_{DS} = f(I_D, V_{GS}); T_j = 125 \text{ }^\circ\text{C}$

Figure 17 Typ. channel reverse characteristics



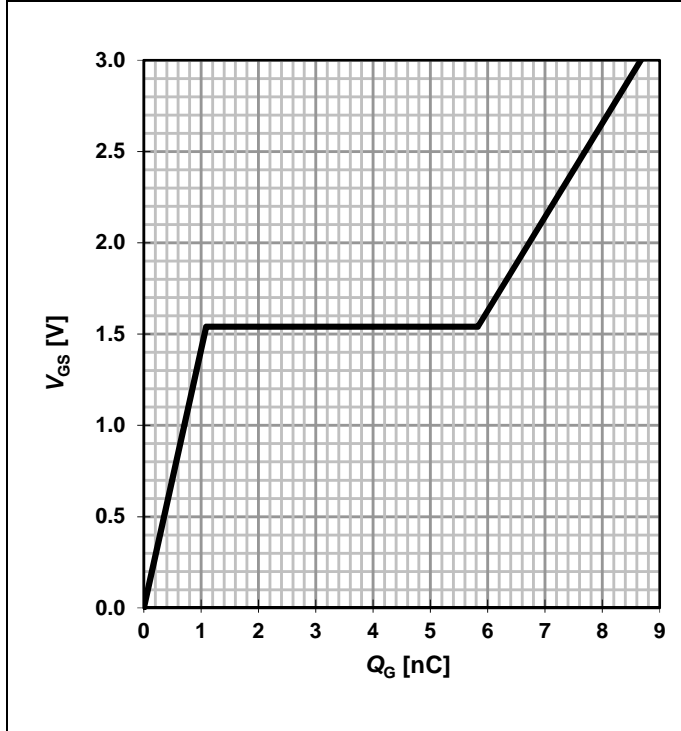
$I_D = f(V_{DS}, V_{GS}); T_j = 25\text{ °C}$

Figure 18 Typ. channel reverse characteristics



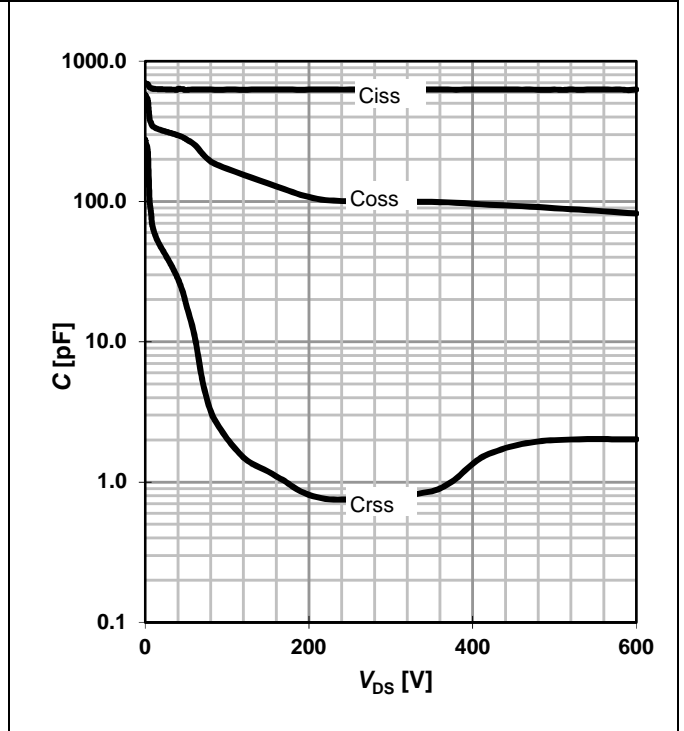
$I_D = f(V_{DS}, V_{GS}); T_j = 125\text{ °C}$

Figure 19 Typ. gate charge

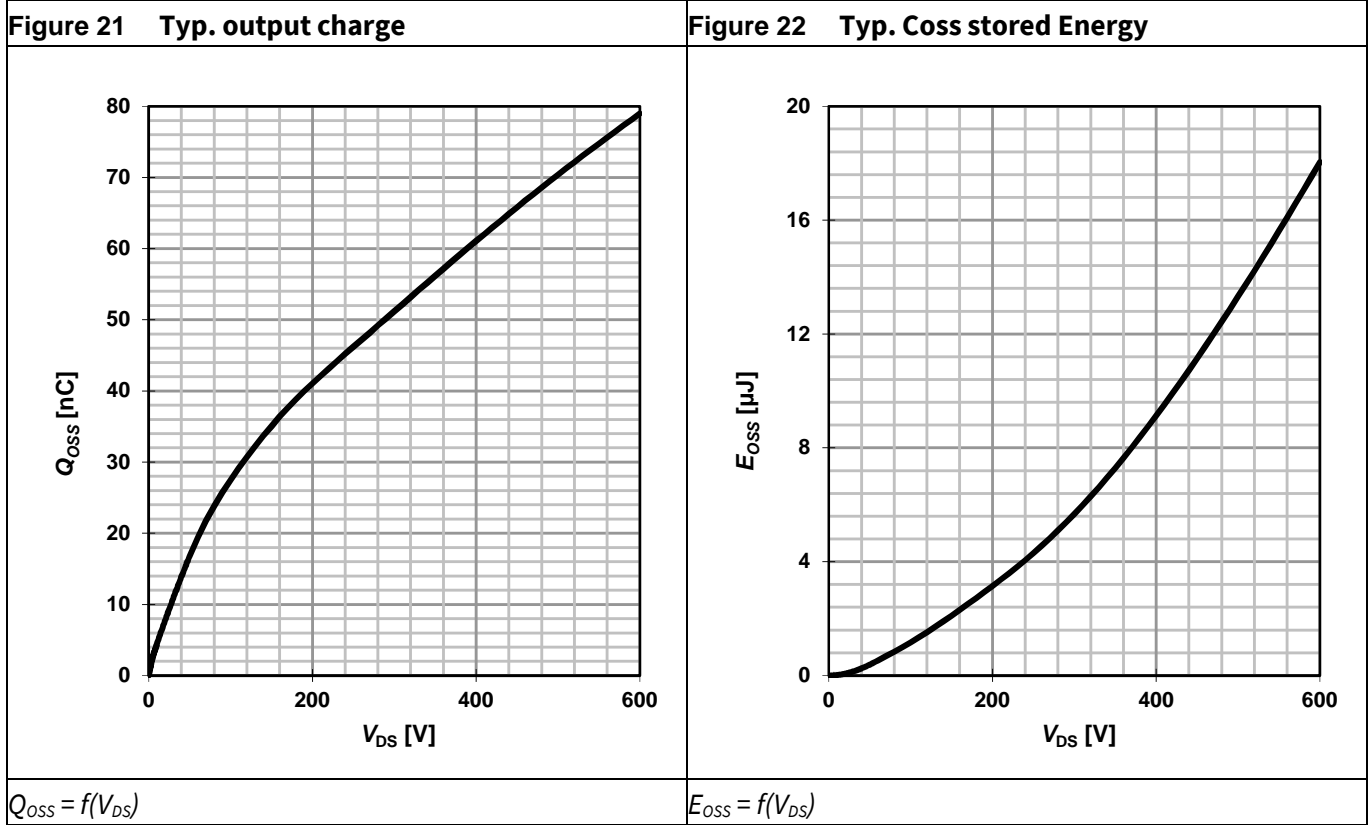


$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 12\text{ A}$

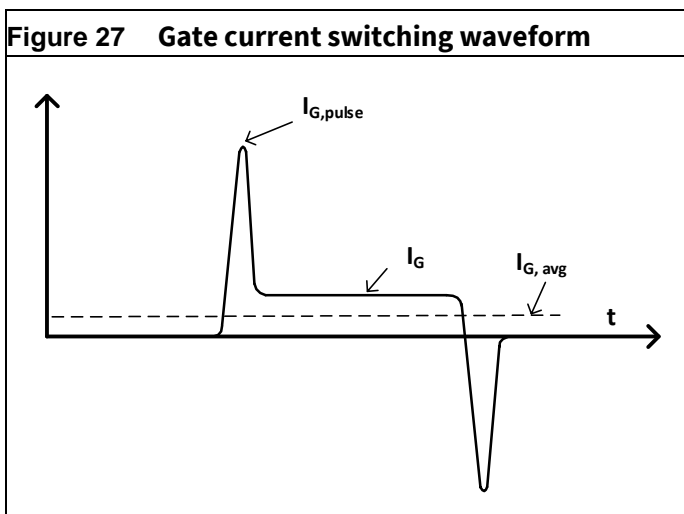
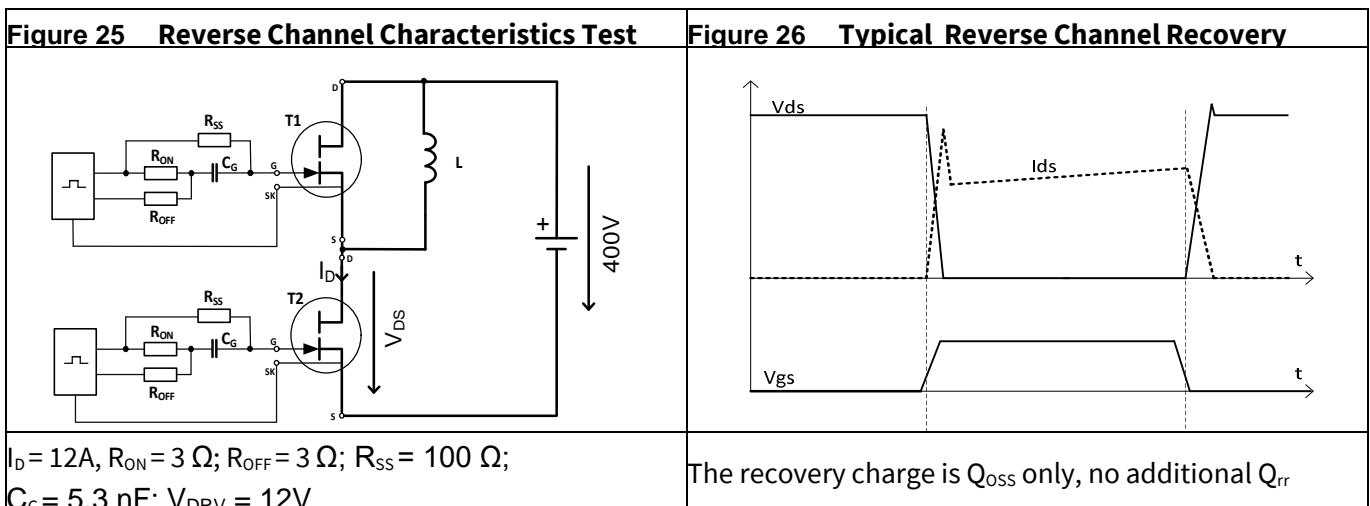
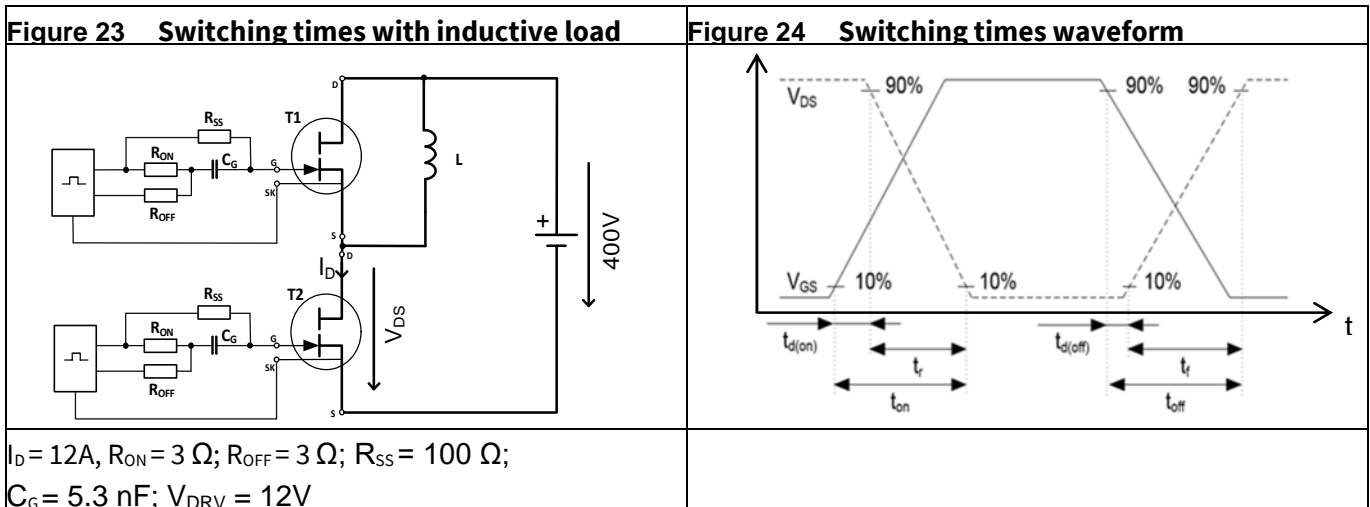
Figure 20 Typ. capacitances



$C_{XSS} = f(V_{DS})$



5 Test Circuits



6 Package Outlines

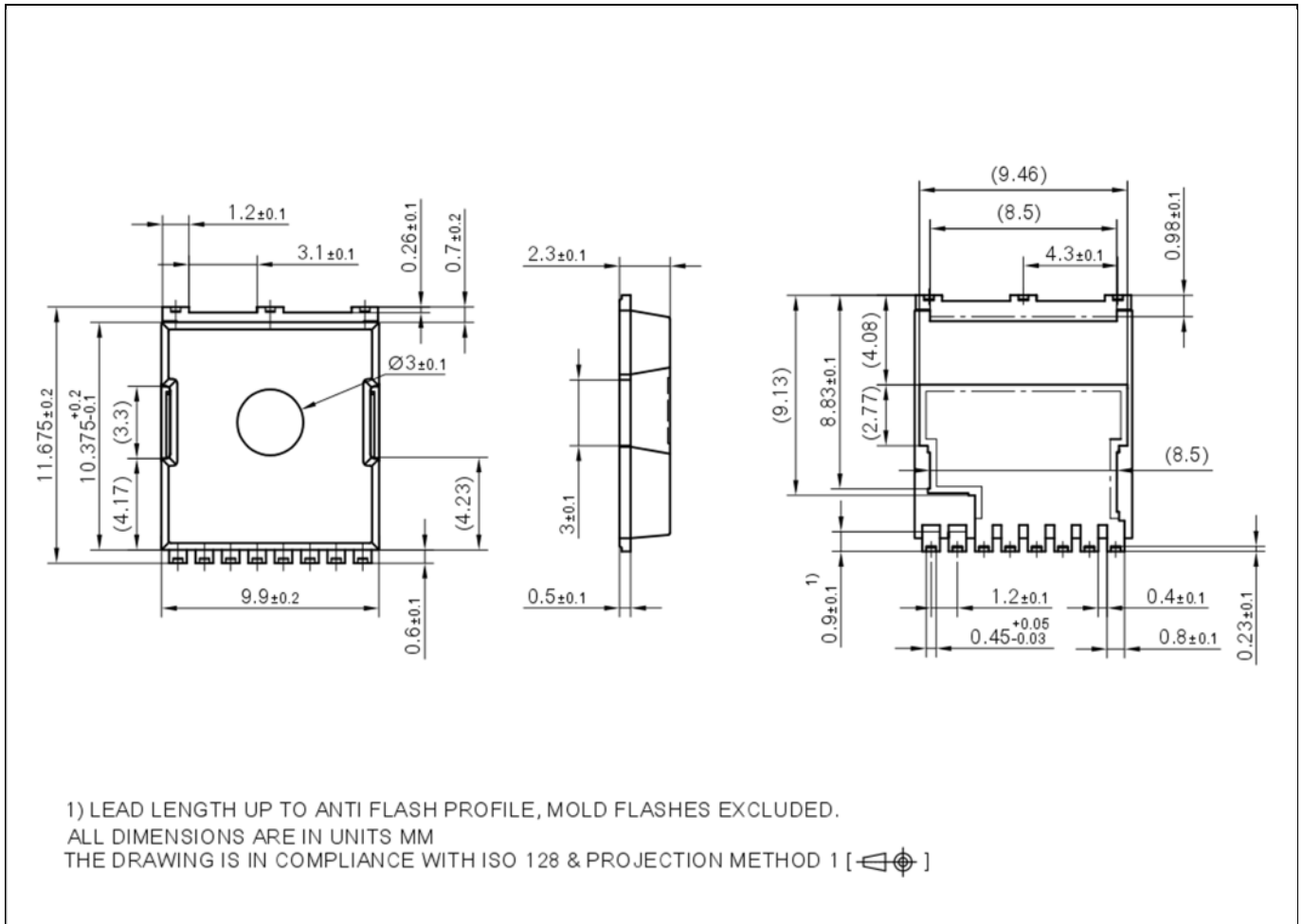


Figure 28 PG-HSOF-8-3 Package Outline, dimensions (mm)

7 Appendix A

Table 9 Related links

- IFX CoolGaN™ webpage: www.infineon.com/why-coolgan
- IFX CoolGaN™ reliability white paper: www.infineon.com/gan-reliability
- IFX CoolGaN™ gate drive application note: www.infineon.com/driving-coolgan
- IFX CoolGaN™ applications information:
 - www.infineon.com/gan-in-server-telecom
 - www.infineon.com/gan-in-wirelesscharging
 - www.infineon.com/gan-in-audio
 - www.infineon.com/gan-in-adapter-charger

8 Revision History

Major changes since the last revision

Revision	Date	Description of change
2.0	2023-02-22	Final release

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