

# BGS15MA12

SP5T Rx Diversity Switch

## Data Sheet

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Power Management & Multimarket

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| 20   | Carrier Tape drawing updated (Fig. 12)       |
|      |  |

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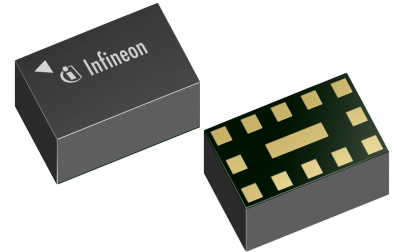
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## BGS15MA12 SP5T Rx Diversity Switch

### 1 Features

- Low insertion loss
- Low harmonic generation
- High port-to-port-isolation
- Suitable for LTE / WCDMA Rx Applications
- 0.1 to 2.9 GHz coverage
- No decoupling capacitors required if no DC applied on RF lines
- On chip control logic including ESD protection
- Integrated MIPI RFFE interface operating in 1.1 to 1.95 V voltage range
- Software programmable MIPI RFFE USID
- Direct to battery supply
- Small form factor 1.1 mm x 1.9 mm
- No power supply blocking required
- High EMI robustness
- RoHS and WEEE compliant package



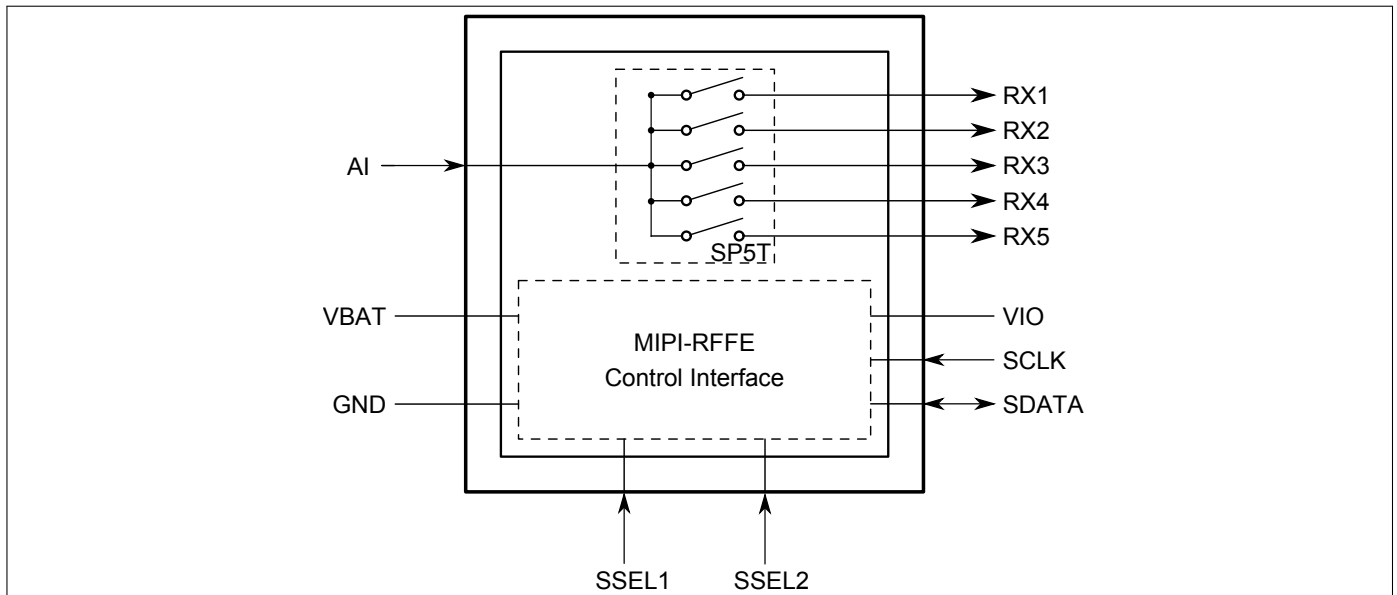
### 2 Product Description

The BGS15MA12 RF MOS switch is specifically designed for LTE and WCDMA diversity applications. This SP5T offers low insertion loss and low harmonic generation in termination mode.

The switch is controlled via a MIPI RFFE controller. The on-chip controller allows power-supply voltages from 1.1 to 1.95 V. The switch features direct-connect-to-battery functionality and DC-free RF ports. Unlike GaAs technology, external DC blocking capacitors at the RF Ports are only required if DC voltage is applied externally. The BGS15MA12 RF Switch is manufactured in Infineon's patented MOS technology, offering the performance of GaAs with the economy and integration of conventional CMOS including the inherent higher ESD robustness. The device has a very small size of only 1.1 x 1.9 mm<sup>2</sup> and a maximum height of 0.65 mm.

**Table 1: Ordering Information**

| Type      | Package    | Marking | Chip  |
|-----------|------------|---------|-------|
| BGS15MA12 | ATSLP-12-4 | S4      | m4829 |


**Figure 1:** BGS15MA12 Block diagram

### 3 Maximum Ratings

**Table 2: Maximum Ratings, Table I** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

| Parameter                         | Symbol         | Values |      |      | Unit             | Note / Test Condition      |
|-----------------------------------|----------------|--------|------|------|------------------|----------------------------|
|                                   |                | Min.   | Typ. | Max. |                  |                            |
| Frequency Range                   | f              | 0.1    | –    | –    | GHz              | <sup>1)</sup>              |
| Supply voltage                    | $V_{BAT}$      | -0.5   | –    | 6.0  | V                | –                          |
| Storage temperature range         | $T_{STG}$      | -55    | –    | 150  | $^\circ\text{C}$ | –                          |
| Junction temperature              | $T_j$          | –      | –    | 125  | $^\circ\text{C}$ | –                          |
| RF input power at all RX ports    | $P_{RF\_RX}$   | –      | –    | 27   | dBm              | CW                         |
| ESD capability, CDM <sup>2)</sup> | $V_{ESD\_CDM}$ | -1     | –    | +1   | V                | All pins                   |
| ESD capability, HBM <sup>3)</sup> | $V_{ESD\_HBM}$ | -1     | –    | +1   | kV               | Digital, digital versus RF |
|                                   |                | -1     | –    | +1   | kV               | RF                         |

<sup>1)</sup>There is also a DC connection between switched paths. The DC voltage at RF ports  $V_{RFDC}$  has to be 0V.

<sup>2)</sup>Field-Induced Charged-Device Model JESD22-C101. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

<sup>3)</sup>Human Body Model ANSI/ESDA/JEDEC JS-001-2012 (R=1.5 k $\Omega$ , C=100 pF).

<sup>4)</sup>IEC 61000-4-2 (R=330  $\Omega$ , C=150 pF), contact discharge.

**Table 3: Maximum Ratings, Table II** at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified

| Parameter   | Symbol     | Values |      |                          | Unit | Note / Test Condition              |
|---|------------|--------|------|--------------------------|------|------------------------------------|
|   |            | Min.   | Typ. | Max.                     |      |                                    |
| Maximum DC-voltage on RF-Ports and RF-Ground              | $V_{RFDC}$ | 0      | –    | 0                        | V    | No DC voltages allowed on RF-Ports |
| RF FE Supply Voltage                                      | $V_{IO}$   | -0.5   | –    | 3                        | V    | –                                  |
| RF FE Control Voltage Levels at SCLK, SDATA, SSEL1, SSEL2 | V          | -0.7   | –    | $V_{IO}+0.7$<br>(max. 3) | V    | –                                  |

## 4 Operation Ranges

**Table 4: Operation Ranges**

| Parameter                                    | Symbol        | Values             |      |                    | Unit        | Note / Test Condition                |
|--|---------------|--------------------|------|--------------------|-------------|--------------------------------------|
|  |               | Min.               | Typ. | Max.               |             |                                      |
| Supply voltage                               | $V_{BAT}$     | 2.2                | –    | 5.5                | V           | –                                    |
| Supply current <sup>3)</sup>                 | $I_{BAT}$     | –                  | 80   | 200                | $\mu A$     | –                                    |
| Supply current in standby mode <sup>3)</sup> | $I_{BAT\_SB}$ | –                  | 0.5  | 1                  | $\mu A$     | $V_{IO}$ =low or MIPI low-power mode |
| RFFE supply voltage                          | $V_{IO}$      | 1.1                | 1.8  | 1.95               | V           | –                                    |
| RFFE input high voltage <sup>1)</sup>        | $V_{IH}$      | $0.7 \cdot V_{IO}$ | –    | $V_{IO}$           | V           | –                                    |
| RFFE input low voltage <sup>1)</sup>         | $V_{IL}$      | 0                  | –    | $0.3 \cdot V_{IO}$ | V           | –                                    |
| RFFE output high voltage <sup>2)</sup>       | $V_{OH}$      | $0.8 \cdot V_{IO}$ | –    | $V_{IO}$           | V           | –                                    |
| RFFE output low voltage <sup>2)</sup>        | $V_{OL}$      | 0                  | –    | $0.2 \cdot V_{IO}$ | V           | –                                    |
| RFFE control input capacitance               | $C_{Ctrl}$    | –                  | –    | 2                  | pF          | –                                    |
| RFFE supply current                          | $I_{VIO}$     | –                  | 15   | –                  | $\mu A$     | Idle State                           |
| Ambient temperature                          | $T_A$         | -30                | 25   | 85                 | $^{\circ}C$ | –                                    |

<sup>1)</sup>SCLK, SDATA, SSEL1 and SSEL2

<sup>2)</sup>SDATA

<sup>3)</sup> $T_A = -30^{\circ}C - 85^{\circ}C$ ,  $V_{BAT} = 2.2 - 5.5 V$ 
**Table 5: RF Input Power**

| Parameter               | Symbol       | Values |      |      | Unit | Note / Test Condition |
|-------------------------|--------------|--------|------|------|------|-----------------------|
|                         |              | Min.   | Typ. | Max. |      |                       |
| RX ports (50 $\Omega$ ) | $P_{RF\_RX}$ | –      | –    | 24   | dBm  | –                     |



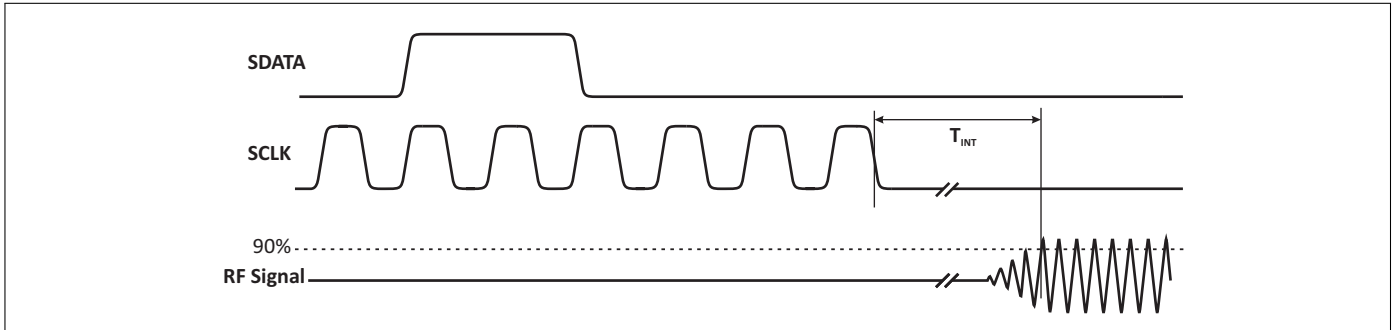
## 5 RF Characteristics

**Table 6: RF Characteristics** at  $T_A = -30\text{ }^{\circ}\text{C} - 85\text{ }^{\circ}\text{C}$ ,  $P_{IN} = 0\text{ dBm}$ , Supply Voltage  $V_{BAT} = 2.2\text{ V} - 5.5\text{ V}$ , unless otherwise specified

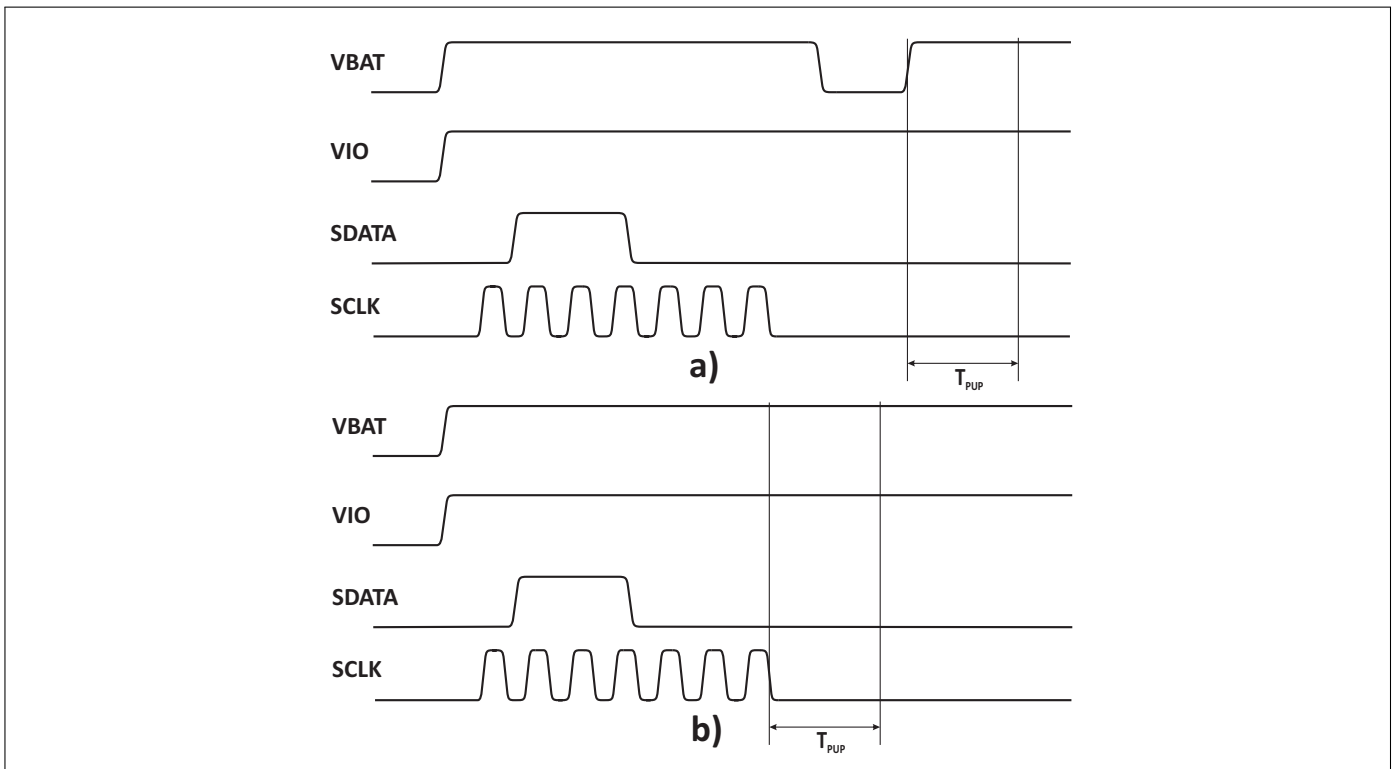
| Parameter   | Symbol        | Values |      |      | Unit          | Note / Test Condition                             |
|---|---------------|--------|------|------|---------------|---|
|   |               | Min.   | Typ. | Max. |               |   |
| <b>Insertion Loss<sup>1)</sup></b>  |               |        |      |      |               |   |
| All RX Ports  | IL            | 0.2    | 0.28 | 0.35 | dB            | 700–1000 MHz                                      |
|   |               | 0.25   | 0.35 | 0.5  | dB            | 1700–2200 MHz                                     |
|   |               | 0.3    | 0.42 | 0.6  | dB            | 2300–2700 MHz                                     |
| <b>Return Loss<sup>1)</sup></b>   |               |        |      |      |               |   |
| All RX Ports  | RL            | 20     | 30   | –    | dB            | 700–1000 MHz                                      |
|   |               | 18     | 28   | –    | dB            | 1700–2200 MHz                                     |
|   |               | 12     | 22   | –    | dB            | 2300–2700 MHz                                     |
| Isolation all RX Ports  | ISO           | 24     | 34   | –    | dB            | 700–1000 MHz                                      |
|   |               | 17     | 27   | –    | dB            | 1700–2200 MHz                                     |
|   |               | 15     | 25   | –    | dB            | 2300–2700 MHz                                     |
| Isolation RX Ports to AI  | ISO           | 26     | 36   | –    | dB            | 700–1000 MHz                                      |
|   |               | 21     | 31   | –    | dB            | 1700–2200 MHz                                     |
|   |               | 18     | 28   | –    | dB            | 2300–2700 MHz                                     |
| <b>P1 dB Compression Point, Extrapolated</b>  |               |        |      |      |               |   |
| All RX Ports  | $P_{1dB}$     | >30    | –    | –    | dBm           |   |
| <b>Harmonic Generation up to 12.75 GHz</b>  |               |        |      |      |               |   |
| All RX Ports  | $P_{Harm}$    | –      | -95  | -75  | dBc           | 20 dBm, 50 $\Omega$ , CW mode                     |
| <b>Intermodulation Distortion in Rx Band<sup>2)</sup></b> ( $T_A = 25\text{ }^{\circ}\text{C}$ , $V_{BAT} = 2.6\text{ V}$ ) |               |        |      |      |               |   |
| IMD2, low   | $IMD2_{low}$  | –      | -115 | -105 | dBm           | Tx = 10 dBm,<br>Interferer = -15 dBm, 50 $\Omega$ |
| IMD3  | IMD3          | –      | -125 | -110 | dBm           |   |
| IMD2, high  | $IMD2_{high}$ | –      | -120 | -110 | dBm           |   |
| <b>Switching Time</b>   |               |        |      |      |               |   |
| RF Rise Time RX Port On/Off   | $t_{on/off}$  | 0.5    | 1    | 5    | $\mu\text{s}$ | 90% OFF to 90% ON;<br>90% ON to 90% OFF           |
| MIPI to RF Time   | $t_{INT}$     | 0.5    | 1.5  | 5    | $\mu\text{s}$ | 50% last SCLK falling flank to<br>90% ON, Fig. 2  |
| Power Up Settling Time  | $t_{PUS}$     | –      | 10   | 25   | $\mu\text{s}$ | After power down mode,<br>Fig. 3                  |

<sup>1)</sup>On application board with a RF low-Q two element matching network at the antenna port

<sup>2)</sup>On application board with shunt inductor, Min/Max-values measured with phase shifter.



**Figure 2:** MIPI to RF Time



**Figure 3:** Power-Up Settling Time Definition: **a)** when the device is already in Active Mode. **b)** when changing from Low Power Mode to Active Mode. After Power-Up of VIO the device is set to Low Power Mode. An additional MIPI instruction is necessary to set the switch to Active Mode. This case is covered by **b)**.

## 6 MIPI RFFE Specification

All sequences are implemented according to the 'MIPI Alliance Specification for RF Front-End Control Interface' document version 1.10 - 26. July 2011.

**Table 7: MIPI Features**

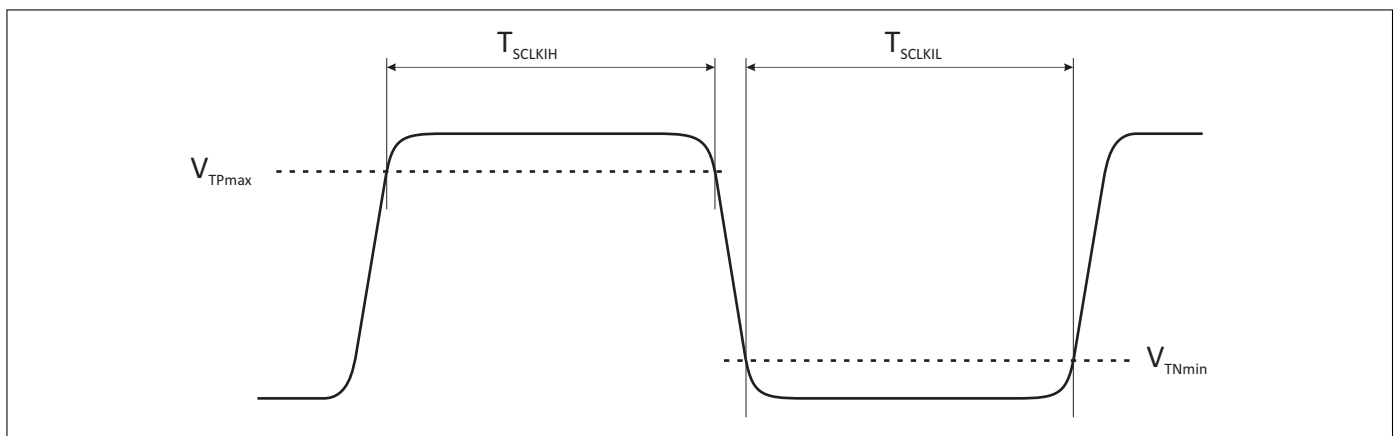
| Feature                                  | Supported | Comment   |
|--|-----------|---|
| Register write command sequence          | Yes       |   |
| Register read command sequence           | Yes       |   |
| Extended register write command sequence | No        | Up to 4 Bytes   |
| Extended register read command sequence  | No        | Up to 4 Bytes   |
| Register 0 write command sequence        | Yes       |   |
| Trigger function                         | Yes       | Trigger assignment to each control register is supported  |
| Programmable USID                        | Yes       | 3 register command sequence and extended register command sequence  |
| Status Register                          | Yes       | Register for debugging  |
| Reset                                    | Yes       | By VIO, Power Mode and RFFE_STATUS  |
| Group SID                                | Yes       |   |
| SSEL1 and SSEL2 pins                     | Yes       | External pins for changing USID:<br>SSEL1=0 & SSEL2=0 → 1000,<br>SSEL1=0 & SSEL2=1 → 1001,<br>SSEL1=1 & SSEL2=0 → 1010,<br>SSEL1=1 & SSEL2=1 → 1011 |
| Full speed write                         | Yes       |   |
| Half speed read                          | Yes       |   |
| Full speed read                          | Yes       |   |

**Table 8: Startup Behavior**

| Feature          | State     | Comment   |
|------------------|-----------|---|
| Power status     | LOW POWER | The chip is in low power mode after startup   |
| Trigger function | ENABLED   | Trigger function is enabled after startup. Trigger function can be disabled via PM_TRIG register. |

**Table 9: MIPI RFFE Operating Timing**

| Parameter            | Symbol    | Values |      |       | Unit    | Note / Test Condition  |
|----------------------|-----------|--------|------|-------|---------|------------------------|
|                      |           | Min.   | Typ. | Max.  |         |                        |
| SCLK Frequency       | FSCLK     | 0.032  | –    | 26    | MHz     | Full speed             |
|                      |           | 0.032  | –    | 13    | MHz     | Half speed             |
| SCLK Period          | TSCLK     | 0.038  | –    | 32    | $\mu$ s | Full speed             |
|                      |           | 0.077  | –    | 32    | $\mu$ s | Half speed             |
| SCLK Low Period      | TSCLKIL   | 11.25  | –    | –     | ns      | Full speed, see Fig. 4 |
|                      |           | 24     | –    | –     | ns      | Half speed, see Fig. 4 |
| SCLK High Period     | TSCLKIH   | 11.25  | –    | –     | ns      | Full speed, see Fig. 4 |
|                      |           | 24     | –    | –     | ns      | Half speed, see Fig. 4 |
| SDATA Setup Time     | TS        | 1      | –    | –     | ns      | Full speed, see Fig. 5 |
|                      |           | 2      | –    | –     | ns      | Half speed, see Fig. 5 |
| SDATA Hold Time      | TH        | 5      | –    | –     | ns      | Full speed, see Fig. 5 |
|                      |           | 5      | –    | –     | ns      | Half speed, see Fig. 5 |
| SDATA Release Time   | TSDATAZ   | –      | –    | 10    | ns      | Full speed, see Fig. 6 |
|                      |           | –      | –    | 18    | ns      | Half speed, see Fig. 6 |
| Time for Data Output | TD        | –      | –    | 10.25 | ns      | Full speed, see Fig. 7 |
|                      |           | –      | –    | 22    | ns      | Half speed, see Fig. 7 |
| SDATA Rise/Fall Time | TSDATAOTR | 2.1    | –    | 6.5   | ns      | Full speed, see Fig. 7 |
|                      |           | 2.1    | –    | 10    | ns      | Half speed, see Fig. 7 |
| VIO Rise Time        | TVIO-R    | 10     | –    | 450   | $\mu$ s | See Fig. 8             |
| VIO Reset Time       | TVIO-RST  | 10     | –    | –     | $\mu$ s | See Fig. 8             |
| Reset Delay Time     | TSIGOL    | 0.12   | –    | –     | $\mu$ s | See Fig. 8             |


**Figure 4: Received clock signal constraints**

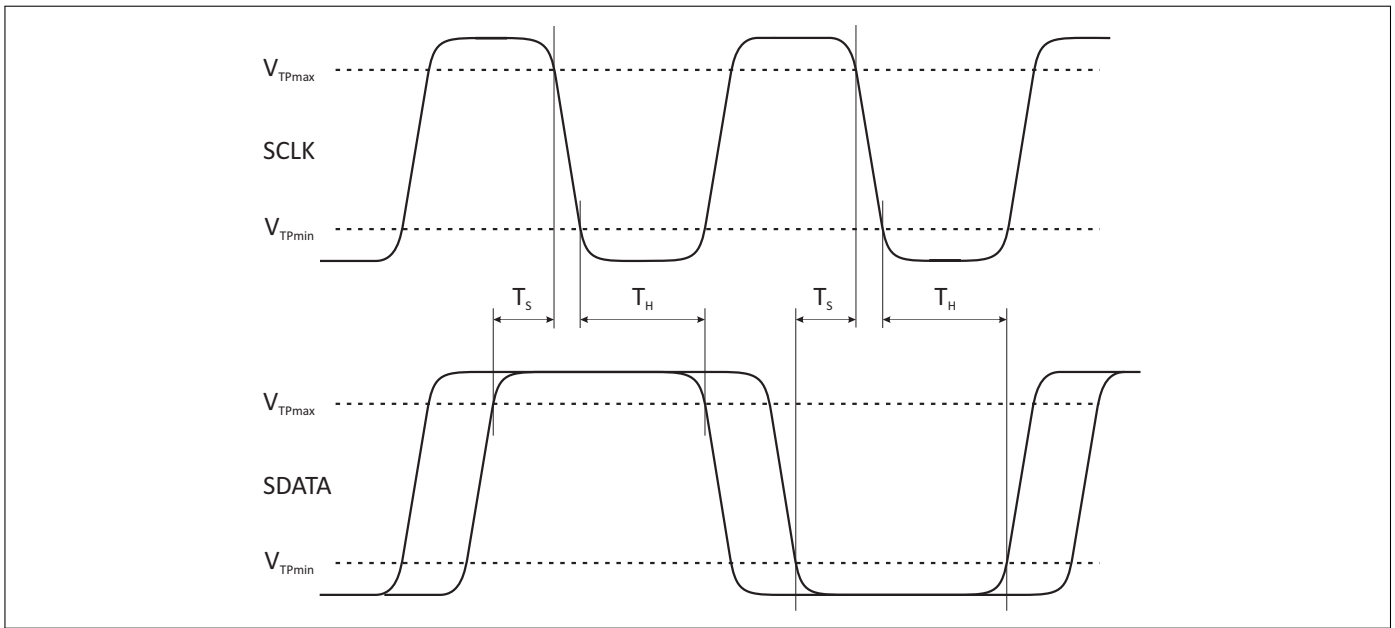


Figure 5: Bus active data receiver timing requirements

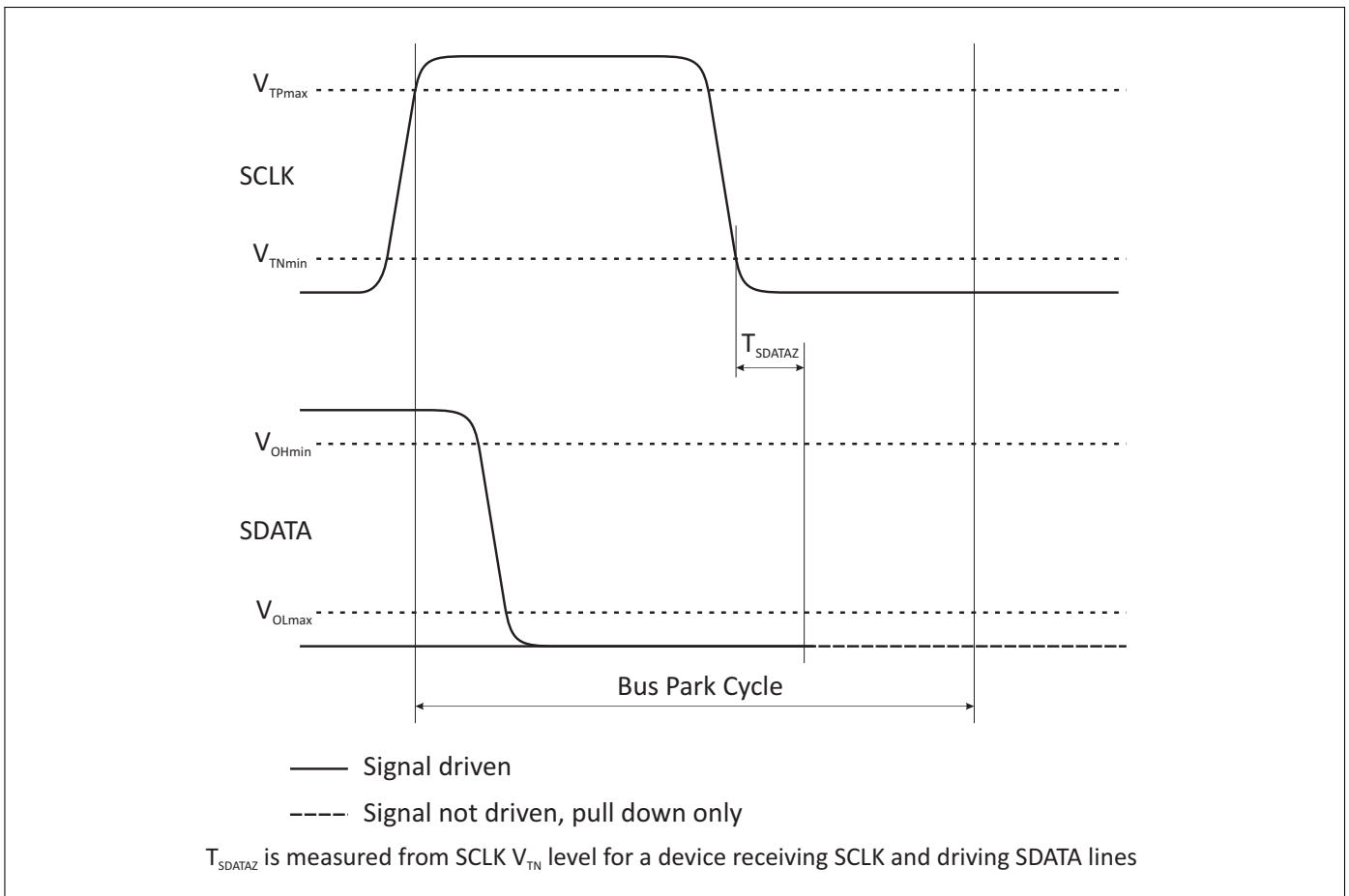
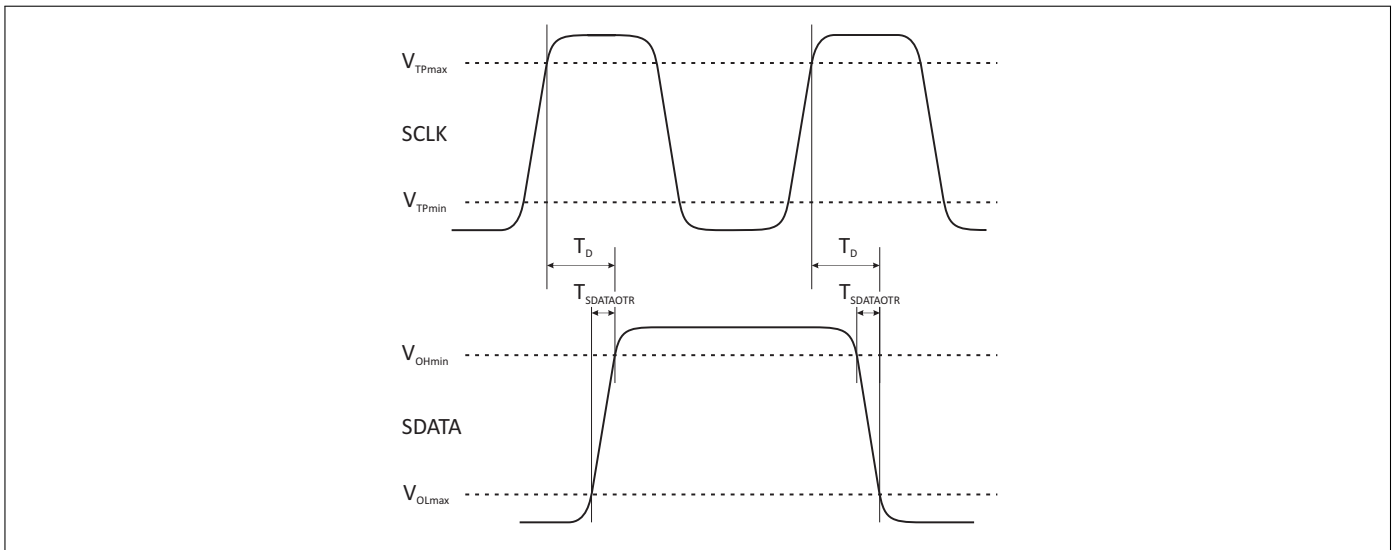
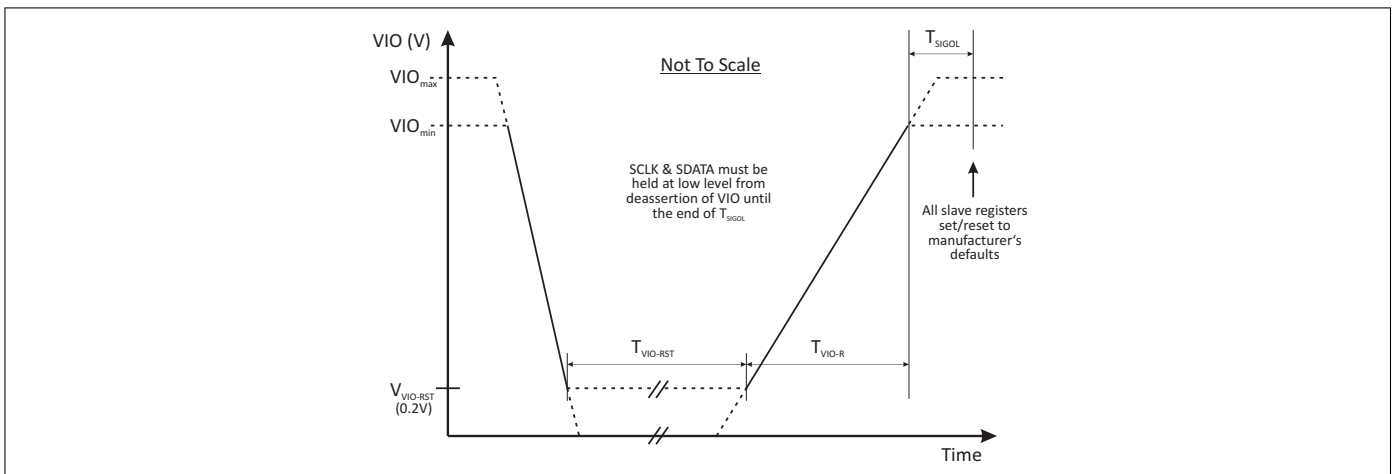


Figure 6: Bus park cycle timing



**Figure 7:** Bus active data transmission timing specification



**Figure 8:** Requirements for VIO-initiated reset

**Table 10: Register Mapping**

| Register Address | Register Name         | Data Bits | Function              | Description   | Default   | Broadcast_ID Support  | Trigger Support | R/W |     |
|------------------|-----------------------|-----------|-----------------------|---|---|---|-----------------|-----|-----|
| 0x0000           | REGISTER_0            | 7:0       | MODE_CTRL             | Switch control  | 00000000  | No  | Yes             | R/W |     |
| 0x001D           | PRODUCT_ID            | 7:0       | PRODUCT_ID            | This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.                  | 11010000  | No  | No              | R   |     |
| 0x001E           | MANUFACTURER_ID       | 7:0       | MANUFACTURER_ID [7:0] | This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value.                 | 00011010  | No  | No              | R   |     |
| 0x001C           | PM_TRIG               | 7:6       | PWR_MODE              | 00: Normal operation<br>01: Default settings (STARTUP)<br>10: Low power (LOW POWER)<br>11: Reserved   | 10  | Yes   | No              | R/W |     |
|                  |                       | 5         | TRIGGER_MASK_2        | If this bit is set, trigger 2 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 2, the data goes directly to the destination register.                | 0   | No  | No              |     |     |
|                  |                       | 4         | TRIGGER_MASK_1        | If this bit is set, trigger 1 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 1, the data goes directly to the destination register.                | 0   | No  | No              |     |     |
|                  |                       | 3         | TRIGGER_MASK_0        | If this bit is set, trigger 0 is disabled. When all triggers disabled, if writing to a register that is associated to trigger 0, the data goes directly to the destination register.                | 0   | No  | No              |     |     |
|                  |                       | 2         | TRIGGER_2             | A write of a one to this bit loads trigger 2's registers.   | 0   | Yes   | No              |     |     |
|                  |                       | 1         | TRIGGER_1             | A write of a one to this bit loads trigger 1's registers.   | 0   | Yes   | No              |     | R/W |
|                  |                       | 0         | TRIGGER_0             | A write of a one to this bit loads trigger 0's registers.   | 0   | Yes   | No              |     | R/W |
|                  |                       | 0x001F    | MAN_USID              | 7:6   | SPARE   | These are read-only bits that are reserved and yield a value of 0b00 at readback. | 00              | No  | No  |
| 5:4              | MANUFACTURER_ID [9:8] |           |                       | These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value.                      | 01  |   |                 |     |     |
| 3:0              | USID                  |           |                       | Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device. | USID_Sel12<br>=00 →<br>1000,<br>USID_Sel12<br>=01 →<br>1001,<br>USID_Sel12<br>=10 →<br>1010,<br>USID_Sel12<br>=11 →<br>1011 |   |                 |     |     |

Continued on next page

**Table 10: Register Mapping – Continued from previous page**

| Register Address | Register Name | Data Bits | Function                 | Description  | Default | Broadcast_ID Support | Trigger Support | R/W |
|------------------|---------------|-----------|--------------------------|--|---------|----------------------|-----------------|-----|
| 0x001A           | RFFE_STATUS   | 7         | SOFTWARE RESET           | 0: Normal operation<br>1: Software reset                       | 0       | No                   | No              | R/W |
|                  |               | 6         | COMMAND_FRAME_PARITY_ERR | Command sequence received with parity error - discard command. | 0       | No                   | No              | R   |
|                  |               | 5         | COMMAND_LENGTH_ERR       | Command length error   | 0       |                      |                 |     |
|                  |               | 4         | ADDRESS_FRAME_PARITY_ERR | Address frame parity error = 1                                 | 0       |                      |                 |     |
|                  |               | 3         | DATA_FRAME_PARITY_ERR    | Data frame with parity error                                   | 0       |                      |                 |     |
|                  |               | 2         | READ_UNUSED_REG          | Read command to an invalid address                             | 0       |                      |                 |     |
|                  |               | 1         | WRITE_UNUSED_REG         | Write command to an invalid address                            | 0       |                      |                 |     |
|                  |               | 0         | BID_GID_ERR              | Read command with a BROADCAST_ID or GROUP_SID                  | 0       |                      |                 |     |
| 0x001B           | GROUP_SID     | 7:4       | RESERVED                 |  | 0       |                      |                 |     |
|                  |               | 3:0       | GROUP_SID                | Group slave ID   | 0       |                      |                 |     |

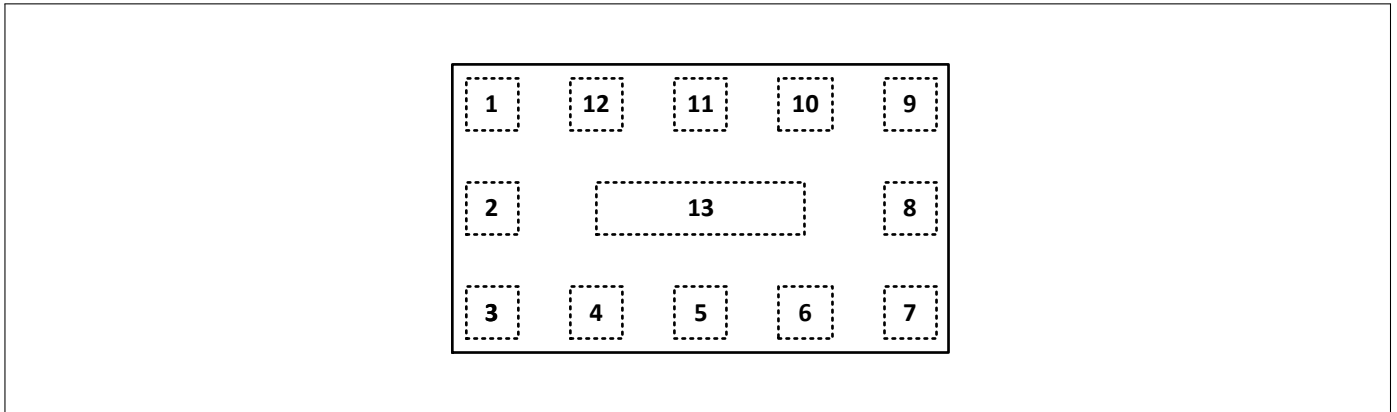
**Table 11: Modes of Operation (Truth Table, Register\_0)**

| State | Mode       | REGISTER_0 Bits |    |    |    |    |    |    |    |
|-------|------------|-----------------|----|----|----|----|----|----|----|
|       |            | D7              | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 1     | Isolation  | x               | x  | x  | 0  | 0  | 0  | 0  | 0  |
| 2     | RX1-AI     | x               | x  | x  | 0  | 0  | 0  | 0  | 1  |
| 3     | RX2-AI     | x               | x  | x  | 0  | 0  | 0  | 1  | 0  |
| 4     | RX3-AI     | x               | x  | x  | 0  | 1  | 0  | 0  | 0  |
| 5     | RX4-AI     | x               | x  | x  | 0  | 0  | 1  | 0  | 0  |
| 6     | RX5-AI     | x               | x  | x  | 1  | 0  | 0  | 0  | 0  |
| 7     | RX1&RX2-AI | x               | x  | x  | 0  | 0  | 0  | 1  | 1  |
| 8     | RX2&RX3-AI | x               | x  | x  | 0  | 1  | 0  | 1  | 0  |
| 9     | RX3&RX4-AI | x               | x  | x  | 0  | 1  | 1  | 0  | 0  |
| 10    | RX4&RX5-AI | x               | x  | x  | 1  | 0  | 1  | 0  | 0  |
| 11    | RX1&RX3-AI | x               | x  | x  | 0  | 1  | 0  | 0  | 1  |
| 12    | RX2&RX4-AI | x               | x  | x  | 0  | 0  | 1  | 1  | 0  |
| 13    | RX3&RX5-AI | x               | x  | x  | 1  | 1  | 0  | 0  | 0  |
| 14    | RX1&RX4-AI | x               | x  | x  | 0  | 0  | 1  | 0  | 1  |
| 15    | RX2&RX5-AI | x               | x  | x  | 1  | 0  | 0  | 1  | 0  |
| 16    | RX1&RX5-AI | x               | x  | x  | 1  | 0  | 0  | 0  | 1  |



## 7 Application Information

### Pin Configuration and Function



**Figure 9:** BGS15MA12 Pin Configuration (top view)

**Table 12: Pin Definition and Function**

| Pin No. | Name  | Function                        |
|---------|-------|---------------------------------|
| 1       | SLK   | MIPI RFFE Clock (Input)         |
| 2       | VIO   | MIPI RFFE Power Supply          |
| 3       | RX5   | RF-Port RX No. 5                |
| 4       | RX4   | RF-Port RX No. 4                |
| 5       | RX3   | RF-Port RX No. 3                |
| 6       | RX2   | RF-Port RX No. 2                |
| 7       | RX1   | RF-Port RX No. 1                |
| 8       | SSEL1 | MIPI SEL Port No. 1 (Input)     |
| 9       | SSEL2 | MIPI SEL Port No. 2 (Input)     |
| 10      | AI    | RF-Input Port                   |
| 11      | VBAT  | Power Supply                    |
| 12      | SDATA | MIPI RFFE Data (Input / Output) |
| 13      | GND   | Ground                          |

Application Board Configuration

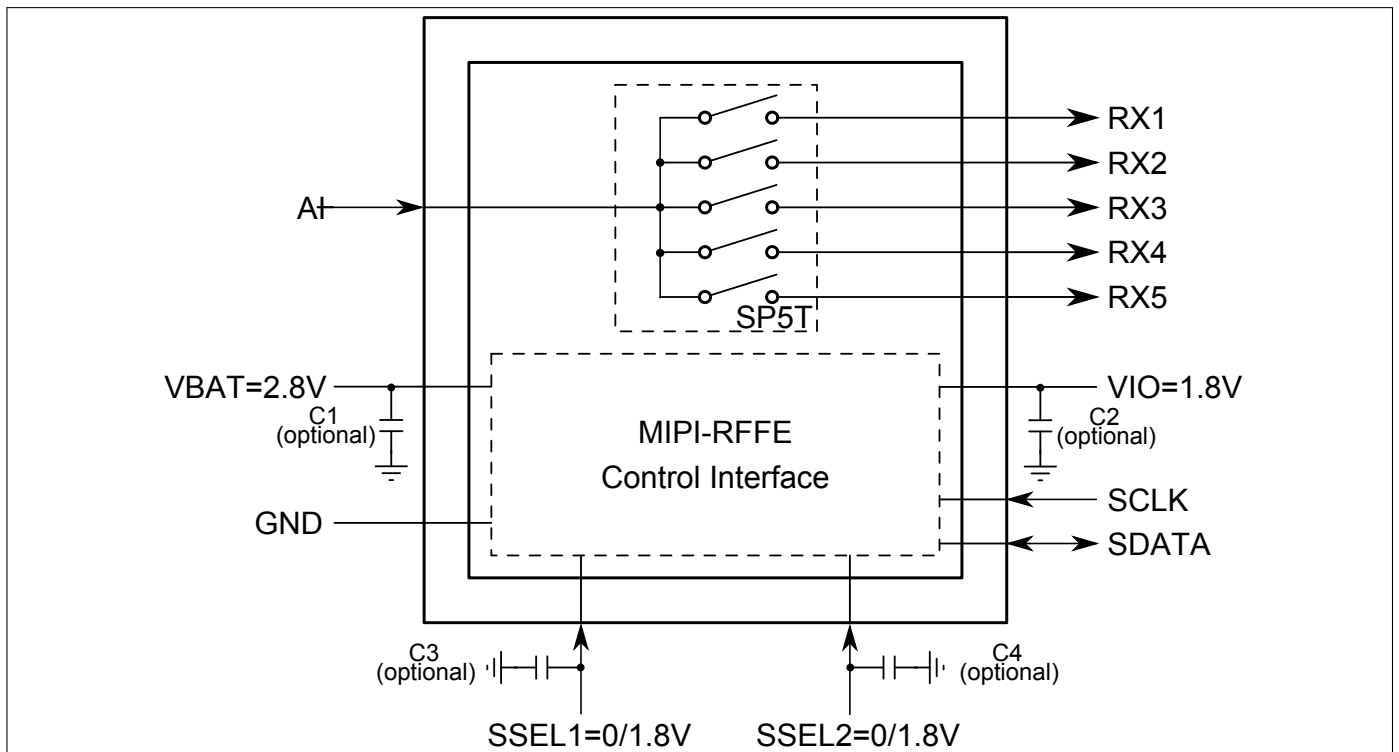


Figure 10: BGS15MA12 Application Schematic

Table 13: Bill of Materials Table

| Name          | Value     | Package    | Manufacturer | Function                |
|---------------|-----------|------------|--------------|-------------------------|
| C1 (optional) | 1 nF      | 0201       | Various      | RF Bypass <sup>1)</sup> |
| C2 (optional) | 1 nF      | 0201       | Various      | RF Bypass <sup>1)</sup> |
| C3 (optional) | 1 nF      | 0201       | Various      | RF Bypass <sup>1)</sup> |
| C4 (optional) | 1 nF      | 0201       | Various      | RF Bypass <sup>1)</sup> |
| N1            | BGS15MA12 | ATSLP-12-4 | Infineon     | RF MOS Switch           |

<sup>1)</sup> RF bypass recommended to mitigate power supply noise

## 8 Package Information

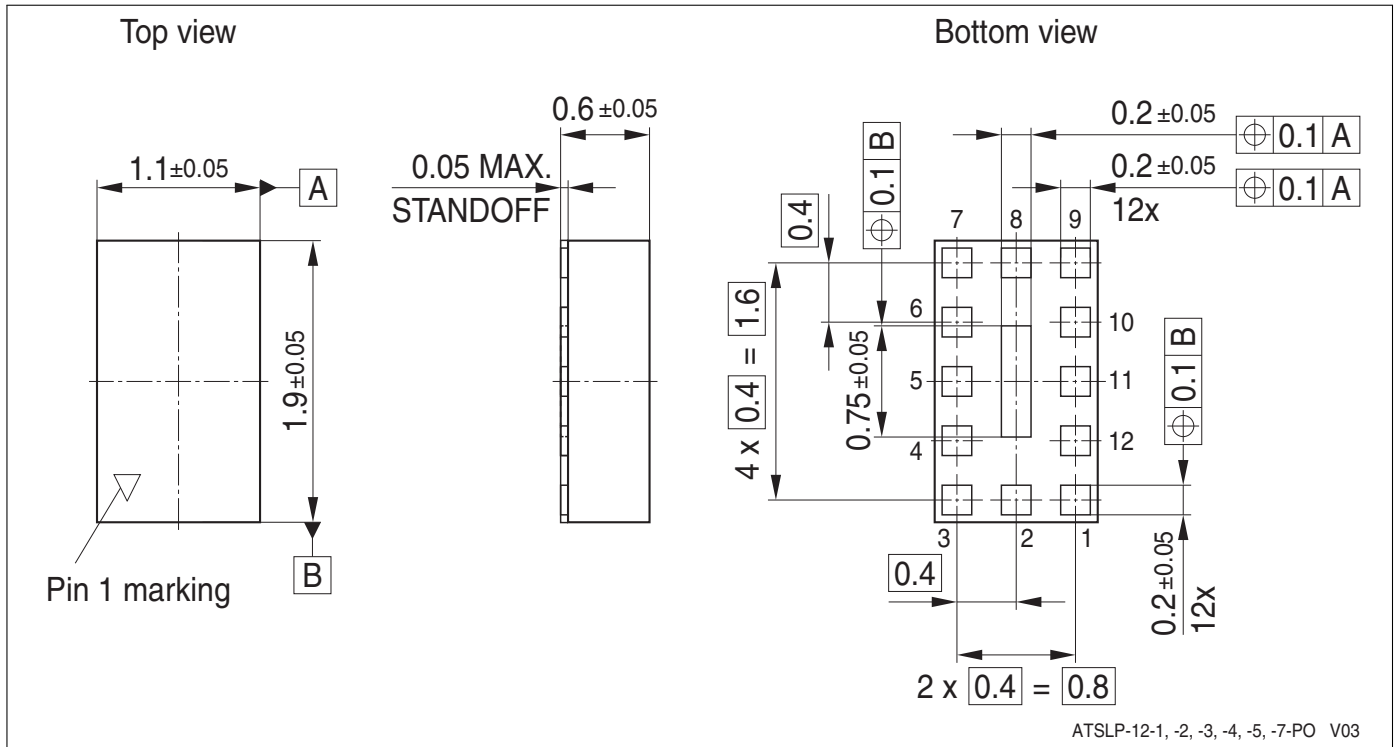


Figure 11: ATSLP-12-4 Package Outline (top, side and bottom views)

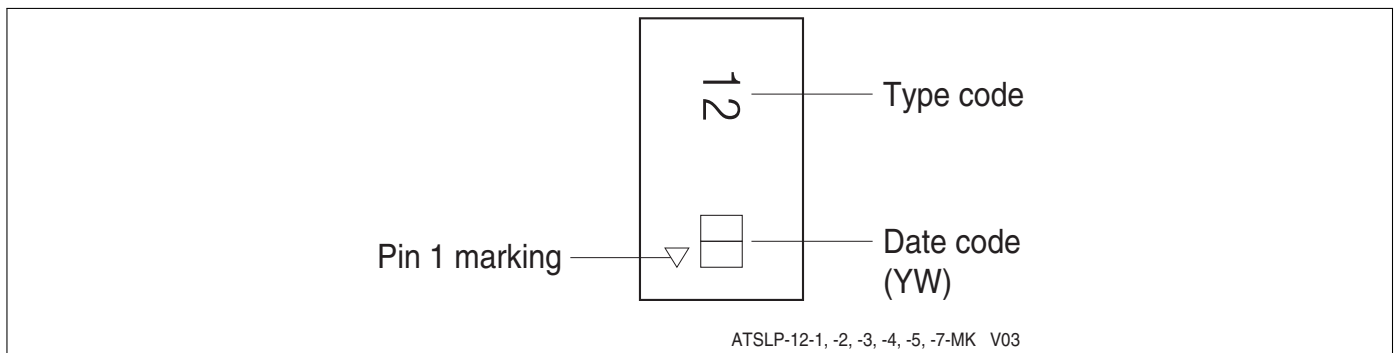


Figure 12: Marking Specification (top view)

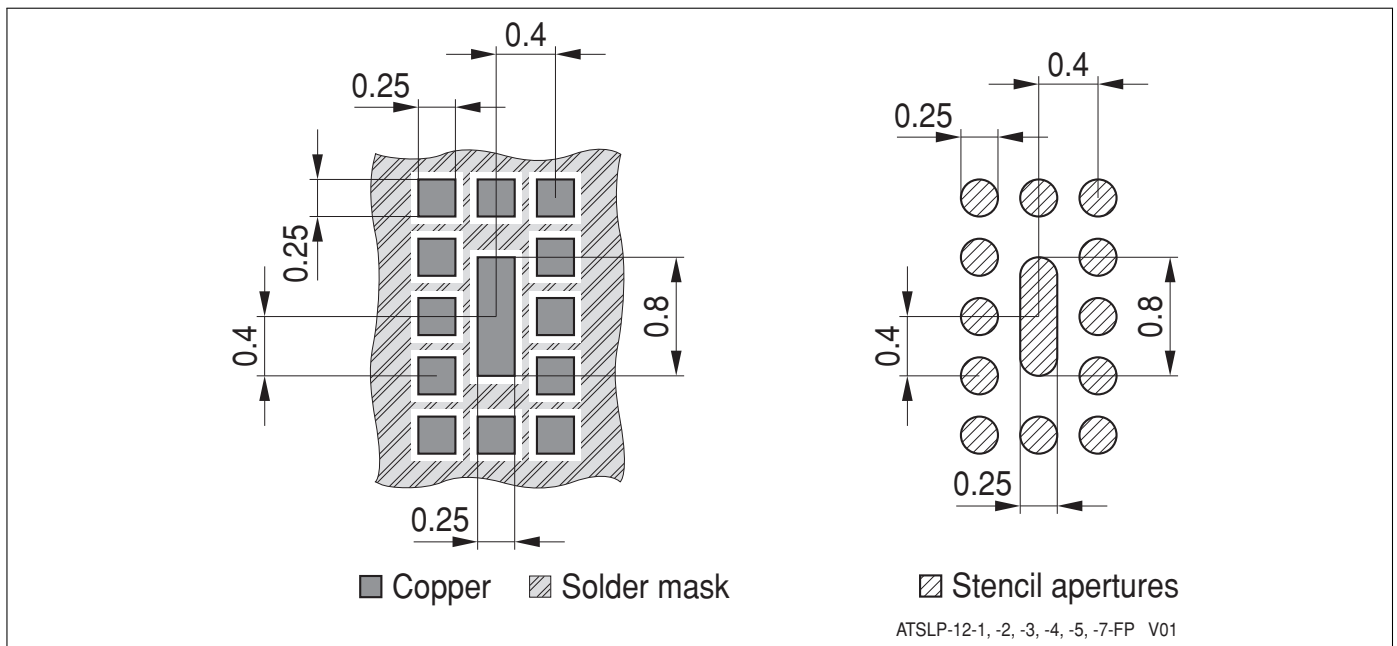


Figure 13: Footprint Recommendation

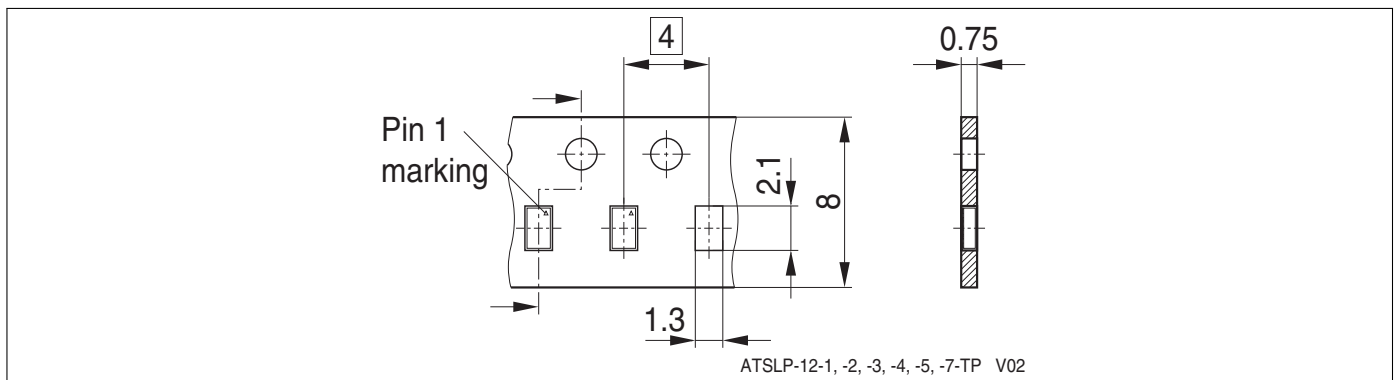


Figure 14: ATSLP-12-4 Carrier Tape

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