International
IOR Rectifier
AN INFINEON TECHNOLOGIES COMPANY

PD-97826A

# RIC7S113A4

## RADIATION HARDENED HIGH AND LOW SIDE GATE DRIVER

### Features

- Total dose capability to 100 kRads(Si)
- Floating channel designed for bootstrap operation
- Fully operational to +400V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 10 to 20V
- Undervoltage lockout for both channels
- Separate logic supply range from 5 to 20V
  Logic and power ground ±5V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs
- Hermetically Sealed
- Lightweight
- ESD Rating: Class 1C per MIL-STD-883, Method 3015

### Product Summary

| | |
|---|---|
| $V_{OFFSET}$ | 400V max. |
| $I_{O+/-}$ | 2A / 2A |
| $V_{OUT}$ | 10 - 20V |
| $t_{on/off}$ (typ.) | 120 & 100 ns |
| Delay Matching(typ.) | 5 ns |

### Description

The RIC7S113A4 is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 400 volts.

### Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$ | High Side Floating Supply Voltage | -0.5 | $V_S$ + 20 | V |
| $V_S$ | High Side Floating Supply Offset Voltage | — | 400 | |
| $V_{HO}$ | High Side Floating Output Voltage | $V_S$ - 0.5 | $V_B$ + 0.5 | |
| $V_{CC}$ | Low Side Fixed Supply Voltage | -0.5 | 20 | |
| $V_{LO}$ | Low Side Output Voltage | -0.5 | $V_{CC}$ + 0.5 | |
| $V_{DD}$ | Logic Supply Voltage | -0.5 | $V_{SS}$ + 20 | |
| $V_{SS}$ | Logic Supply Offset Voltage | $V_{CC}$ - 20 | $V_{CC}$ + 0.5 | |
| $V_{IN}$ | Logic Input Voltage (HIN, LIN & SD) | $V_{SS}$ - 0.5 | $V_{DD}$ + 0.5 | |
| $dV_s/dt$ | Allowable Offset Supply Voltage Transient (Figure 2) | — | 50 | V/ns |
| $P_D$ | Package Power Dissipation @ $T_{LEAD} \leq +25°C$ | — | 0.8 | W |
| $R_{thJC}$ | Thermal Resistance, Junction to Case | 12 (Typ) | 15.9 | °C/W |
| $R_{thJ-LEAD}$ | Thermal Resistance, Junction to Lead * | 150 (Typ) | — | |
| $R_{thJ-LID}$ | Thermal Resistance, Junction to Lid * | 27 (Typ) | — | |
| $T_J$ | Junction Temperature | -55 | 125 | °C |
| $T_S$ | Storage Temperature | -55 | 150 | |
| $T_L$ | Lead Temperature (Soldering, 10 seconds) | — | 300 | |
| | Weight | 0.6(typical) | | g |

* Guaranteed by design, not tested

## Recommended Operating Conditions

The Input/Output logic timing diagram is shown in Figure 1. The $V_S$ and $V_{SS}$ offset ratings are tested with all supplies biased at 15V differential.

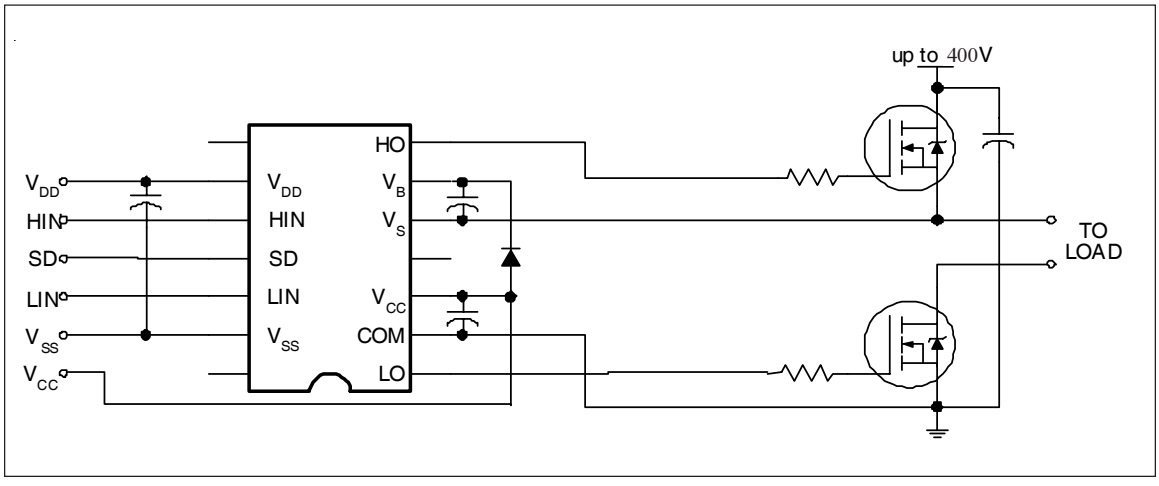
| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $V_B$ | High Side Floating Supply Absolute Voltage | $V_S$ + 10 | $V_S$ + 20 | V |
| $V_S$ | High Side Floating Supply Offset Voltage | -4 | 400 | |
| $V_{HO}$ | High Side Floating Output Voltage | $V_S$ | $V_B$ | |
| $V_{CC}$ | Low Side Fixed Supply Voltage | 10 | 20 | |
| $V_{LO}$ | Low Side Output Voltage | 0 | $V_{CC}$ | |
| $V_{DD}$ | Logic Supply Voltage | $V_{SS}$ + 5 | $V_{SS}$ + 20 | |
| $V_{SS}$ | Logic Supply Offset Voltage | -5 | 5 | |
| $V_{IN}$ | Logic Input Voltage (HIN, LIN & SD) | $V_{SS}$ | $V_{DD}$ | |

## Dynamic Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$, $V_{DD}$) = 15V, and $V_{SS}$ = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

| | | Tj = 25°C | | | Tj = -55 to 125°C | | | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min. | Typ. | Max. | Min. | Max. | Units | Test Conditions |
| $t_{on}$ | Turn-On Propagation Delay | — | 120 | 150 | — | 260 | ns | $V_S$ = 0V |
| $t_{off}$ | Turn-Off Propagation Delay | — | 100 | 125 | — | 220 | | $V_S$ = 400V |
| $t_{sd}$ | Shutdown Propagation Delay | — | 110 | 140 | — | 235 | | $V_S$ = 400V |
| $t_r$ | Turn-On Rise Time | — | 25 | 35 | — | 50 | | $C_L$ = 1000pf |
| $t_f$ | Turn-Off Fall Time | — | 17 | 25 | — | 40 | | $C_L$ = 1000pf |
| MT | Delay Matching, HS & LS Turn-On/Off | — | 5 | 20 | — | — | | $\lvert Ht_{on}-Lt_{on}\rvert$ or $\lvert Ht_{off}-Lt_{off}\rvert$ |

## Typical Connection



## Static Electrical Characteristics

$V_{BIAS}$ ($V_{CC}$, $V_{BS}$, $V_{DD}$) = 15V, unless otherwise specified. The $V_{IN}$, $V_{TH}$ and $I_{IN}$ parameters are referenced to $V_{SS}$ and are applicable to all three logic input pins: HIN, LIN and SD. The $V_O$ and $I_O$ parameters are referenced to COM or $V_S$ and are applicable to the respective output pins: HO or LO.

| | | Tj = 25°C | | Tj = -55 to 125°C | | | |
|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Min. | Max. | Min. | Max. | Units | Test Conditions |
| $V_{IH}$ | Logic "1" Input Voltage | 3.1 | — | 3.3 | — | V | $V_{DD}$ = 5V |
| | | 6.4 | — | 6.8 | — | | $V_{DD}$ = 10V |
| | | 9.5 | — | 10 | — | | $V_{DD}$ = 15V |
| | | 12.5 | — | 13.3 | — | | $V_{DD}$ = 20V |
| $V_{IL}$ | Logic "0" Input Voltage | — | 1.6 | — | 1.6 | V | $V_{DD}$ = 5V |
| | | — | 3.8 | — | 3.6 | | $V_{DD}$ = 10V |
| | | — | 6.0 | — | 5.7 | | $V_{DD}$ = 15V |
| | | — | 8.3 | — | 7.9 | | $V_{DD}$ = 20V |
| $V_{OH}$ | High Level Output Voltage, $V_{BIAS}$ - $V_O$ | — | 1.2 | — | 1.5 | | $V_{IN}$ = $V_{IH}$, $I_O$ = 0A |
| $V_{OL}$ | Low Level Output Voltage, $V_O$ | — | 0.1 | — | 0.1 | | $V_{IN}$ = $V_{IH}$, $I_O$ = 0A |
| $I_{LK}$ | Offset Supply Leakage Current | — | 50 | — | 250 | µA | $V_B$ = $V_S$ = 400V |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | — | 230 | — | 500 | | $V_{IN}$ =0V or $V_{DD}$ |
| $I_{QCC}$ | Quiescent $V_{CC}$ Supply Current | — | 340 | — | 600 | | $V_{IN}$ =0V, or $V_{DD}$ |
| $I_{QDD}$ | Quiescent $V_{DD}$ Supply Current | — | 30 | — | 60 | | $V_{IN}$ =0V, or $V_{DD}$ |
| $I_{IN+}$ | Logic "1" Input Bias Current | — | 40 | — | 70 | | $V_{IN}$ = $V_{DD}$ |
| $I_{IN-}$ | Logic "0" Input Bias Current | — | 1.0 | — | 10 | | $V_{IN}$ = 0V |
| $V_{BSUV+}$ | $V_{BS}$ Supply Undervoltage Positive Going Threshold | 7.5 | 9.7 | — | | — | |
| $V_{BSUV-}$ | $V_{BS}$ Supply Undervoltage Negative Going Threshold | 7.0 | 9.4 | — | — | | |
| $V_{CCUV+}$ | $V_{CC}$ Supply Undervoltage Positive Going Threshold | 7.4 | 9.6 | — | — | V | |
| $V_{CCUV-}$ | $V_{CC}$ Supply Undervoltage Negative Going Threshold | 7.0 | 9.4 | — | — | | |
| $I_{O+}$ | Output High Short Circuit Pulsed Current * | 2.0 | — | — | — | A | $V_O$ = 0V, $V_{IN}$ = $V_{DD}$ PW ≤ 10 µs |
| $I_{O-}$ | Output Low Short Circuit Pulsed Current * | 2.0 | — | — | — | | $V_O$ = 15V, $V_{IN}$ = 0V PW ≤ 10 µs |

* Guaranteed by design, not tested

## Radiation Performance

International Rectifier Radiation Hardened gate drivers are tested to verify their hardness capability. The hardness assurance program at International rectifier uses a Cobalt-60 ($^{60}$Co) source and heavy ion irradiation.

Every wafer shall be tested per MIL-STD-883, Method 1019, test condition A "Ionizing Radiation (Total Dose) Test Procedure".

Both pre- and post- irradiation performances are tested and specified using the same drive circuitry and test conditions to provide a direct comparison.

For Static Irradiation Test Conditions refer to Figure 7.

## Static Electrical Characteristics

Tj = 25°C

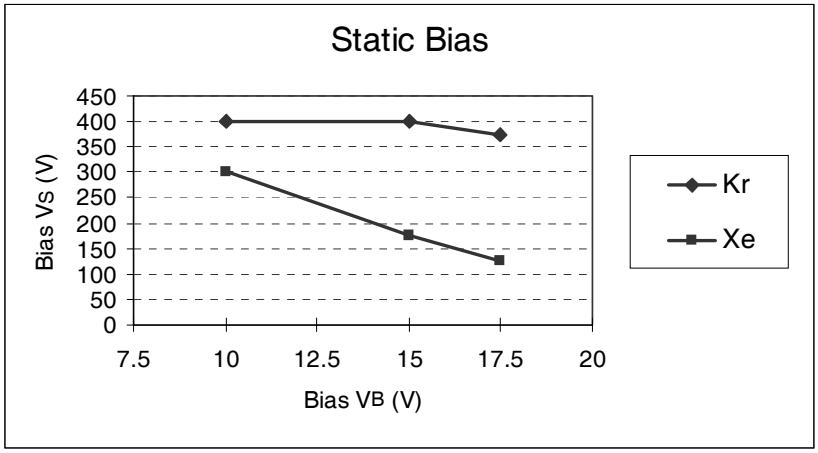
| Symbol | Parameter | 100K Rads (Si) Min | 100K Rads (Si) Max | Units | Test Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | Logic "1" Input Voltage | 3.1 | — | V | VDD = 5V |
| | | 6.4 | — | | VDD = 10V |
| | | 9.5 | — | | VDD = 15V |
| | | 12.5 | — | | VDD = 20V |
| $V_{IL}$ | Logic "0" Input Voltage | — | 1.6 | V | VDD = 5V |
| | | — | 1.6 | | VDD = 10V |
| | | | 6.0 | | VDD = 15V |
| | | — | 8.3 | | VDD = 20V |
| $V_{OH}$ | High Level Output Voltage, $V_{BIAS}$ - $V_O$ | — | 1.2 | | $V_{IN}$ =$V_{IH}$, $I_O$ = 0A |
| $V_{OL}$ | Low Level Output Voltage, $V_O$ | — | 0.1 | | $V_{IN}$ =$V_{IH}$, $I_O$ = 0A |
| $I_{LK}$ | Offset Supply Leakage Current | — | 50 | µA | VB =VS = 400V |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | — | 230 | | VIN =0V or VDD |
| $I_{QCC}$ | Quiescent $V_{CC}$ Supply Current | — | 340 | | VIN =0V or VDD |
| $I_{QDD}$ | Quiescent $V_{DD}$ Supply Current | — | 30 | | VIN =0V or VDD |
| $I_{IN+}$ | Logic "1" Input Bias Current | — | 40 | | VIN =VDD |
| $I_{IN-}$ | Logic "0" Input Bias Current | — | 1.0 | | VIN =0V |
| $V_{BSUV+}$ | $V_{BS}$ Supply Undervoltage Positive Going Threshold | 7.5 | 9.7 | V | |
| $V_{BSUV-}$ | $V_{BS}$ Supply Undervoltage Negative Going Threshold | 7.0 | 9.4 | | |
| $V_{CCUV+}$ | $V_{CC}$ Supply Undervoltage Positive Going Threshold | 7.4 | 9.9 | | |
| $V_{CCUV-}$ | $V_{CC}$ Supply Undervoltage Negative Going Threshold | 7.0 | 9.6 | | |
| $I_{O+}$ | Output High Short Circuit Pulsed Current * | 2.0 | — | A | VO =0V, VIN =VDD PW ≤ 10 µs |
| $I_{O-}$ | Output Low Short Circuit Pulsed Current * | 2.0 | — | | VO =15V, VIN =0V PW ≤ 10 µs |

* Guaranteed by design, not tested

International Rectifier radiation hardened Gate Drivers have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization data is illustrated in Table and Curve below. For Static Bias Test Conditions refer to Figure 8.

## Single Event Effect Safe Operating Area

| Ion | LET (MeV/(mg/cm$^2$)) | Energy (MeV) | Range (µm) | $V_{CC}/V_{DD}$ | $V_S$ (V) | | |
|---|---|---|---|---|---|---|---|
| | | | | | $V_B$ = 10V | $V_B$ = 15V | $V_B$ = 17.5V |
| Kr | 27.2 | 1089 | 143 | 20V | 400 | 400 | 375 |
| Xe | 50.4 | 1618 | 128.7 | 20V | 300 | 175 | 125 |



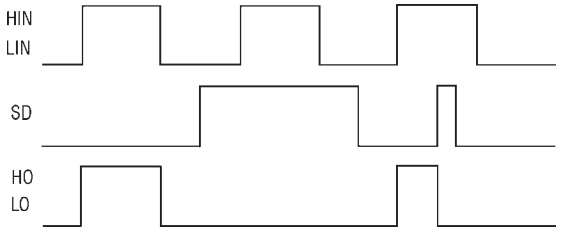



Figure 1. Input/Output Logic Timing Diagram

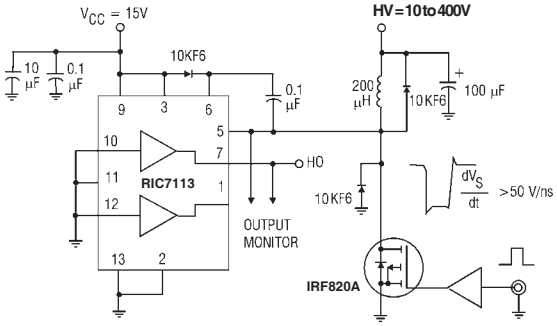



Figure 2. Floating Supply Voltage Transient Test Circuit

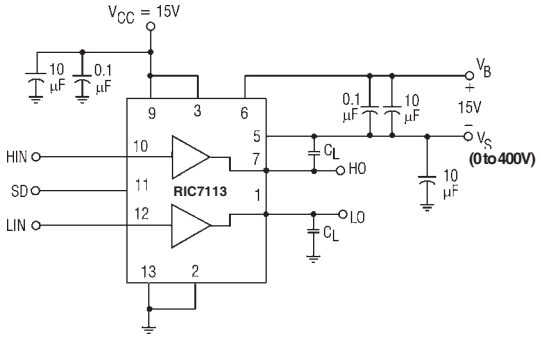



Figure 3. Switching Time Test Circuit

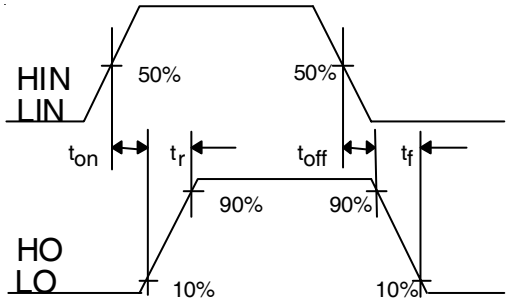



Figure 4. Switching Time Waveform Definition

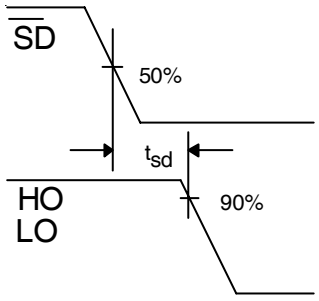



Figure 5. Shutdown Waveform Definitions

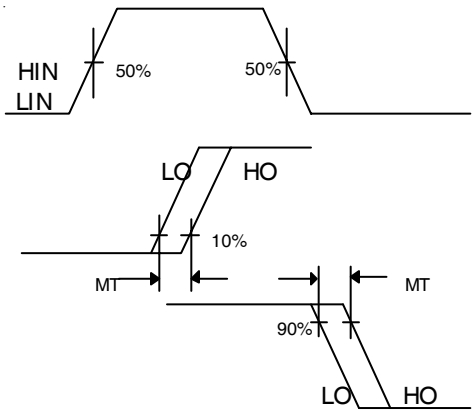



Figure 6. Delay Matching Waveform Definitions

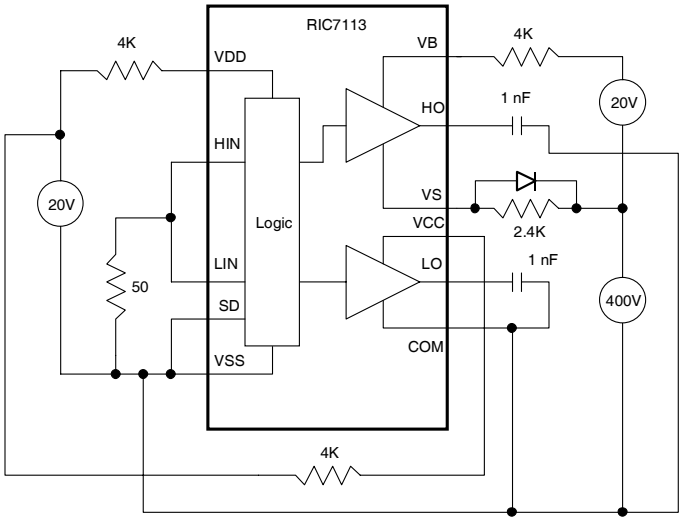



Figure 7. Static Bias Conditions for Total Ionizing DoseTest

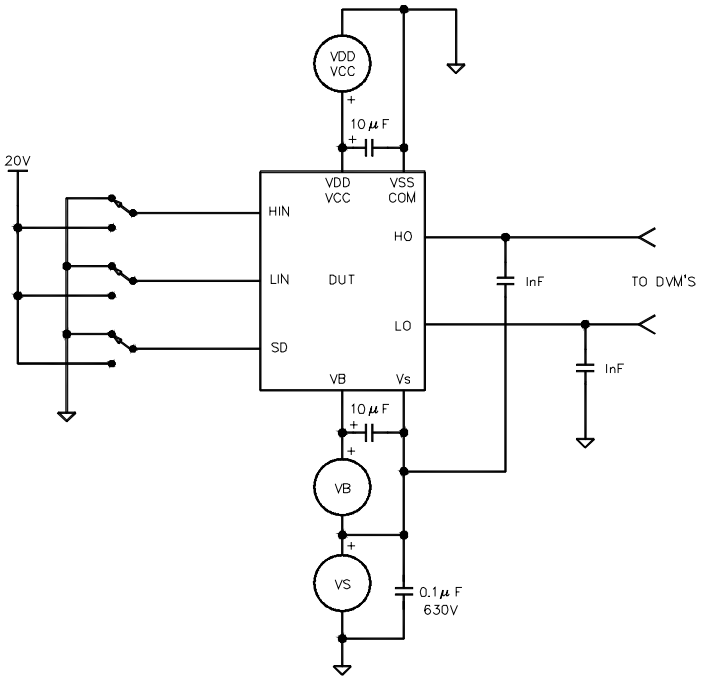
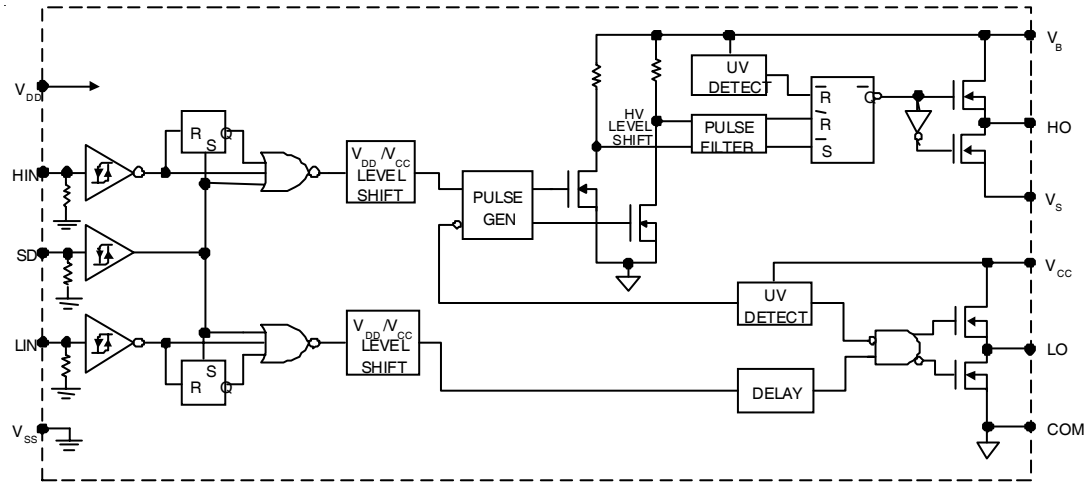



Figure 8. Static Bias Conditions for Single Event Effect Test

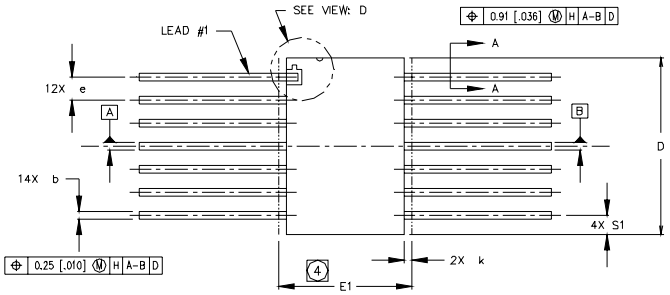
## Functional Block Diagram

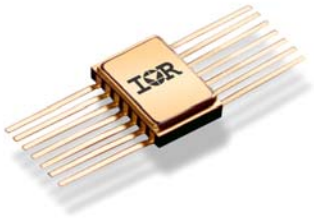


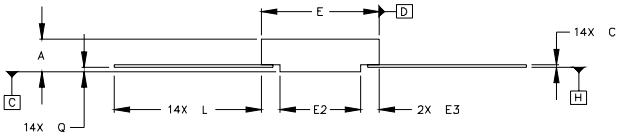

## Lead Definitions

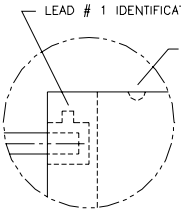
| Symbol | Description |
|---|---|
| $V_{DD}$ | Logic supply |
| HIN | Logic input for high side gate driver output (HO), in phase |
| SD | Logic input for shutdown |
| LIN | Logic input for low side gate driver output (LO), in phase |
| $V_{SS}$ | Logic ground |
| $V_B$ | High side floating supply |
| HO | High side gate drive output |
| $V_S$ | High side floating supply return |
| $V_{CC}$ | Low side supply |
| LO | Low side gate drive output |
| COM | Low side return |

## Case Outline and Dimensions — 14 Lead FlatPack



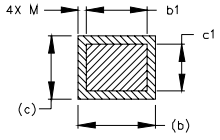






VIEW D

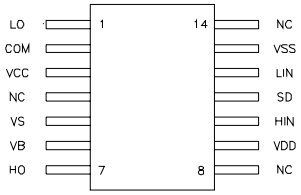
LOCATION OF LEAD #1 IDENTIFICATION MARKS




SECTION A–A

| SYMBOL | DIMENSIONS | | | |
|---|---|---|---|---|
| | MILLIMETERS | | INCHES | |
| | MIN | MAX | MIN | MAX |
| A | 1.14 | 2.92 | .045 | .115 |
| b | 0.38 | 0.56 | .015 | .022 |
| b1 | 0.38 | 0.48 | .015 | .019 |
| c | 0.10 | 0.23 | .004 | .009 |
| c1 | 0.10 | 0.15 | .004 | .006 |
| D | --- | 9.91 | --- | .390 |
| E | 5.97 | 6.60 | .235 | .260 |
| E1 | --- | 7.37 | --- | .290 |
| E2 | 3.18 | --- | .125 | --- |
| E3 | 0.76 | --- | .030 | --- |
| e | 1.27 BSC | | .050 BSC | |
| k | 0.20 | 0.38 | .008 | .015 |
| L | 6.86 | 9.40 | .270 | .370 |
| Q | 0.18 | 0.33 | .007 | .013 |
| S1 | 0.13 | --- | 005 | --- |
| M | --- | 0.04 | --- | .0015 |

LEAD ASSIGNMENT




NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLING DIMENSION: INCH
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. OUTLINE CONFORMS TO MIL–STD–1835C, OUTLINE CDFP3–F14 EXCEPT FOR DIMENSION Q.

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*Data and specifications subject to change without notice. 10/2015*

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>>Infineon Technologies(英飞凌)