

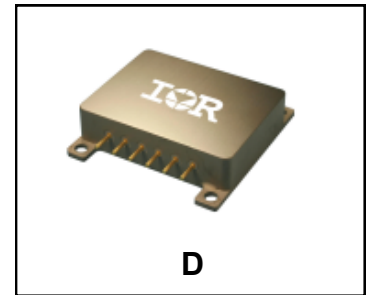
**HIGH RELIABILITY
RADIATION HARDENED
LOW POWER
DC-DC CONVERTER****Description**

The D-Series of DC-DC converters are low power radiation hardened, high reliability devices designed for radiation environments such as those encountered by geostationary earth orbit satellites, deep space probes and communication systems. Features include small size, high efficiency, low weight and a high tolerance to total ionizing dose, single event effects, and environmental stresses such as temperature extremes, mechanical shock, and vibration. All components are fully de-rated to meet the requirements of EEE-INST-002. Extensive documentation including worst case analysis, radiation susceptibility, thermal analysis, stress analysis, and reliability analysis are available.

The D-Series converters have two outputs, each is independently regulated. The outputs can be both positive or one positive and one negative. The D-Series converters incorporate a fixed frequency flyback power stage topology and internal EMI filter. The converters include an enhanced input EMI filter that meets most major satellite power buses. The converters can be remotely turned on and off via an Inhibit pin. Additional Inhibit pins are also provided to control the outputs individually. This feature facilitates turn-on outputs sequencing if desired. Each converter is encased in a cold rolled steel hermetic package. The package measures 1.80"L x 1.40"W x 0.42"H and weighs less than 55 grams. The package utilizes rugged ceramic feed-through copper core pins and is hermetically sealed using parallel seam welding. Two package options are available. Please refer to page 8 for I/O configurations.

Environmental screening includes temperature cycling, constant acceleration, fine and gross leak, and burn-in as specified by MIL-PRF-38534 for class H hybrids.

Non-flight versions of the D-Series converters are available for system development purposes. Variations in electrical specifications and screening to meet custom requirements can be accommodated.

**26 to 50V Input, Regulated Dual Output
(+1.8V and +3.3V)****Features**

- Total Dose Guaranteed to 50 kRad(Si)
- SEE with LET up to 40 MeV·cm²/mg
- Low Weight < 55 grams
- 26V to 55V DC Input Range
- Up to 10W Output Power
- Independently Regulated Outputs:
+1.8V and +3.3V and Other Outputs Available
- -55°C to +80°C Operating Temperature Range
- 100MΩ @ 100VDC Isolation
- Input Under-Voltage Protection
- Meets Conducted Emission Requirements of Most Major Power Buses:
100Hz - 100kHz: 80dBμArms
100kHz - 10MHz: Log-linear Decrease
10MHz - 50MHz: 40dBμArms
- Short Circuit and Overload Protection
- Meets the De-rating Requirements of EEE-INST-002
- On/Off Control via Converter's Inhibit Pin and Individual Output's Inhibit Pin
- High CS Damping

Applications

- Launch Vehicles
- Communication Systems
- Geostationary or Low Earth Orbit Satellites

Circuit Description

The D-Series DC-DC converters utilize two-stage regulation with a fly back topology with a switching frequency of 250kHz for primary regulation and linear post regulation in the secondary for each of the outputs.

Output power is limited under any load fault condition to approximately 110% of rated output. An overload condition causes the converter output to behave like a constant current source with the output voltage dropping below nominal. The converter will resume normal operation when the load current is reduced below the current limit point. This protects the converter from both overload and short circuit conditions. There are no latching elements to eliminate the possibility of falsely triggering the protection circuits during single event radiation exposure.

An under-voltage protection circuit prohibits the converter from operating when the line voltage is too low for safe operation. The converter will not start until the line voltage rises to approximately 20V.

An inhibit pin is provided to control converter operation. This inhibit pin is intended for operation with an open collector transistor drive or a relay closure to the input return. The pin may be left open for normal operation and has a nominal open circuit voltage of 4.0V. Also provided are the individual output on/off control pins (Pin 10, Output 1 Inhibit and Pin 9, Output 2 Inhibit).

Synchronization input pin is included allowing multiple converters to operate at a common switching frequency. Converters can be synchronized to a common frequency with an external clock. This may be used to eliminate beat frequency noise or to avoid generating noise at certain frequencies for noise sensitive systems.

Design Methodology

The D-Series is developed using a proven conservative design methodology, which includes selecting radiation tolerant and established reliability components and fully de-rating to the requirements of EEE-INST-002. Heavy de-rating of the radiation-hardened power MOSFET virtually eliminates the possibility of SEGR and SEB.

Specifications

Absolute Maximum Ratings		Recommended Operating Conditions	
Input Voltage range	-0.5V _{DC} to +80V _{DC}	Input Voltage range (Note 13)	26V _{DC} to 55V _{DC}
Output power	Internally limited	Output power	0 to Max. Rated
Lead Temperature	+300°C for 10 seconds	Operating temperature	-55°C to +115°C
Operating Case temperature (Note 12)	-55°C to +125°C	Operating temperature	-55°C to +80°C
Storage temperature	-55°C to +135°C	De-rated (Note 13)	

Electrical Performance Characteristics

Parameter	Group A Subgroup	Conditions -55°C ≤ T _C ≤ +85°C V _{IN} = 42V DC ± 5%, C _L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Input Voltage			26	42	55	V
Output voltage (V _{OUT}) (Out 1/Out 2)						V/μs
1.8V	1	I _{OUT} = 100% rated load	1.782	1.800	1.818	V
3.3V	1		3.267	3.300	3.333	
1.8V	2,3	I _{OUT} = 100% rated load	1.746	1.800	1.854	V
3.3V	2,3		3.200	3.300	3.399	
Output power (P _{OUT}) (Out 1/Out 2)		V _{IN} = 26, 42, 55V, Notes 2, 11 Either Output				W
1.8V	1,2,3		0		2.7	
3.3V			0		5.0	
Output current (I _{OUT}) (Out 1/Out 2)		V _{IN} = 26, 42, 55V, Notes 2, 11 Either Output				A
1.8V	1,2,3		0		1.5	
3.3V	1,2,3		0		1.5	
Line regulation (VR _{LINE}) Each Output	1,2,3	V _{IN} = 26, 42, 55V I _{OUT} = 0%, 50%, 100% rated	-0.2		0.2	%
Load regulation (VR _{LOAD}) Each Output	1,2,3	I _{OUT} = 0%, 50%, 100% rated V _{IN} = 26, 42, 55V	-0.5		1.5	%
Cross regulation (VR _{CROSS})	1,2,3	V _{IN} = 26, 42, 55V, Note 1			5.0	mV
Input current (I _{IN})		I _{OUT} = 0, Pin 6 open Pin 6 connected to Pin 2			35 10	mA
Switching frequency (F _S)	1,2,3		225	250	275	kHz
Synchronization Input	1,2,3	External clock on sync In (Pin 4)	450		500	kHz
Frequency range			2.5		5.0	V
Pulse high level			-0.5		0.5	V
Pulse low level			40			V/μs
Pulse transition time			20		80	%

For Notes to Electrical Performance Characteristics Table, refer to page 5

Electrical Performance Characteristics (continued)

Parameter	Group A Subgroup	Conditions -55°C ≤ T _C ≤ +85°C V _{IN} = 42V DC ± 5%, C _L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
Output ripple (V _{RIP}) Each output 1.8V 3.3V	1,2,3	V _{IN} = 26, 42, 55V I _{OUT} = 100% rated load Note 3			50 50	mV p-p
Output ripple @ switch frequency	1,2,3	V _{IN} = 26, 42, 55V I _{OUT} = 100% rated load, Note 1		0.5	0.75	mVp-p
Efficiency (E _{FF})	1,2,3	I _{OUT} = 100% rated load	45	47		%
Enable Input (Inhibit) Open circuit voltage Drive current (sink) Voltage range	1,2,3	Note 1	0 -0.5		4 600 50	V μA V
Current Limit Point Each output 1.8V 3.3V	1,2,3	V _{OUT} = 90% of Nominal Note 10	105 105		145 145	%
Power dissipation load fault (P _D)	1,2,3	Short Circuit, Overload, Note 5			24	W
Output response to step load changes (V _{TLD}) 1.8V 3.3V	4,5,6	Half Load to/ from Full Load, Note 6	-15 -15		15 15	mVpk
Recovery time, step load changes (T _{TLD}) 1.8V 3.3V	4,5,6	Half Load to/from Full Load, Notes 6, 7			500 500	μs
Recovery time, step line changes (T _{TLN})	4,5,6	26V to/from 55V I _{OUT} = 100% rated load, Notes 1, 7, 8			100	μs
Turn-on Response Overshoot (V _{OS}) 1.8V 3.3V Turn-on Delay (T _{DLY})	4,5,6	10% Load, Full Load Note 9	0.2		25 25 10	mV mV ms
Capacitive Load (C _L) 1.8V 3.3V	1	I _{OUT} = 100% rated load No effect on DC performance, Notes 1, 4 Each output			220 220	μF

For Notes to Electrical Performance Characteristics Table, refer to page 5

Electrical Performance Characteristics (continued)

Parameter	Group A Subgroup	Conditions -55°C ≤ T _C ≤ +85°C V _{IN} = 42V DC ± 5%, C _L = 0 unless otherwise specified	Limits			Unit
			Min	Nom	Max	
EMC conducted susceptibility (Line rejection)	1	I _{OUT} = 100% rated load Primary power sine wave injection of 2Vp-p, 100Hz to 50MHz, Note 1	80	90		dB
Electromagnetic Interference (EMI), conducted emission (CE)	1	I _{OUT} = 100% rated load, Note 1	Limits per Figure 1			
Isolation	1	Input to Output or Any Pin to Case except pin 3, test @ 100 VDC	100			MΩ
Device Weight					55	g
MTBF		MIL-HDBK-217F2, SF, 35°C	1 x 10 ⁵			Hours

Notes: Specification and Electrical Performance Characteristics

- Parameter is tested as part of design characterization or after design changes. Thereafter, parameter shall be guaranteed to the limits specified.
- Parameter verified during line and load regulation tests.
- Guaranteed for a D.C. to 20MHz bandwidth. Tested using a 20kHz to 10MHz bandwidth.
- Capacitive load may be any value from 0 to the maximum limit without compromising dc performance. A capacitive load in excess of the maximum limit may interfere with the proper operation of the converter's overload protection, causing erratic behavior during turn-on.
- Overload power dissipation is defined as the device power dissipation with the load set such that both outputs are in a short circuit mode.
- Load step transition time ≤ 10 μs.
- Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of its steady state value.
- Line step transition time ≤ 100 μs.
- Turn-on delay time from either a step application of input power or a logic low to a logic high transition on the inhibit pin (pin 6) to the point where V_{OUT} = 90% of nominal.
- Current limit point expressed as a percentage of full rated load current
- For models with two positive outputs the envelope specification for the design is that each output voltage is limited to the range 1V to 5V.
- Although operation at temperatures between +85°C and +125°C is guaranteed, no parameter limits are specified
- Meets the de-rating requirements of EEE-INST-002 and MIL-STD-1547B – except for ceramic capacitors with voltage stress below 10V will minimum be rated at 50V and a minimum load of 20mA on each output.

Device Screening

Test/Inspection	Method	/EM Suffix ^②	Flight (No suffix)
Element Evaluation	MIL-PRF-38534 class H equivalent with SEM	N/A	X
Nondestructive Bond Pull	MIL-STD-883, Method 2023	N/A	X
Internal Visual	MIL-STD-883, Method 2017	①	X
Temperature Cycling	MIL-STD-883, Method 1010	N/A	Condition C
Constant Acceleration	MIL-STD-883, Method 2001, Y1 Axis	N/A	3000 G's
PIND	MIL-STD-883, Method 2020	N/A	A
Burn-in (2 × 220 hours)	MIL-STD-883, Method 1015	48 hours @115°C	440 hours @115°C
Final Electrical (Group A)	In accordance with device specification	X	X
Seal Fine Leak Gross Leak	MIL-STD-883, Method 1014	Condition A	A1 C
Radiographic	MIL-STD-883, Method 2012	N/A	N/A
External Visual	MIL-STD-883, Method 2009	①	Yes

Notes:

- ① Best commercial practice.
- ② Any Engineering Model (EM) build with the "EM" Suffix shall only be form, fit and functional equivalent to its Flight Model (FM) counterpart, and it may not meet the radiation performance. The EM Model shall not be expected comply with MIL-PRF-38534 flight quality/workmanship standards, and configuration control. An EM build may use electrical equivalent commercial grade components. IR HiRel will provide a list of non-compliance items upon request.

Radiation Performance Characteristics

Test	Conditions	Min	Unit
Total Ionizing Dose (Gamma)*	MIL-STD-883, Method 1019.5 Operating bias applied during exposure, Full Rated Load, $V_{IN} = 50V$	50	kRads(Si)
Single Event Effects* SEU, SEL, SEGR, SEB	Heavy ions (LET) Operating bias applied during exposure, Full Rated Load, $V_{IN} = 26, 42, 55V$	40	MeV·cm ² /mg

* Test performed at TAMU

IR HiRel currently does not have a DLA certified Radiation Hardness Assurance Program.

Fig. 1 – EMI conducted emission Performance Limit

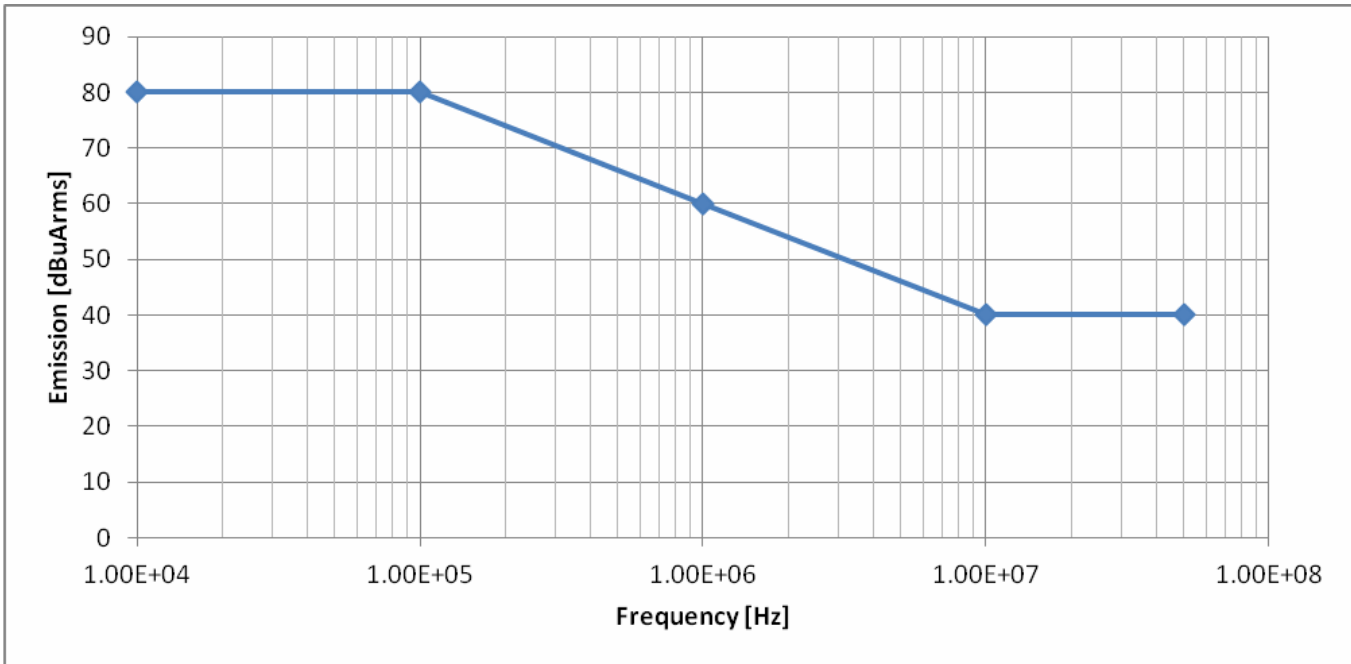
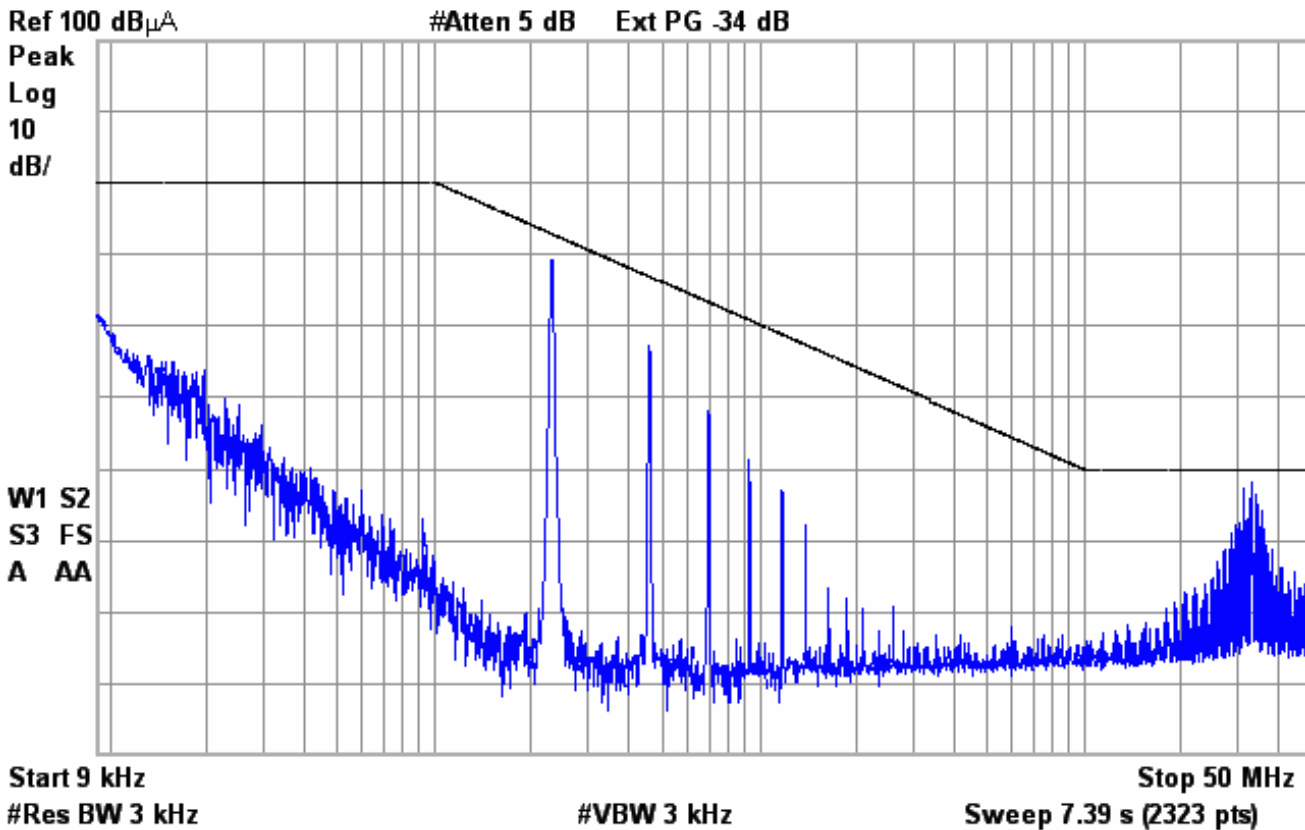
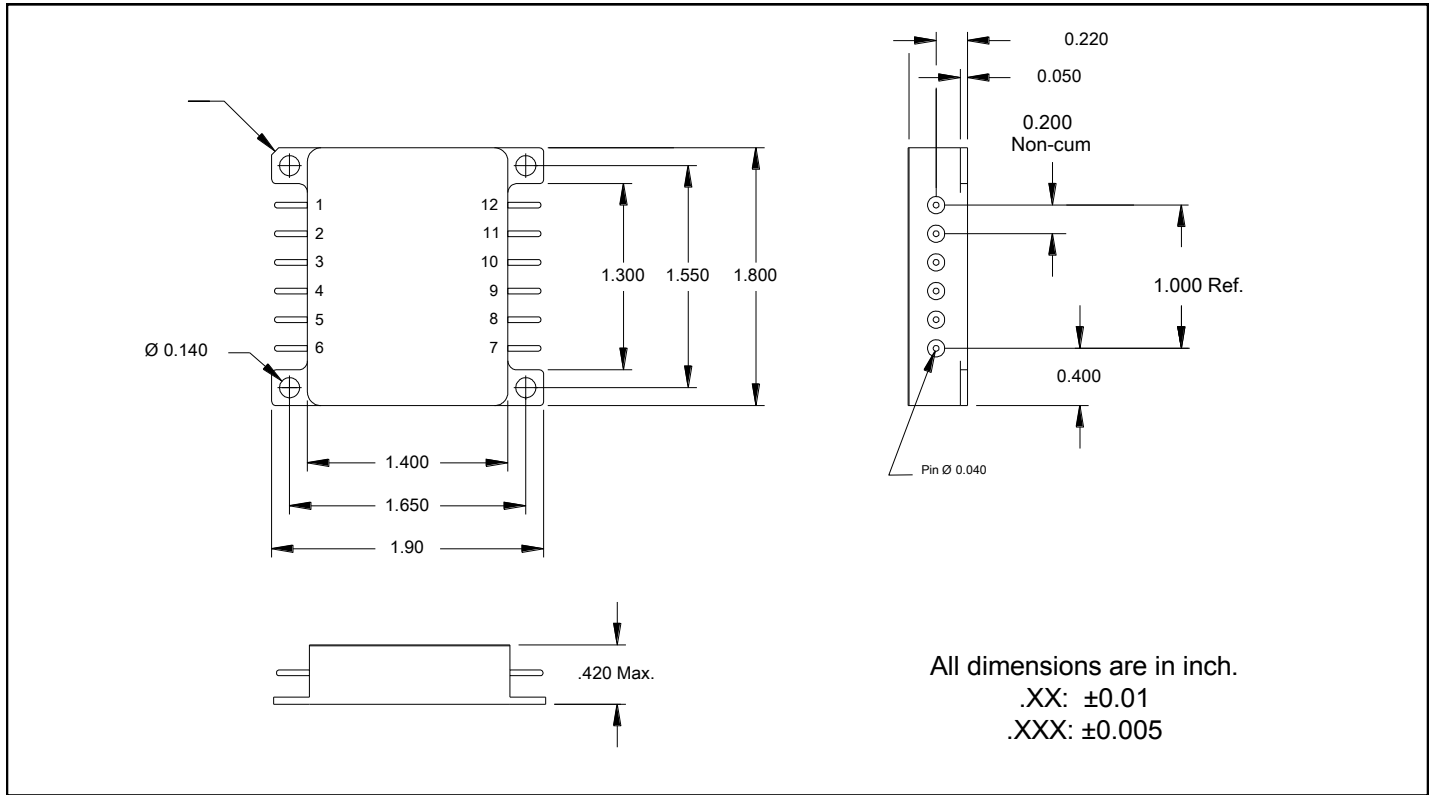


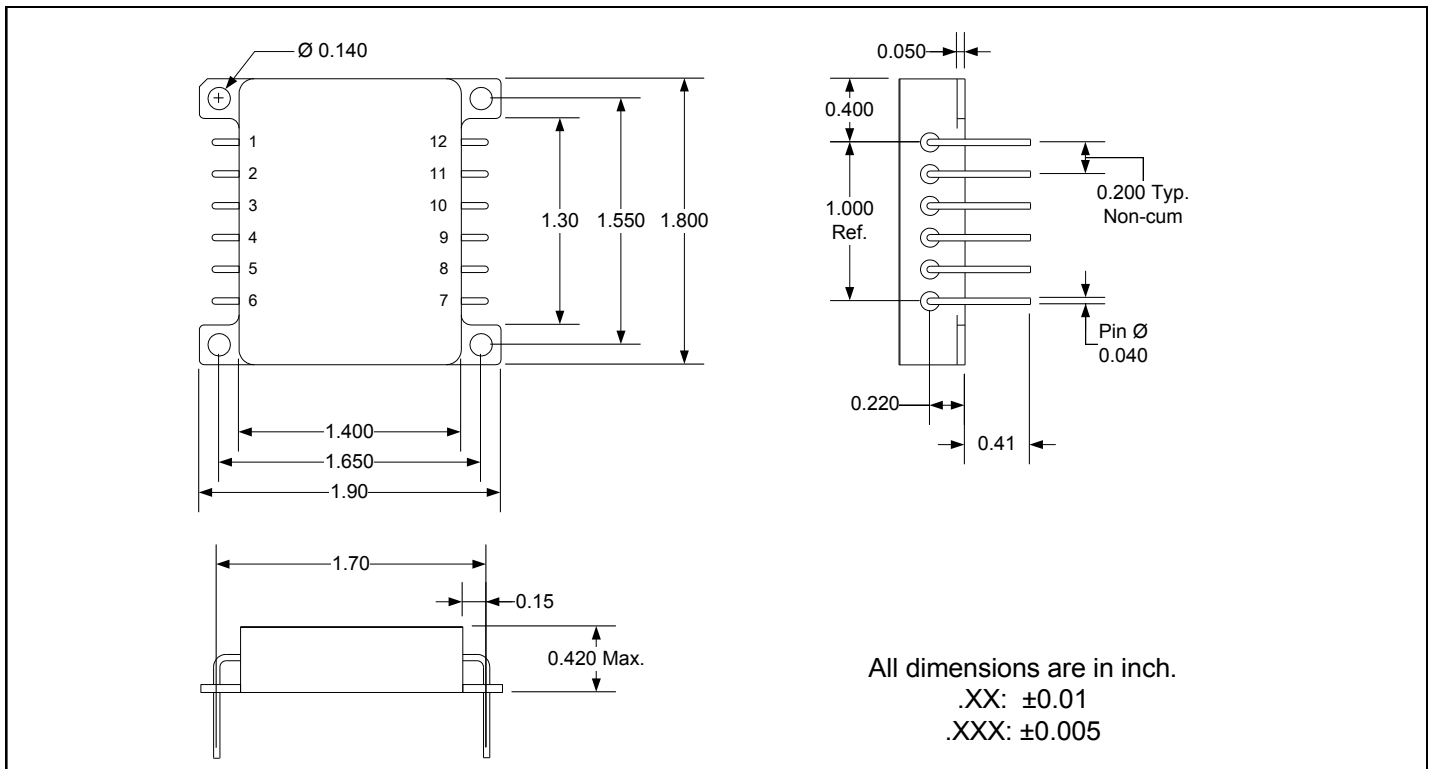
Fig. 2 - A Typical input EMI Conducted Emission Performance



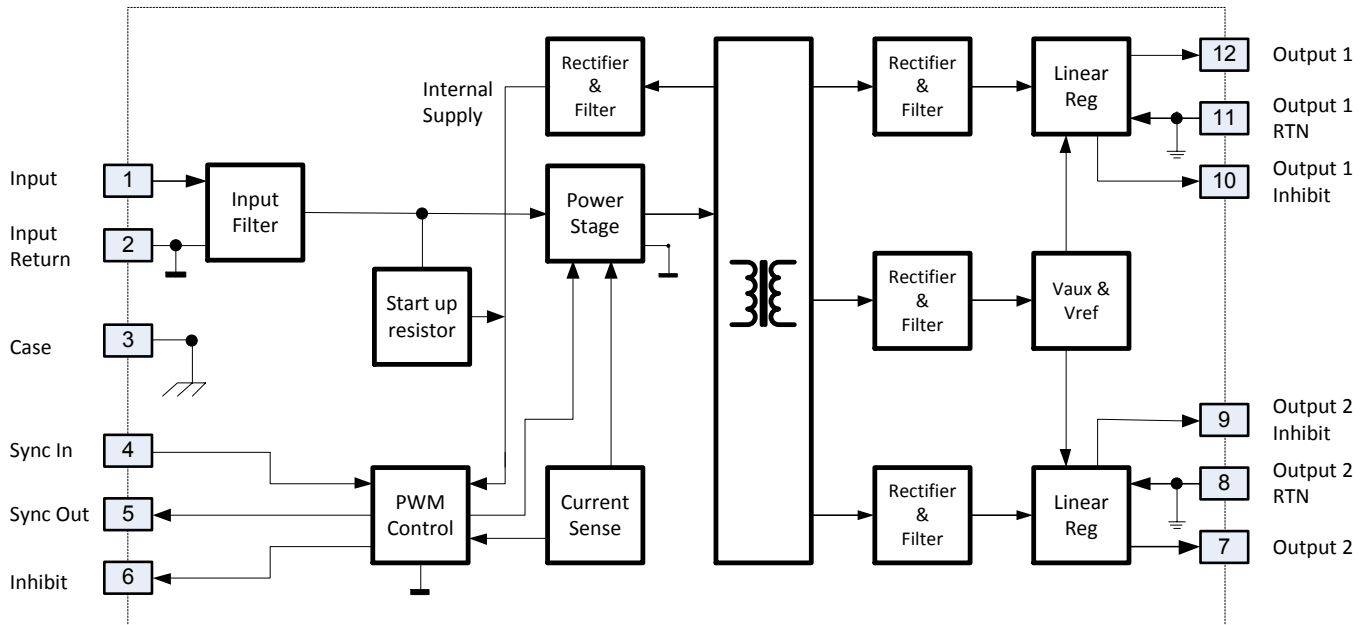
Mechanical Outline - Option A (Straight Pins)



Mechanical Outline - Option B (Down Pins)



Block Diagram

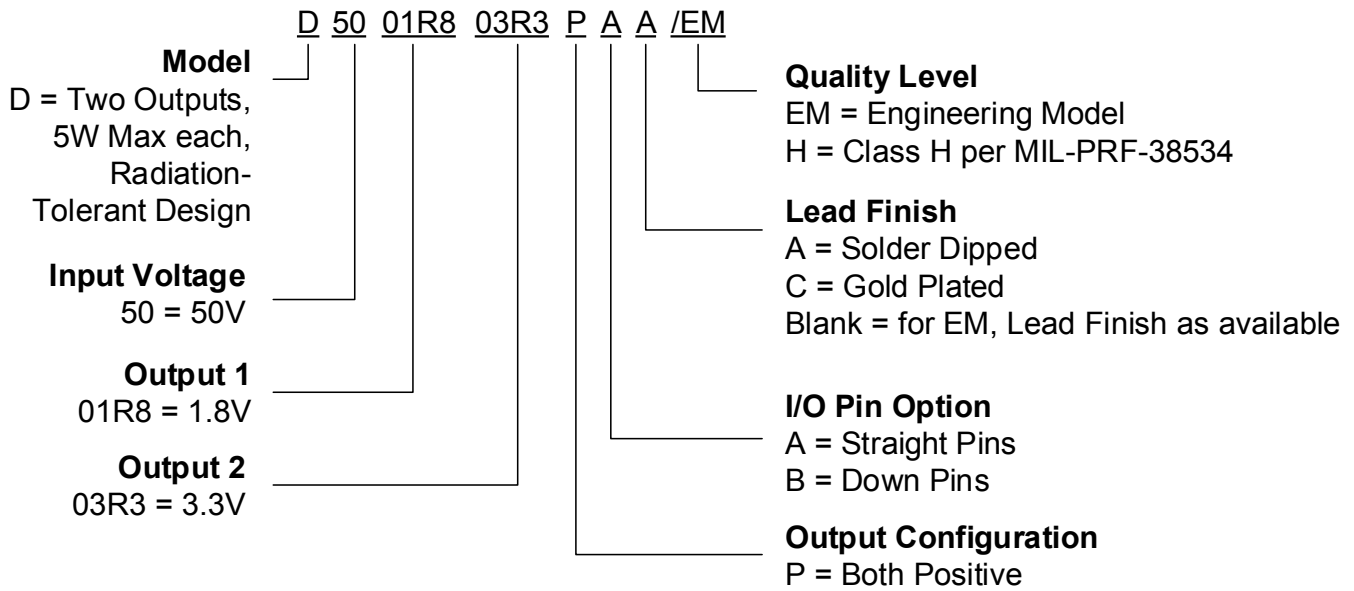


Pin Designation

Pin #	P (Both Output Positive)
1	Input
2	Input Return
3	Case
4	Sync In
5	Sync Out
6	Inhibit
7	Output 2
8	Output 2 Return
9	Output 2 Inhibit
10	Output 1 Inhibit
11	Output 1 Return
12	Output 1

Note: Pins 8 and 11 are internally connected

Part Numbering



IMPORTANT NOTICE

The information given in this document shall be in no event regarded as guarantee of conditions or characteristic. The data contained herein is a characterization of the component based on internal standards and is intended to demonstrate and provide guidance for typical part performance. It will require further evaluation, qualification and analysis to determine suitability in the application environment to confirm compliance to your system requirements.

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