

## IGBT3 Chip Medium Power

### Features:

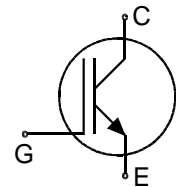
- 650V Trench & Field Stop technology
- high short circuit capability, self limiting short circuit current
- positive temperature coefficient
- easy paralleling
- Qualified according to JEDEC for target applications

### Recommended for:

- power modules

### Applications:

- drives



Chip Type	V <sub>CE</sub>	I <sub>CN</sub>	Die Size	Package
IGC54T65T8RM	650V	100A	5.97 x 8.97 mm <sup>2</sup>	sawn on foil

### Mechanical Parameters

Die size	5.97 x 8.97		mm <sup>2</sup>
Emitter pad size (incl. gate pad)	See chip drawing		
Gate pad size	1.615 x 0.817		
Area total	53.6		µm
Thickness	80		
Wafer size	200		
Max.possible chips per wafer	486		
Passivation frontside	Photoimide		
Pad metal	3200 nm AlSiCu		
Backside metal	Ni Ag –system		
Die bond	Electrically conductive epoxy glue and soft solder		
Wire bond	Al, <500µm		
Reject ink dot size	Ø 0.65mm ; max 1.2mm		
Storage environment	for original and sealed MBB bags	Ambient atmosphere air, Temperature 17°C – 25°C, < 6 month	
	for open MBB bags	Acc. to IEC62258-3: Atmosphere >99% Nitrogen or inert gas, Humidity <25%RH, Temperature 17°C – 25°C, < 6 month	

## Maximum Ratings

Parameter	Symbol	Value	Unit
Collector-Emitter voltage, $T_{vj}=25\text{ °C}$	$V_{CE}$	650	V
DC collector current, limited by $T_{vj\text{ max}}$	$I_C$	1)	A
Pulsed collector current, $t_p$ limited by $T_{vj\text{ max}}$ 2)	$I_{C,puls}$	300	A
Gate emitter voltage	$V_{GE}$	$\pm 20$	V
Operating junction temperature	$T_{vj}$	-40 ... +175	°C
Short circuit data 2)3) $V_{GE} = 15V, V_{CC} = 360V, T_{vj} = 150\text{ °C}$	$t_{SC}$	10	$\mu s$

1) depending on thermal properties of assembly

2) not subject to production test - verified by design/characterization

3) allowed number of short circuits: <1000; time between short circuits: >1s.

## Static Characteristics (tested on wafer), $T_{vj}=25\text{ °C}$

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter breakdown voltage	$V_{(BR)CES}$	$V_{GE}=0V, I_C=4\text{ mA}$	650			V
Collector-Emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15V, I_C=90A$	1.08	1.55	1.82	
Gate-Emitter threshold voltage	$V_{GE(th)}$	$I_C=1.6mA, V_{GE}=V_{CE}$	5.1	5.8	6.4	
Zero gate voltage collector current	$I_{CES}$	$V_{CE}=650V, V_{GE}=0V$			0.54	$\mu A$
Gate-Emitter leakage current	$I_{GES}$	$V_{CE}=0V, V_{GE}=20V$			600	nA
Integrated gate resistor	$r_G$			2		$\Omega$

## Electrical Characteristics (not subject to production test - verified by design / characterization)

Parameter	Symbol	Conditions	Value			Unit
			min.	typ.	max.	
Collector-Emitter saturation voltage	$V_{CEsat}$	$V_{GE}=15V, I_C=100A$		1.55	1.95	V
				1.75		
Input capacitance	$C_{ies}$	$V_{CE}=25V, V_{GE}=0V, f=1MHz, T_{vj}=25\text{ °C}$		6160		pF
Reverse transfer capacitance	$C_{res}$			183		



# IGC54T65T8RM

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## Further Electrical Characteristic

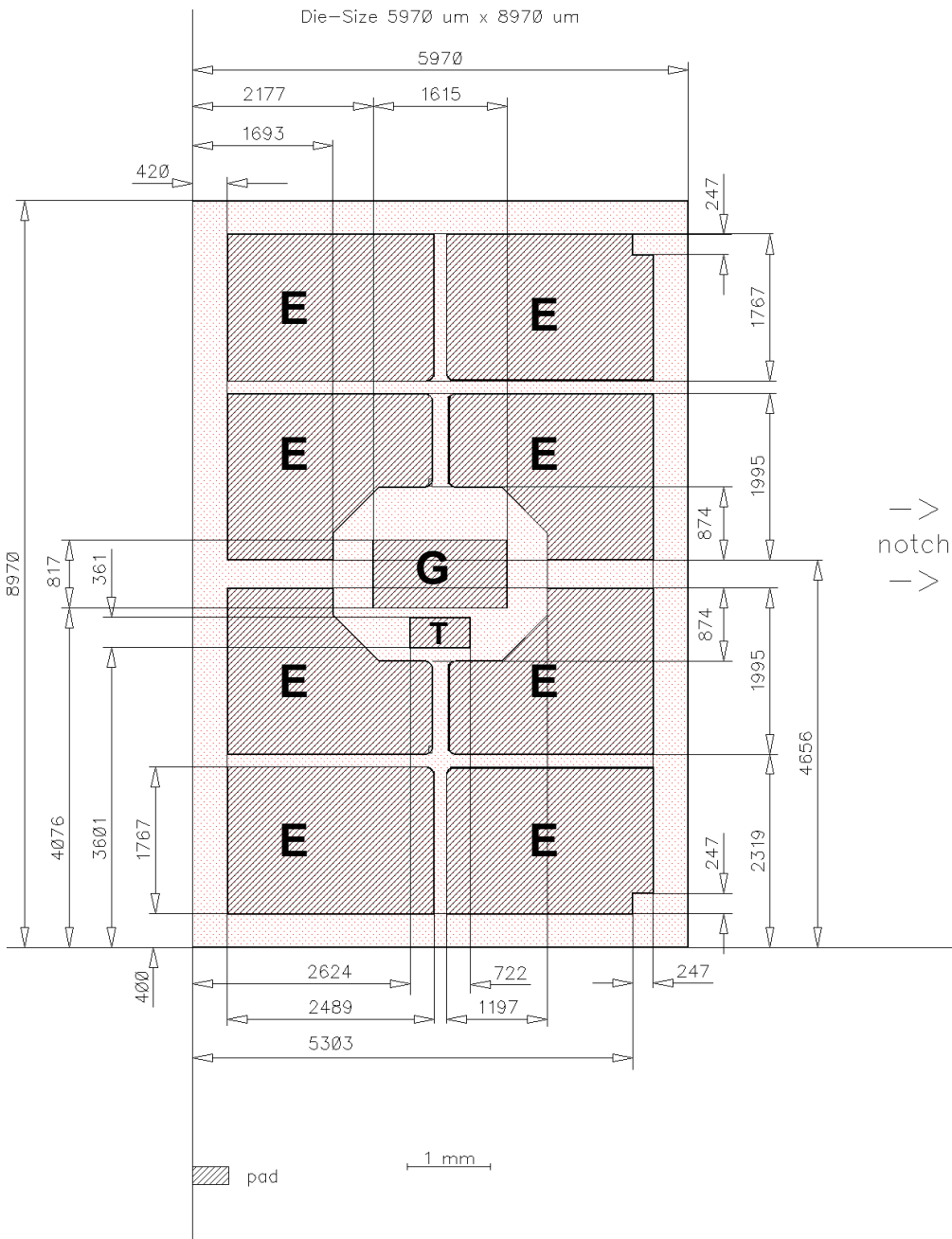
Switching characteristics and thermal properties are depending strongly on module design and mounting technology and can therefore not be specified for a bare die.

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This chip data sheet refers to the device data sheet	FS100R07N2E4	Rev 2.0
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## Chip Drawing



- E** = Emitter
- G** = Gate
- T** = Test pad do not contact



# IGC54T65T8RM

## Description

AQL 0,65 for visual inspection according to failure catalogue

Electrostatic Discharge Sensitive Device according to MIL-STD 883

## Revision History

Version	Subjects (major changes since last revision)	Date

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