International
IOR Rectifier

IRS2548D

SMPS/LED DRIVER PFC + HALF-BRIDGE CONTROL IC

Features

- PFC, system control and half-bridge driver in one IC
- Critical-conduction mode boost-type PFC
- Programmable PFC over-current protection
- Half Bridge Driver
- Half Bridge Over Current Protection
- Variable Frequency Oscillator
- Fixed internal 1.6us HO and LO deadtime
- Internal bootstrap MOSFET
- Internal 15.6V zener clamp diode on Vcc
- Micropower startup (250μA)
- Latch immunity and ESD protection

Typical Applications

- Isolated LED Drivers
- Power Supplies

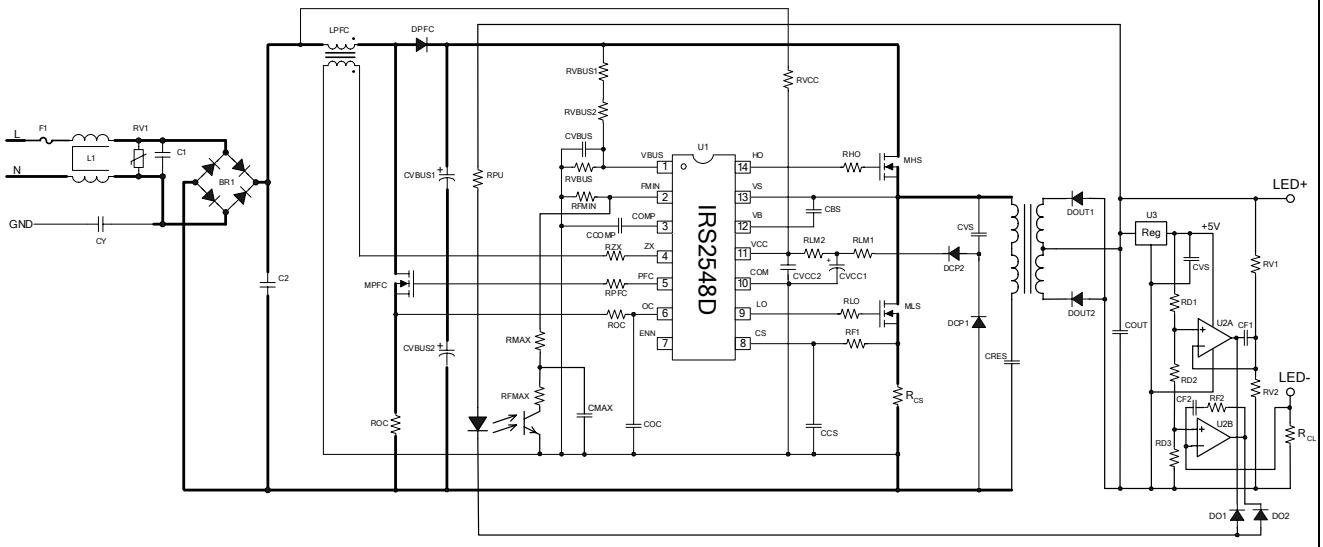
Product Summary

Topology	Half Bridge
V_{OFFSET}	600V
V_{OUT}	VCC
I_{o+} & I_{o-} (typical)	500mA/500mA
t_{ON} & t_{OFF} (typical)	120nS/50nS
Deadtime (typical)	1.6uS

Package

14-Lead SOIC

Typical Connection Diagram



Description

The IRS2548D is a fully integrated, fully protected 600V LED or switched mode power supply control IC with integrated PFC control for a Boost pre-regulator. The IRS2548D is based on the popular IRS2168D electronic ballast control IC re-designed for use in LED driver or half-bridge power supply applications. The PFC circuitry operates in critical conduction mode and provides high PF, low THD and DC bus regulation. The IRS2548D features include programmable minimum run frequency and adjustable oscillator frequency that can be driven by an opto isolator or other feedback circuit in a feedback loop for frequency modulation in resonant systems. The IRS2548D also includes PFC over-voltage and over-current protection, half bridge over current protection and a logic level enable input that can be used for PWM dimming in LED drivers or general burst mode operation.

Qualification Information†

Qualification Level		Industrial††
		Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.
Moisture Sensitivity Level		MSL2††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class A (per JEDEC standard JESD22-A115)
	Human Body Model	Class 1C (per EIA/JEDEC standard EIA/JESD22-A114)
IC Latch-Up Test		Class I, Level A (per JESD78)
RoHS Compliant		Yes

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM, all currents are defined positive into any lead. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V_B	VB Pin High-Side Floating Supply Voltage	-0.3	625	V
V_S	VS Pin High-Side Floating Supply Offset Voltage	V_B – 25	V_B + 0.3	
V_{HO}	HO Pin High-Side Floating Output Voltage	V_S - 0.3	V_B + 0.3	
V_{LO}	LO Pin Low-Side Output Voltage	-0.3	V_{CC} + 0.3	
V_{PFC}	PFC Gate Driver Output Voltage			
I_{OMAX}	Maximum allowable output current (HO, LO, PFC) due to external power transistor miller effect	-500	500	mA
I_{CC}	VCC current †	0	25	mA
V_{VBUS}	VBUS Pin Voltage	-0.3	V_{CC} + 0.3	V
V_{COMP}	COMP Pin Voltage			
V_{OC}	OC Pin Voltage			
V_{ENN}	SD/EOL Pin Voltage			
V_{CS}	CS Pin Voltage			
V_{ZX}	ZX Pin Voltage	-0.3	VZX_{CLAMP} + 0.3	V
I_{FMIN}	FMIN Pin Current	-5	5	mA
I_{COMP}	COMP Pin Current			
I_{ZX}	ZX Pin Current			
I_{OC}	OC Pin Current			
I_{ENN}	ENN Pin Current			
I_{CS}	CS Pin Current			
dV/dt	Allowable VS Pin Offset Voltage Slew Rate	-50	50	V/ns
P_D	Package Power Dissipation @ TA ≤ +25ºC $PD = (T_{JMAX}-T_A)/R_{\theta JA}$	---	1.0	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	---	120	ºC/W
T_J	Junction Temperature	-55	150	ºC
T_S	Storage Temperature	-55	150	
T_L	Lead Temperature (soldering, 10 seconds)	---	300	

† This IC contains a zener clamp structure between the chip V_{CC} and COM, with a nominal breakdown voltage of 15.6 V. Please note that this supply pin should not be driven by a low impedance DC power source greater than V_{CLAMP} specified in the electrical characteristics section.

Recommended Operating Conditions

For proper operation the device should be used within recommended conditions.

Symbol	Definition	Min.	Max.	Units
V_{B-VS}	High Side Floating Supply Voltage	V_{BSUV+}	V_{CLAMP}	V
VS	Steady State High-side Floating Supply Offset Voltage	-1	600	
V_{CC}	Supply Voltage	V_{CCUV+}	V_{CLAMP}	
I_{CC}	V_{CC} Supply Current	††	10	mA
I_{ENN}	ENN Pin Current	-1	1	
I_{CS}	CS Pin Current			
I_{OC}	OC Pin Current			
I_{ZX}	ZX Pin Current			
R_{FMIN}	FMIN Pin Programming Resistor	10	300	KOhm
V_{B-VS}	High Side Floating Supply Voltage	-25	125	ºC

†† Sufficient current should be supplied to V_{CC} to keep the internal 15.6 V zener regulating at V_{CLAMP}.

Electrical Characteristics

V_{CC} = V_{BS} = V_{BIAS}=14V +/- 0.25V, C_{LO} = C_{HO} = C_{PFC} = 1000pF, RFMIN = 42.2kOhm,
V_{ENN} = V_{COMP} = V_{CS} = V_{OC} = V_{BUS} = V_{ZX} = 0V, T_A=25C unless otherwise specified.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Supply Characteristics						
V_{CCUV+}	V_{CC} Supply Undervoltage Positive Going Threshold	11.5	12.5	13.5	V	V_{CC} rising from 0V
V_{CCUV-}	V_{CC} Supply Undervoltage Negative Going Threshold	9.5	10.5	11.5		V_{CC} falling from 14V
V_{UVHYS}	V_{CC} Supply Undervoltage Lockout Hysteresis	1.5	2.0	3.0		
I_{QCCUV}	UVLO Mode V_{CC} Quiescent Current	---	250	---	µA	V_{CC} = 8V
IQCCFLT	V_{CC} Quiescent current in fault mode	---	400	---		MODE=FAULT
I_{CCRUN}	Run Mode V_{CC} Supply Current	---	5.5	---	mA	MODE = RUN VBUS=4V ENN=1nF PFC off time = 5us
V_{CLAMP}	V_{CC} Zener Clamp Voltage	14.6	15.6	16.6	V	I_{CC} = 10mA

Electrical Characteristics (cont'd)

V_{CC} = V_{BS} = V_{BIAS}=14V +/- 0.25V, C_{LO} = C_{HO} = C_{PFC} = 1000pF, R_{FMIN} = 42.2kOhm,
V_{ENN} = V_{COMP} = V_{CS} = V_{OC} = V_{BUS} = V_{ZX} = 0V, T_A=25C unless otherwise specified.

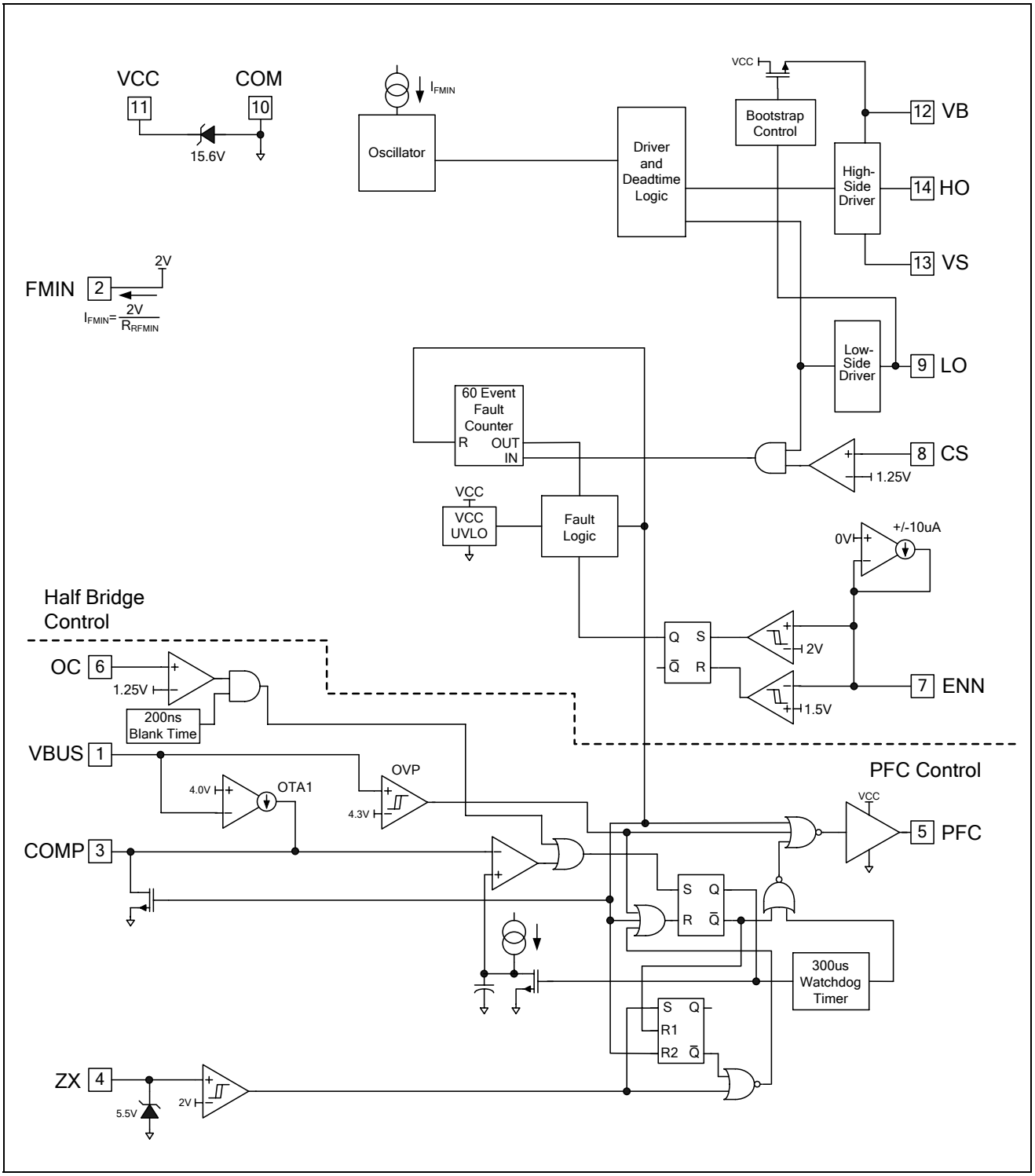
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
Floating Supply Characteristics						
I_{BS}	V_{BS} Supply Current	---	0.9	1.3	mA	MODE=RUN
V_{BSUV+}	V_{BS} Supply Undervoltage Positive Going Threshold	8.0	9.0	10.0	V	V_{BS} rising from 0V
V_{BSUV-}	V_{BS} Supply Undervoltage Negative Going Threshold	7.0	8.0	9.0		V_{BS} falling from 14V
I_{LKVS}	V_S Offset Supply Leakage Current	---	---	50	uA	V_B = V_S = 600V
PFC Error Amplifier Characteristics						
$I_{COMP\ SOURCE}$	COMP Pin OTA Error Amplifier Output Current Sourcing	---	30	---	uA	MODE = RUN V_{VBUS} = 3.5V VCOMP=4.0V
$I_{COMP\ SINK}$	COMP Pin OTA Error Amplifier Output Current Sinking	---	-30	---		MODE = RUN V_{VBUS} = 4.5V VCOMP=4.0V
V_{COMPOH}	OTA Error Amplifier Output Voltage Swing (high state)	---	12.5	---	V	VBUS=3.5V ICOMP=ICOMP_SOURCE - 5uA
V_{COMPOL}	OTA Error Amplifier Output Voltage Swing (low state)	---	0.4	---		VBUS=5.0V ICOMP=ICOMP_SINK + 5uA
$V_{COMPFLT}$	OTA Error Amplifier Output Voltage in Fault Mode	---	0	---		VBUS=4.0V
PFC Control Characteristics						
$V_{VBUS\ REG}$	VBUS Internal Reference Voltage	3.93	4.03	4.13	V	V_{COMP} = 4.0V
V_{VBUSOV}	VBUS Over-voltage Comparator Threshold	4.1	4.3	4.5		
$V_{VBUSOV\ HYS}$	VBUS Over-voltage Comparator Hysteresis	50	150	300	mV	
V_{ZX}	ZX Pin Threshold Voltage	1.8	2.0	2.2	V	
V_{ZXhys}	ZX pin Comparator Hysteresis	---	300	---	mV	
$V_{ZXclamp}$	ZX pin Clamp Voltage (high state)	---	6.7	---	V	I_{ZX} = 1mA
tBLANK	OC pin current-sensing blank time	---	300	---	ns	VBUS=4.0V VCOMP=4.0V
tWD	PFC Watch-dog Pulse Interval	---	400	---	us	ZX = 0, V_{COMP} = 4.0V
PFC Protection Circuitry Characteristics						
V_{OCTH+}	OC Pin Over-current Sense Threshold	1.1	1.2	1.3		VBUS=VCOMP =4.0V

Electrical Characteristics (cont'd)

VCC = VBS = VBIAS=14V +/- 0.25V, CLO = CHO = CPFC = 1000pF, RFMIN = 42.2kOhm,
VENN = VCOMP = VCS = VOC = VBUS = VZX = 0V, TA=25C unless otherwise specified.

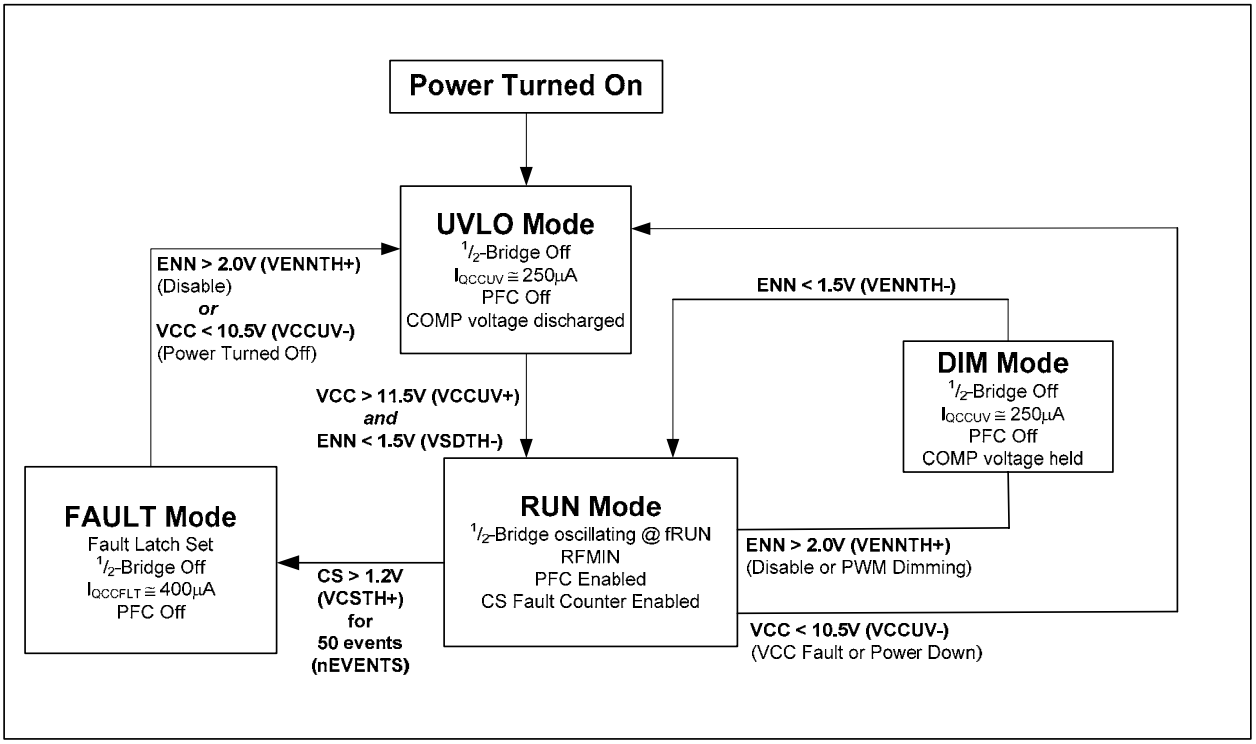
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
System Control Oscillator Characteristics						
fOSCRUN	Half-bridge Oscillator Run Frequency	42.5	44.5	46.5	kHz	MODE = RUN
d	Oscillator duty cycle	---	50	---		
tdLO	LO Output Deadtime	---	1.6	---	us	
tdHO	HO Output Deadtime	---	1.6	---		
VFMIN	FMIN Pin Voltage	1.9	2.0	2.1	V	VCC = 14.0V
VFMINFLT	FMIN Pin Fault or UVLO Mode Voltage	---	0	---		MODE = FAULT or UVLO
System Control Protection Circuitry Characteristics						
VCSTH+	CS Pin Over-current Sense Threshold	1.15	1.25	1.35	V	
nEVENTS	CS Pin Fault Counter No. of Events		65			MODE = RUN
VENNTH+	SD Pin Rising Non-latched Shutdown Threshold Voltage	---	2.0	---	V	
VENNTH-	SD Pin Falling Reset Threshold Voltage	---	1.5	---		
VENNBIAS	EOL Pin Internal Bias Voltage	---	0V	---	V	
VFMINFLT	FMIN Pin Fault Mode Voltage	---	0	---	V	MODE = FAULT
Gate Driver Output Characteristics (HO, LO and PFC pins)						
VOL	Low-Level Output Voltage	---	0	100	mV	IO = 0
VOH	High-Level Output Voltage	---	0	100		VBIAS - VO , IO = 0
t_r	Turn-On Rise Time	---	120	---	nsec	
t_f	Turn-Off Fall Time	---	50	---		
I0+	Source Current	---	180	---	mA	
I0-	Sink Current	---	260	---		
Bootstrap FET Characteristics						
VB_ON	VB when the bootstrap FET is on	---	13.7	---	V	
IB_CAP	VB source current when FET is on	35	55	---	mA	CBS=0.1uF
IB_10V	VB source current when FET is on	8	12	---		VB=10V

Functional Block Diagram



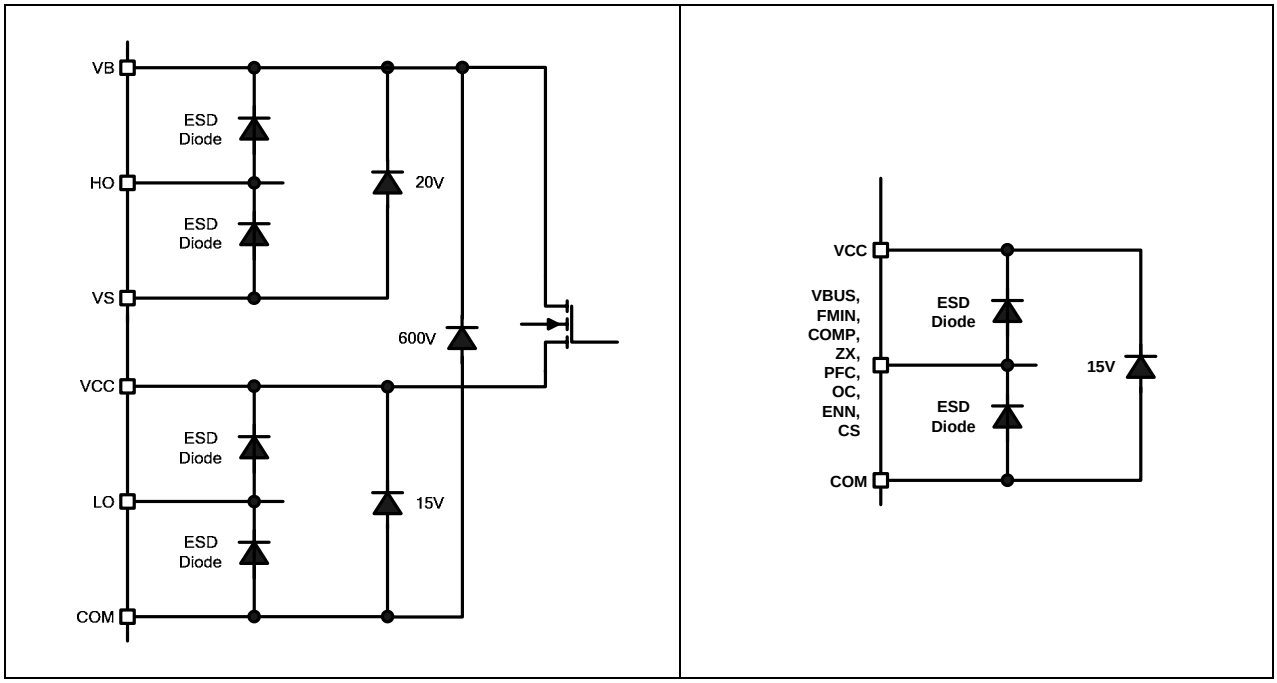
Values in block diagram are typical values

State Diagram



All values are typical.
Please refer to application diagram on page 1.

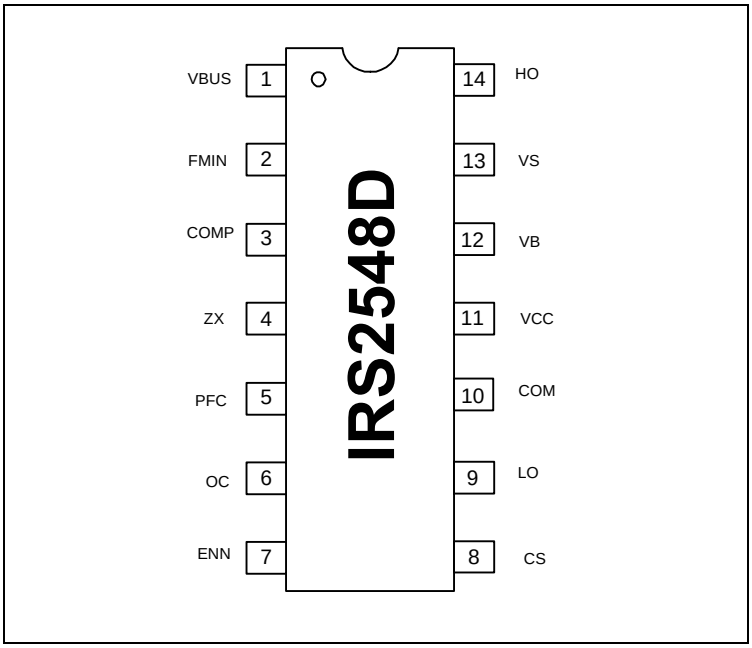
Input/Output Pin Equivalent Circuit Diagrams



Lead Definitions

Symbol	Description
VBUS	DC Bus Sensing Input
FMIN	Oscillator Minimum Frequency Setting
COMP	PFC Error Amplifier Compensation
ZX	PFC Zero-Crossing Detection
PFC	PFC Gate Driver Output
OC	PFC Current Sensing Input
ENN	Enable / PWM Dimming Input
CS	Half-Bridge Current Sensing Input
LO	Low-Side Gate Driver Output
COM	IC Power & Signal Ground
VCC	Logic & Low-Side Gate Driver Supply
VB	High-Side Gate Driver Floating Supply
VS	High Voltage Floating Return
HO	High-Side Gate Driver Output

Lead Assignments



Application Information and Additional Details

I. LED Driver Section
Functional Description

Under-voltage Lock-Out Mode (UVLO)

The under-voltage lock-out mode (UVLO) is defined as the state the IC is in when VCC is below the turn-on threshold of the IC. The IRS2548D undervoltage lock-out is designed to maintain an ultra low supply current and to guarantee the IC is fully functional before the high and low-side output drivers and PFC are activated. Figure 1 shows a possible VCC supply voltage scheme using the micro-power start-up current of the IRS2548D together with a snubber charge pump from the half-bridge output (R_{VCC}, C_{VCC1}, C_{VCC2}, C_{SNUB}, D_{CP1} and D_{CP2}).

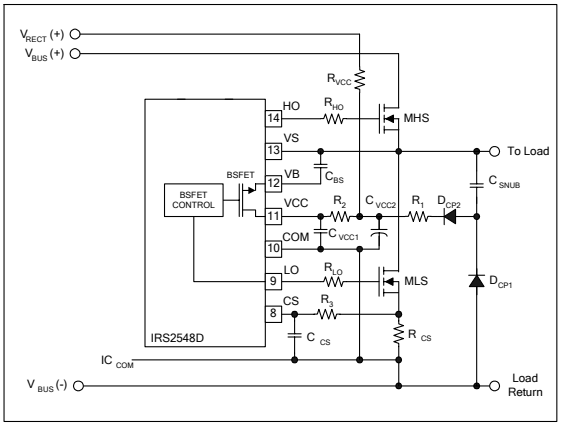


Figure 1: Start-up and supply circuitry.

The VCC capacitors (C_{VCC1} and C_{VCC2}) are charged by the current through supply resistor (R_{VCC}) minus the start-up current drawn by the IC. This resistor is chosen to set the desired AC line input voltage turn-on threshold for the system. When the voltage at VCC exceeds the IC start-up threshold (VCCUV+) and the ENN pin is below 1.5 volts, the IC turns on and LO begins to oscillate. The capacitors at VCC begin to discharge due to the increase in IC operating current (Figure 2). The high-side supply voltage, VB-VS, begins to increase as capacitor C_{BS} is charged through the internal bootstrap MOSFET during the LO on-time of each LO switching cycle. When the VB-VS voltage exceeds the high-side start-up threshold (VBSUV+), HO then begins to oscillate. This may take several cycles of LO to charge VB-VS above VBSUV+ due to RDSon of the internal bootstrap MOSFET.

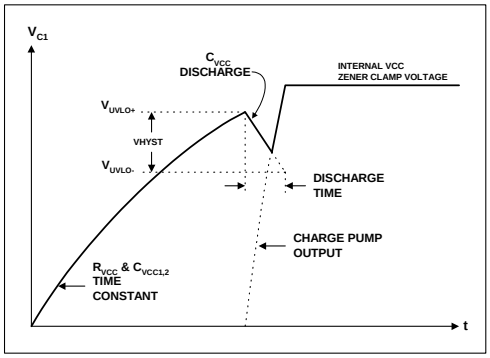


Figure 2: VCC supply voltage.

When LO and HO are both oscillating, the external MOSFETs (MHS and MLS) are turned on and off with a 50% duty cycle and a non-overlapping deadtime of 1.6us. The half-bridge output (pin VS) begins to switch between the DC bus voltage and COM. During the deadtime between the turn-off of LO and the turn-on of HO, the half-bridge output voltage transitions from COM to the DC bus voltage at a dv/dt rate determined by the snubber capacitor (C_{SNUB}). As the snubber capacitor charges, current will flow through the charge pump diode (D_{CP2}) to VCC. After several switching cycles of the half-bridge output, the charge pump and the internal 15.6V zener clamp of the IC take over as the supply voltage. Capacitor C_{VCC2} supplies the IC current during the VCC discharge time and should be large enough such that VCC does not decrease below UVLO- before the charge pump takes over.

This scheme can be used in non-dimming applications, however where PWM dimming is used the charge pump may not supply enough current to VCC at low dimming levels and in this case an auxiliary power supply is required.

Capacitor C_{VCC1} is required for noise filtering and must be placed as close as possible and directly between VCC and COM, and should not be lower than 0.1uF. Resistors R_1 and R_2 are recommended for limiting high currents that can flow to VCC from the charge pump. The internal bootstrap MOSFET and supply capacitor (C_{BS}) provide the floating supply voltage for the high side driver circuitry. During UVLO mode the high and low-side driver outputs HO and LO are both low and the internal oscillator is disabled.

Run Mode (RUN)

After the VCC supply comes up and the IC starts, the IC enters run mode. The operating frequency is set to the minimum limit, which is programmed by the external resistor (RFMIN) at the FMIN pin. If the IRS2548D is used in a series resonant configuration the frequency can be increased to regulate the system output voltage. This can be implemented by sinking additional current from the FMIN pin with an additional resistor, opto isolator or other arrangement.
It should be noted that the FMIN pin input is very sensitive to noise and that traces connected to this pin should be very short and should be kept away from high voltage switching nodes; HO, VB and VS. An additional RC filter can also be added to the FMIN pin if necessary as shown in the application schematic on page 1.
Should hard-switching occur at the half-bridge at any time or excessive current be drawn due to a fault condition, the voltage across the current sensing resistor (RCS) will exceed the internal threshold of 1.2 volts (VCSTH+) and the fault counter will begin counting (see Figure 3).

CS Fault Mode

The current sense function will force the IC to enter fault mode only after the voltage at the CS pin has been greater than 1.2V (VCSTH+) for 65 (nEVENTS) consecutive cycles of LO. The voltage at the CS pin is AND-ed with LO (see Figure 3) so it will work with pulses that occur during the LO on-time or DC. If the over-current faults are not consecutive, then the internal fault counter will count back down each cycle when there is no fault. Should an over-current fault occur only for a few cycles and then not occur again, the counter will eventually reset to zero.

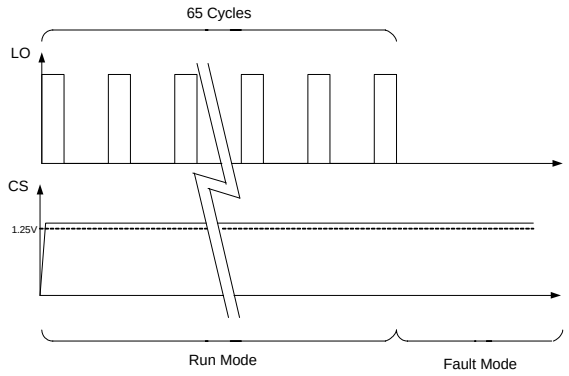


Figure 3: Fault counter timing diagram.

DIM Mode (ENN Input)

PWM dimming can be implemented via the ENN pin. If the voltage input to the ENN pin exceeds 2V during run mode, the IC enters dim mode, LO, HO and PFC gate drivers go to the low state. This is similar to fault mode except that the COMP pin is not internally pulled to COM and so the COMP capacitor retains it's voltage. This allows the PFC to start up rapidly with the on time close to where it was before the ENN signal shut off the IC outputs. When ENN goes below 1.5V and therefore the bus voltage can be maintained while the PFC gate drive being held low during the periods where the LED load is not being driven. This minimizes ripple generated on the DC bus during PWM dimming.

II. PFC Section
Functional Description

In most LED drivers rated at more than a few Watts high power factor high power factor (PC) is a requirement. The driver needs to appear as a resistive load to the AC input line voltage. The degree to which the circuit matches a purely resistive load is measured by the phase shift between the input voltage and input current harmonic distortion of the input current waveform. The cosine of the phase angle between the input voltage and input current is defined as the *displacement power factor* and the amount of harmonic distortion determines the *distortion power factor* and total harmonic distortion (THD). The overall power factor is the ratio between real and apparent power and includes both displacement and distortion. A power factor of 1.0 corresponds to zero phase shift and a THD of 0% representing a pure sinusoidal current waveform. In order to provide a high PF and a low THD the IRS2548D includes an active power factor correction (PFC) circuit.

The control method implemented in the IRS2548D is designed for a PFC Boost converter (Figure 4) running in *critical-conduction mode*, the boundary between continuous and discontinuous mode. During the off period of each switching cycle of the PFC MOSFET the circuit waits until the inductor current falls to zero before turning the PFC MOSFET on again. The PFC MOSFET is turned on and off at a much higher frequency (>10KHz) than the line input frequency (50 to 60Hz).

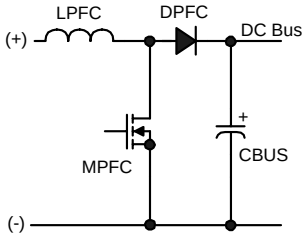


Figure 4: Boost converter circuit.

When the switch MPFC is turned on the inductor LPFC is connected between the rectified line input (+) and (-) causing the current in LPFC to rise linearly. When MPFC is turned off LPFC is connected between the rectified line input (+) and the DC bus capacitor CBUS through diode DPFC and the stored energy in LPFC supplies a current into CBUS. MPFC is turned on and off at a high frequency and the voltage on CBUS charges up to a specified voltage. The feedback loop of the IRS2548D regulates this voltage to a fixed value by continuously monitoring the DC bus voltage and adjusting the on-time of MPFC accordingly. For an increasing DC bus the on-time is decreased and for a decreasing DC bus the on-time is increased. This negative feedback control is performed with a slow loop speed such that the average inductor current smoothly follows the low-frequency line input voltage for high power factor and low THD. The on-time of MPFC therefore appears to be fixed (except for on time modulation which is discussed later) over several cycles of the line voltage. With a fixed on-time and an off-time determined by the inductor current discharging to zero the switching frequency and duty cycle vary to produce a high frequency near the zero crossing of the AC input line voltage and a lower frequency at the peak (Figure 5).

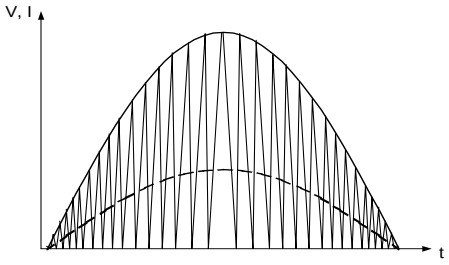


Figure 5: Sinusoidal line input voltage (solid line), triangular PFC Inductor current and smoothed sinusoidal line input current (dashed line) over one half-cycle of the AC line input voltage.

When the line input voltage is low (near the zero crossing), the inductor current will charge to a lower peak level and therefore the discharge time will be fast resulting in a high switching frequency. When the input line voltage is high (near the peak), the inductor current will charge up to a higher amount and the discharge time will be longer giving a lower switching frequency.

The PFC control circuit of the IRS2548D (Figure 6) includes five control pins: VBUS, COMP, ZX, PFC and OC. The VBUS pin measures the DC bus voltage via an external resistor voltage divider. The COMP pin voltage at the transconductance error amplifier output sets the on-time of MPFC where the speed of the feedback loop is determined by the external COMP capacitor. The ZX input detects when the inductor current has discharged to zero each switching cycle using a secondary winding from the PFC inductor. The PFC output provides the gate driver output for the external MOSFET, MPFC. The OC pin senses the current flowing through MPFC and performs cycle-by-cycle over-current protection.

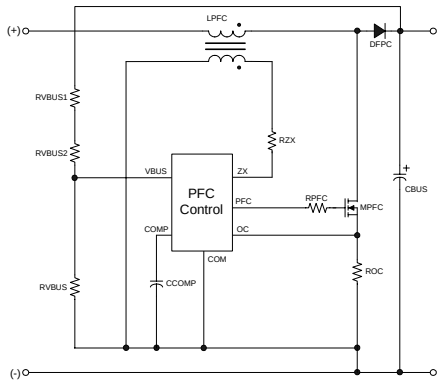


Figure 6: IRS2548D simplified PFC control circuit.

The VBUS pin is regulated against a fixed internal 4V reference voltage for regulating the DC bus voltage (Figure 7). The feedback loop is performed by an operational transconductance amplifier (OTA) that sinks or sources a current to the external capacitor at the COMP pin. The resulting voltage on the COMP pin sets the threshold for the charging of the internal timing capacitor and therefore determines the on-time of MPFC.

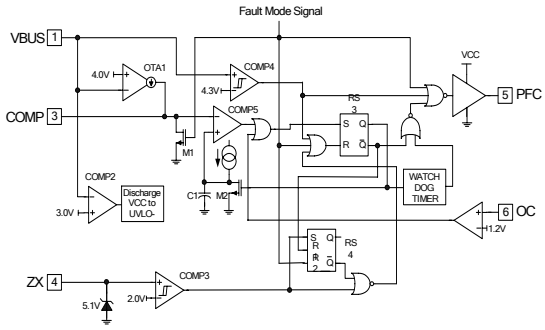


Figure 7: IRS2548D detailed PFC control circuit.

The off-time of MPFC is determined by the time it takes the LPFC current to fall to zero. A positive-going edge at the ZX input exceeding the internal 2V threshold (VZXTH+) signals the beginning of the off-time and the following negative-going edge falling below 1.7V (VZXTH+ - VZXHYS) occurs when the LPFC current discharges to zero which signals the end of the off-time and MPFC is turned on again (Figure 8). The cycle repeats itself indefinitely until the PFC section is disabled due to a fault detected by the system section (Fault Mode), an over-voltage on the DC bus or the negative transition of ZX pin voltage does not occur. Should the negative edge at ZX not be detected, MPFC will remain off until the watch-dog timer forces it to turn-on again after a fixed delay.

Should the OC pin exceed the 1.2V (VOCTH+) over-current threshold during the on-time, the PFC output will turn off. The circuit will then wait for a negative-going transition on the ZX pin or a forced turn-on from the watch-dog timer to turn the PFC output on again.

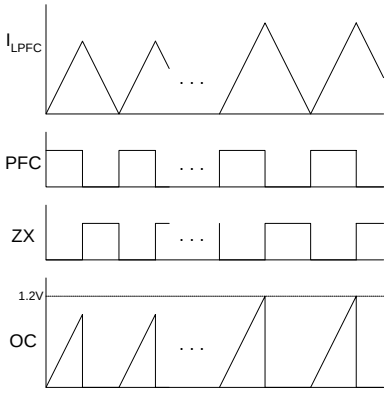


Figure 8: Inductor current, PFC pin, ZX pin and OC pin timing diagram.

On-time Modulation Circuit

A fixed on-time of MPFC over an entire cycle of the line input voltage produces a peak inductor current which naturally follows the sinusoidal shape of the line input voltage. The smoothed averaged line input current is in phase with the line input voltage for high power factor but some harmonic distortion is left. This is mostly due to cross-over distortion of the line current near the zero-crossings of the line input voltage. To achieve lower harmonics that comply with international standards such as EN61000-3-2 class C and general market requirements an additional on-time modulation circuit in included in the PFC control. This circuit dynamically increases the on-time of MPFC as the line input voltage nears the zero-crossings (Figure 9). This causes the peak LPFC current and therefore the smoothed line input current to increase slightly near the zero-crossings of the line input voltage to compensate for cross over distortion which reduces the THD and higher harmonics.

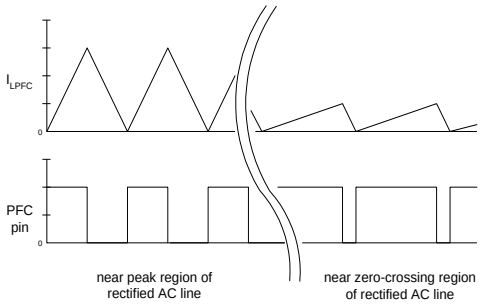


Figure 9: On-time modulation circuit timing diagram

DC Bus Over-voltage Protection

Should over-voltage occur on the DC bus and the VBUS pin exceeds the internal 4.3V threshold (VBUSOV+), the PFC output is disabled (set to a logic 'low'). When the DC bus decreases again and the VBUS pin decreases below the internal 4.15V threshold (VBUSOV-), a watch-dog pulse is forced on the PFC pin and normal PFC operation is resumed.

III. Design Equations (Half-Bridge)

Note: The results from the following design equations can differ slightly from actual measurements due to IC tolerances, component tolerances, and oscillator over- and under-shoot due to internal comparator response time.

Step 1: Program Run Frequency

The run frequency is programmed with the timing resistor RFMIN at the FMIN pin.
The graph in Figure 10 (RFMIN vs. Frequency) can be used to select RFMIN value for desired run frequency.

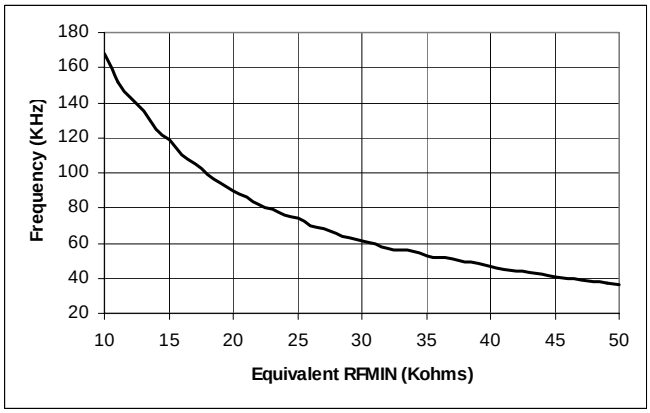


Figure 10: Graph of frequency against RFMIN

Step 2: Program Maximum Current

The maximum current is programmed with the external resistor RCS and an internal threshold of 1.25V (VCSTH+). This threshold determines the over-current limit of the system:

$$I_{MAX} = \frac{1.25}{R_{CS}} \qquad \text{[Amps Peak]}$$

or

$$R_{CS} = \frac{1.25}{I_{MAX}} \qquad \text{[Ohms]}$$

IV. PFC Design Equations

Step1: Calculate PFC inductor value:

$$L_{PFC} = \frac{(VBUS - \sqrt{2} \cdot VAC_{MIN}) \cdot VAC_{MIN}^2 \cdot \eta}{2 \cdot f_{MIN} \cdot P_{OUT} \cdot VBUS}$$ [Henries]

where,

$VBUS$ = DC bus voltage
VAC_{MIN} = Minimum rms AC input voltage
η = PFC efficiency (typically 0.95)
f_{MIN} = Minimum PFC switching frequency at minimum AC input voltage
P_{OUT} = System output power

Step 2: Calculate peak PFC inductor current:

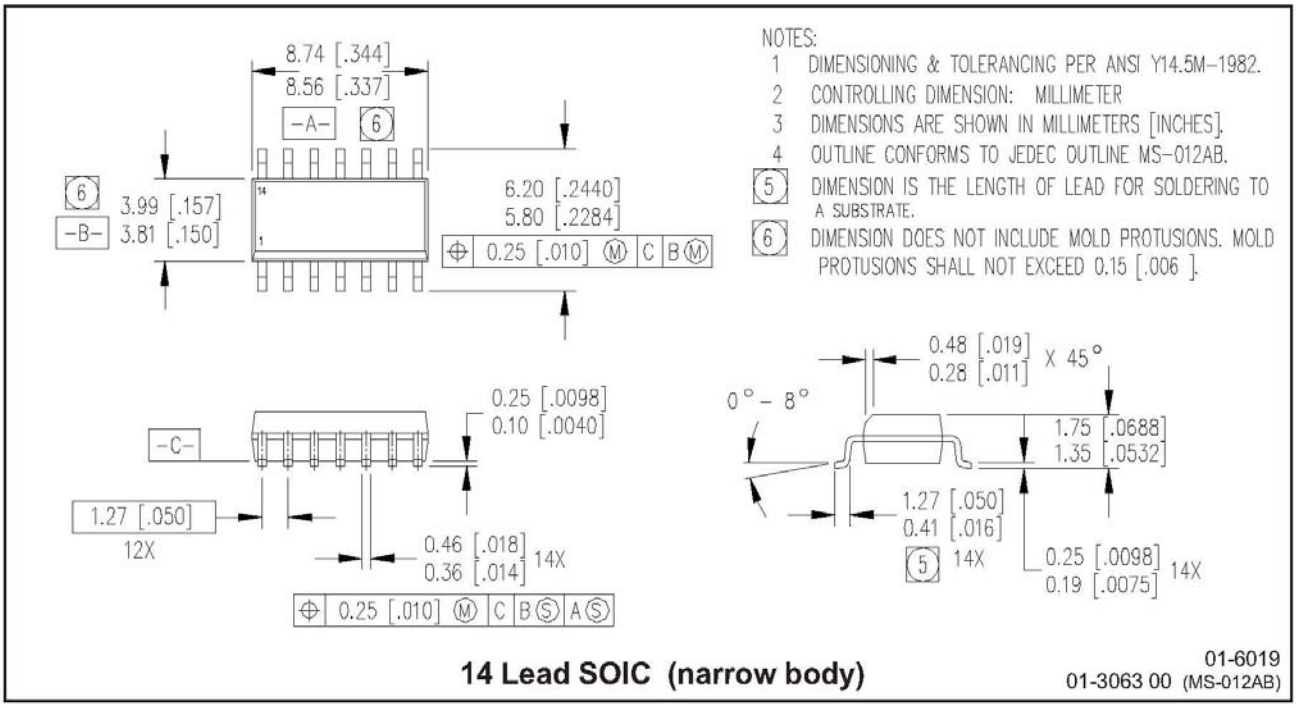
$$i_{PK} = \frac{2 \cdot \sqrt{2} \cdot P_{OUT}}{VAC_{MIN} \cdot \eta}$$ [Amps Peak]

Note: The PFC inductor must not saturate at i_{PK} over the specified system operating temperature range. Proper core sizing and air-gapping should be considered in the inductor design.

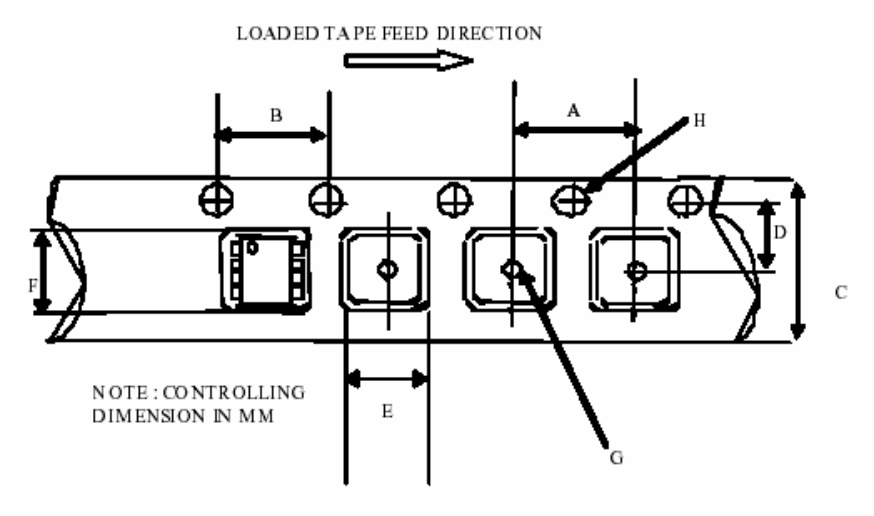
Step 3: Calculate PFC over-current resistor ROC value:

$$R_{OC} = \frac{1.25}{i_{PK}}$$ where VCSTH+ = 1.25V [Ohms]

Package Details

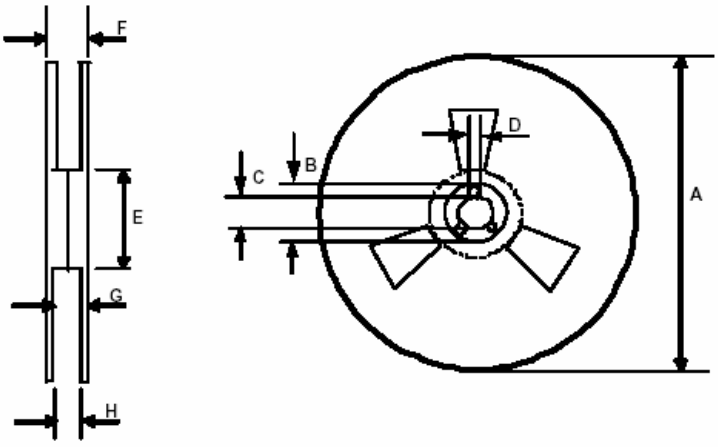


Tape and Reel Details



CARRIER TAPE DIMENSION FOR 14SOICN

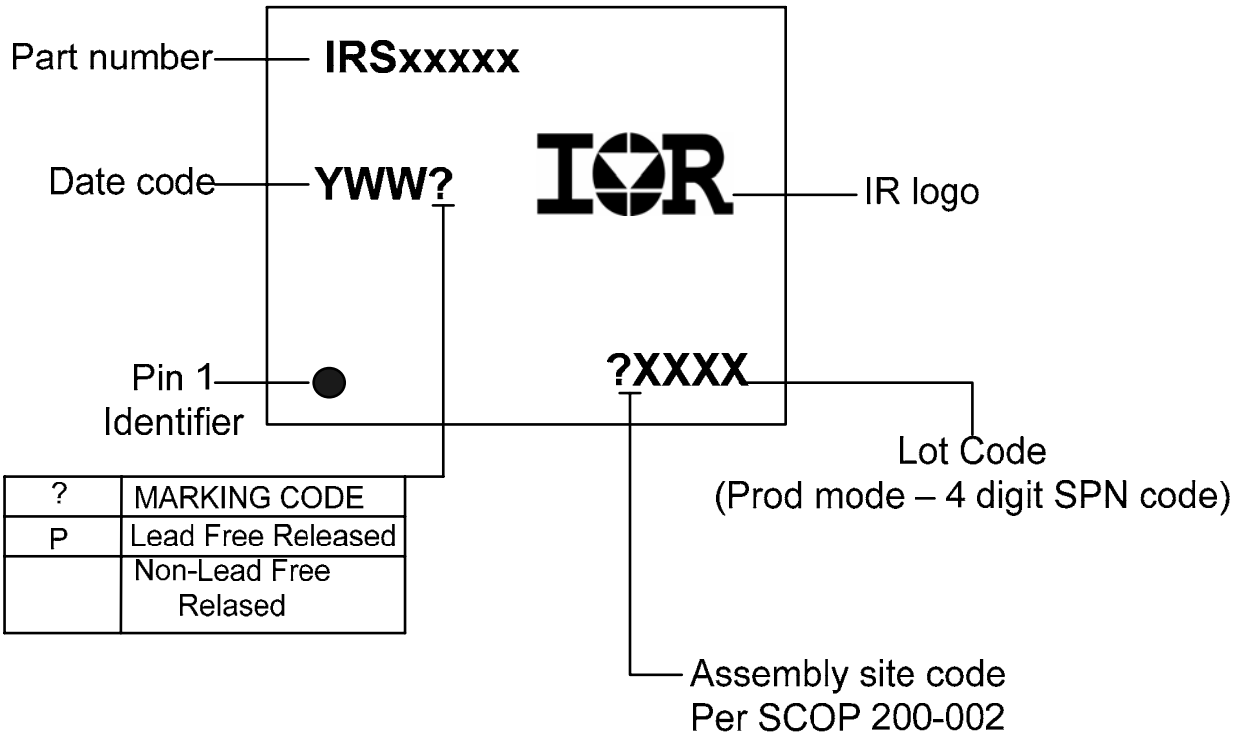
	Metric		Imperial	
Code	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	6.40	6.60	0.252	0.260
F	9.40	9.60	0.370	0.378
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 14SOICN

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



?	MARKING CODE
P	Lead Free Released
	Non-Lead Free Relased

Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
IRS2548D	SOIC14N	Tube/Bulk	55	IRS2548DSPBF
		Tape and Reel	2500	IRS2548DSTRPBF

For technical support, please contact IR's Technical Assistance Center
http://www.irf.com/technical-info/

WORLD HEADQUARTERS:
233 Kansas St., El Segundo, California 90245
Tel: (310) 252-7105

单击下面可查看定价，库存，交付和生命周期等信息

>>Infineon Technologies(英飞凌)