TVS Diodes

Transient Voltage Suppressor Diodes

ESD105-B1-02 Series

Low Capacitance & Low Clamping Bi-directional ESD / Transient Protection Diodes

ESD105-B1-02ELS
ESD105-B1-02EL

Data Sheet

Revision 1.0, 2013-12-12
Final

Power Management & Multimarket

Revision History: Rev. 04, 2013-09-24	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.0, 2013-12-12	
All	Status change to Final

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Last Trademarks Update 2010-06-09

1 Low Capacitance & Low Clamping Bi-directional ESD / Transient Protection Diodes

1.1 Features

- ESD / Transient protection of signal lines exceeding standard:
  - **IEC61000-4-2 (ESD): ±30 kV air / ±25 kV contact discharge**
  - **IEC61000-4-4 (EFT): ±50 A (5/50 ns)**
  - **IEC61000-4-5 (Surge): ±5 A (8/20 µs)**
- One-line diode with ultra-small form factor down to 0.62 x 0.32 x 0.31 mm² (0201) package size
- Bi-directional, symmetrical working voltage up to: V_{RWM} **= ±5.5 V**
- Low capacitance C_L **= 0.3 pF** (typical)
- Very low clamping voltage, low dynamic resistance: R_{DYN} **= 0.36** Ω (typ.)
- Pb-free package (RoHS compliant) and halogen free package

1.2 Application Examples

- USB 3.0. 10/100/1000 Ethernet, Firewire, DVI, HDMI, S-ATA, Display Ports
- Mobile HDMI Link, MDDI, MIPI, SWP, NFC

1.3 Product Description

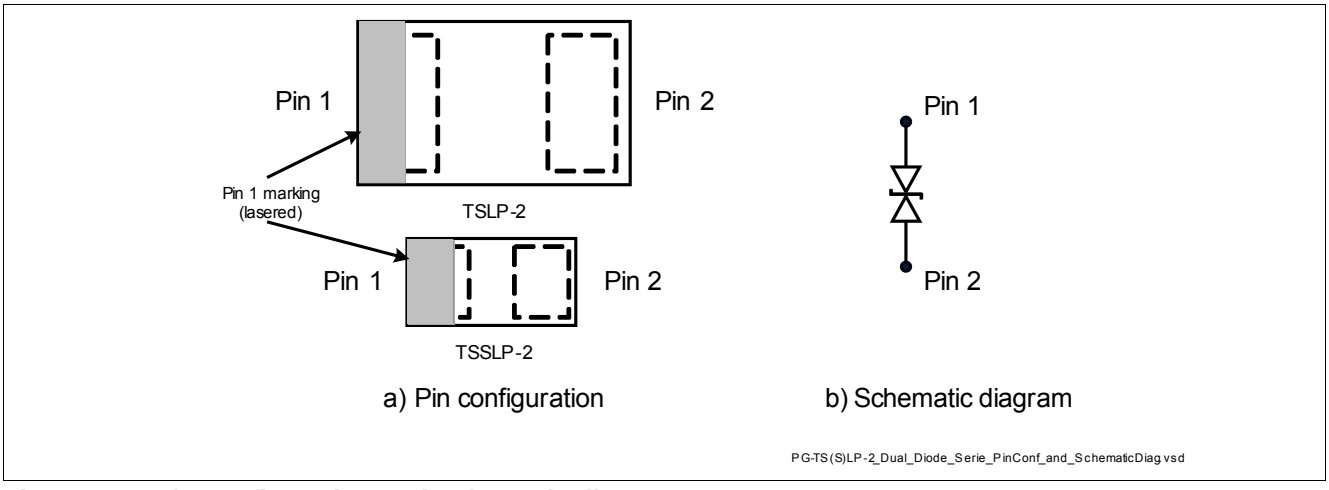

Figure 1 Pin configuration and Schematic diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD105-B1-02ELS	TSSLP-2-4	1 line, bi-directional	N
ESD105-B1-02EL	TSLP-2-20	1 line, bi-directional	N

2 Characteristics

Table 2 Maximum Ratings at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD[2)] air discharge contact discharge	V_{ESD}	 – –	 – –	 30 25	kV
Peak pulse current (t_p = 8 / 20 µs)[3)]	I_{PP}	–	–	5	A
Peak pulse power[3)] t_p = 8 / 20 µs	P_{PK}	 –	 –	 70	W
Operating temperature	T_{OP}	-55	–	125	°C
Storage temperature	T_{stg}	-65	–	150	°C

1) Device is electrically symmetrical
2) V_{ESD} according to IEC61000-4-2
3) I_{PP} according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

2.1 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

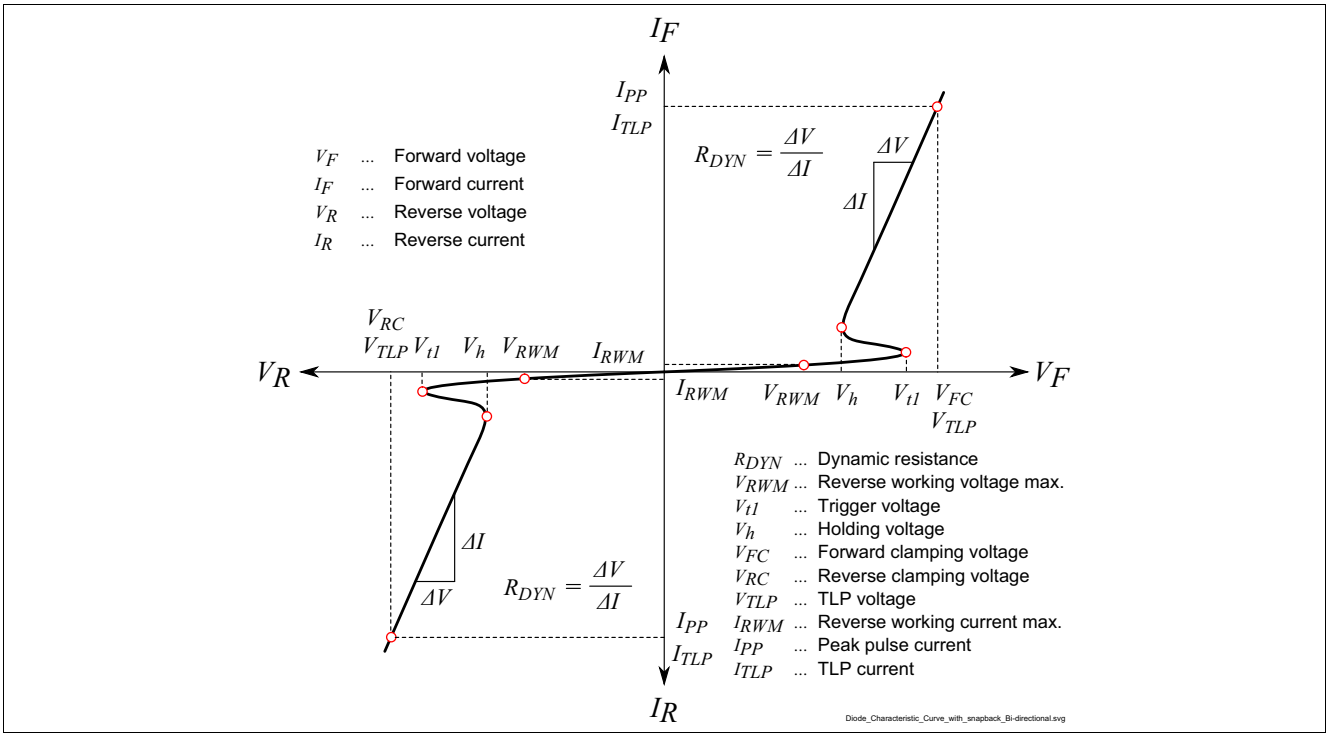

Figure 2 Definitions of electrical characteristics

Table 3 DC Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	5.5	V	
Reverse current	I_R	–	<1	20	nA	V_R = 5.5 V
Trigger voltage	V_{t1}	6.1	–	–	V	
Holding voltage	V_h	6.1	8	–	V	I_R = 1 mA

1) Device is electrically symmetrical

Table 4 AC Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.3	0.45	pF	V_R = 0 V, f = 1 MHz
		–	0.3	0.45		V_R = 0 V, f = 1 GHz

Table 5 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage [2)]	V_{CL}	–	13	16	V	I_{TLP} = 16 A, t_p = 100 ns
		–	19	22		I_{TLP} = 30 A, t_p = 100 ns
Clamping voltage[3)]		–	8.5	11.5		I_{PP} = 2 A, t_p = 8/20 µs
		–	11	14		I_{PP} = 5 A, t_p = 8/20 µs
Dynamic resistance[2)]	R_{DYN}	–	0.36	0.45	Ω	t_p = 100 ns

1) Device is electrically symmetrical

2) Please refer to Application Note AN210 [1]. TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 300ps, averaging window: t_1 = 30 ns to t_2 = 60 ns, extraction of dynamic resistance using least squares fit of TLP characteristics between I_{TLP1} = 10 A and I_{TLP2} = 50 A.

3) I_{PP} according to IEC61000-4-5 (t_p = 8/20 µs)

3 Typical Characteristics at T_A = 25 °C, unless otherwise specified

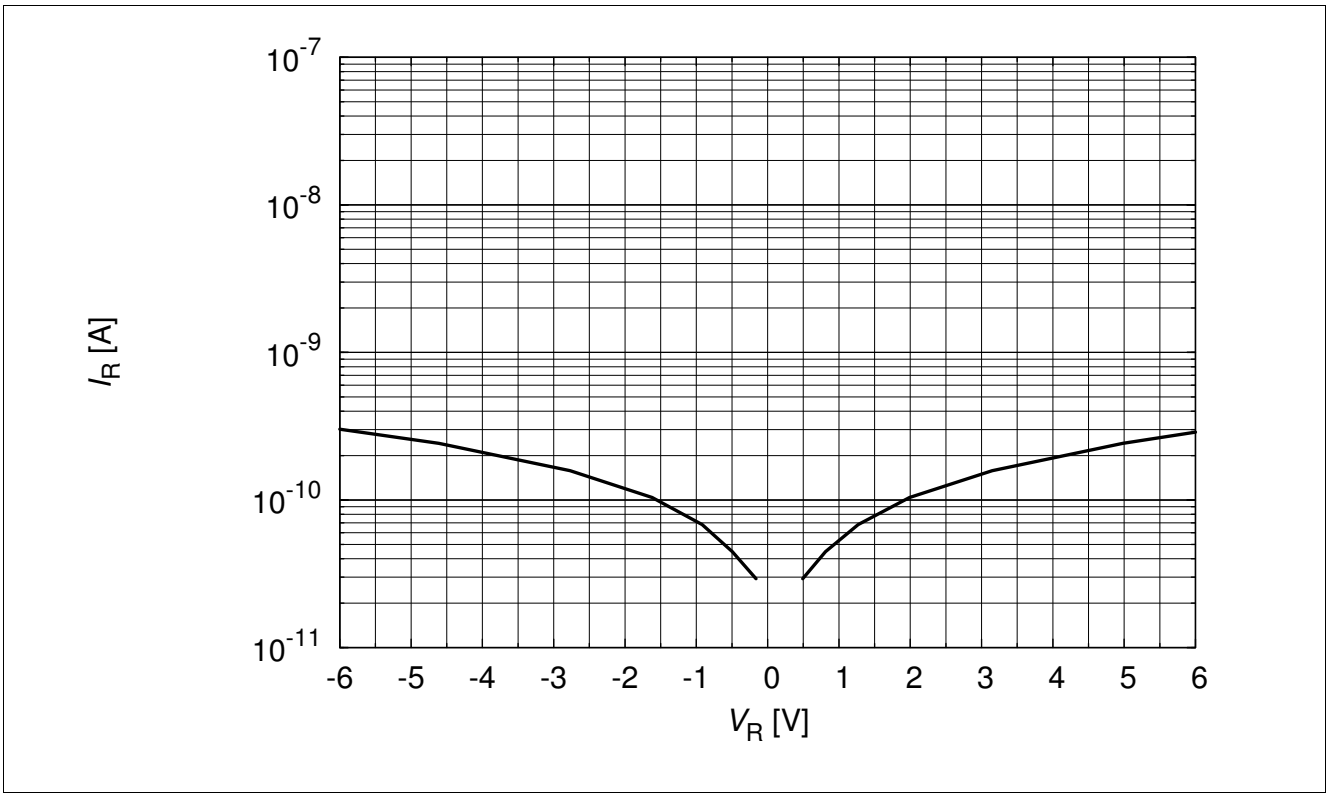

Figure 3 Reverse current: $I_R = f(V_R)$

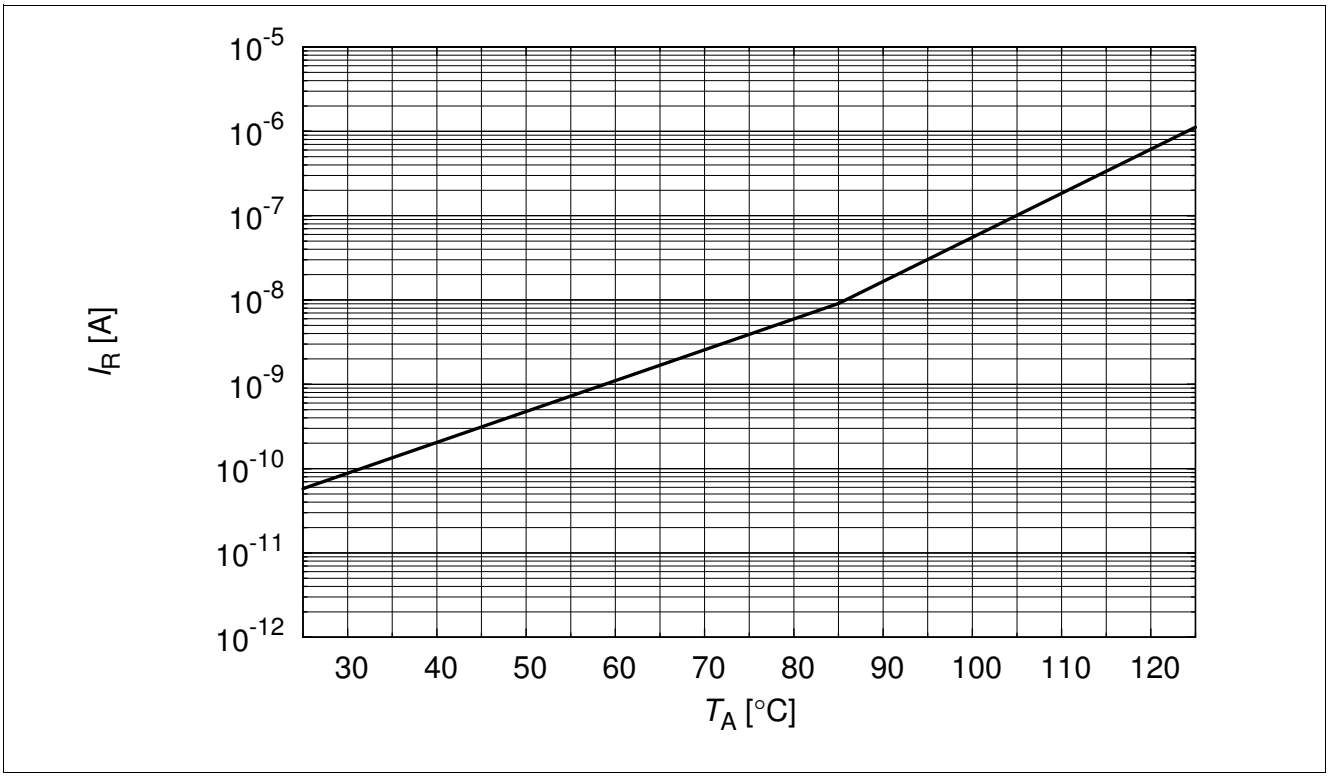

Figure 4 Reverse current: $I_R = f(T_A)$, V_R = 5.5 V

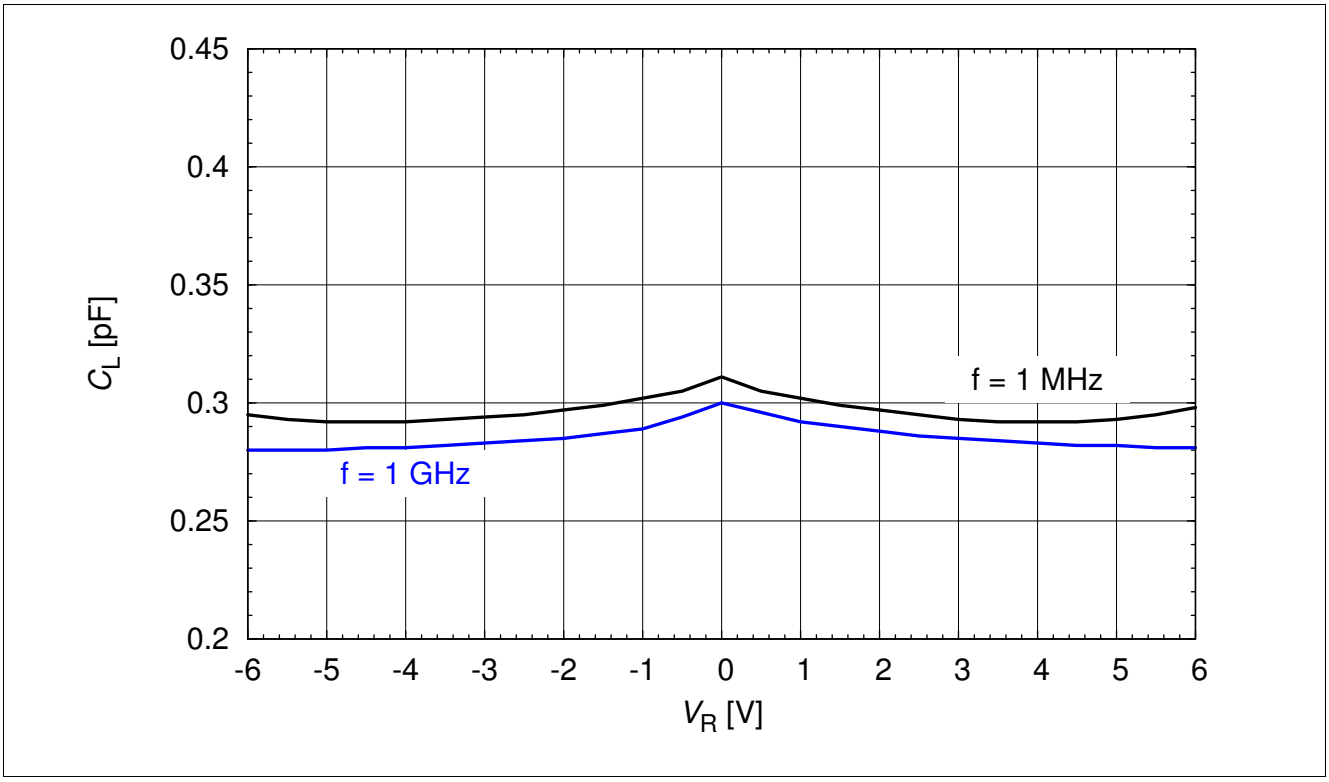

Figure 5 **Line capacitance: $C_L = f(V_R)$, f = 1MHz**

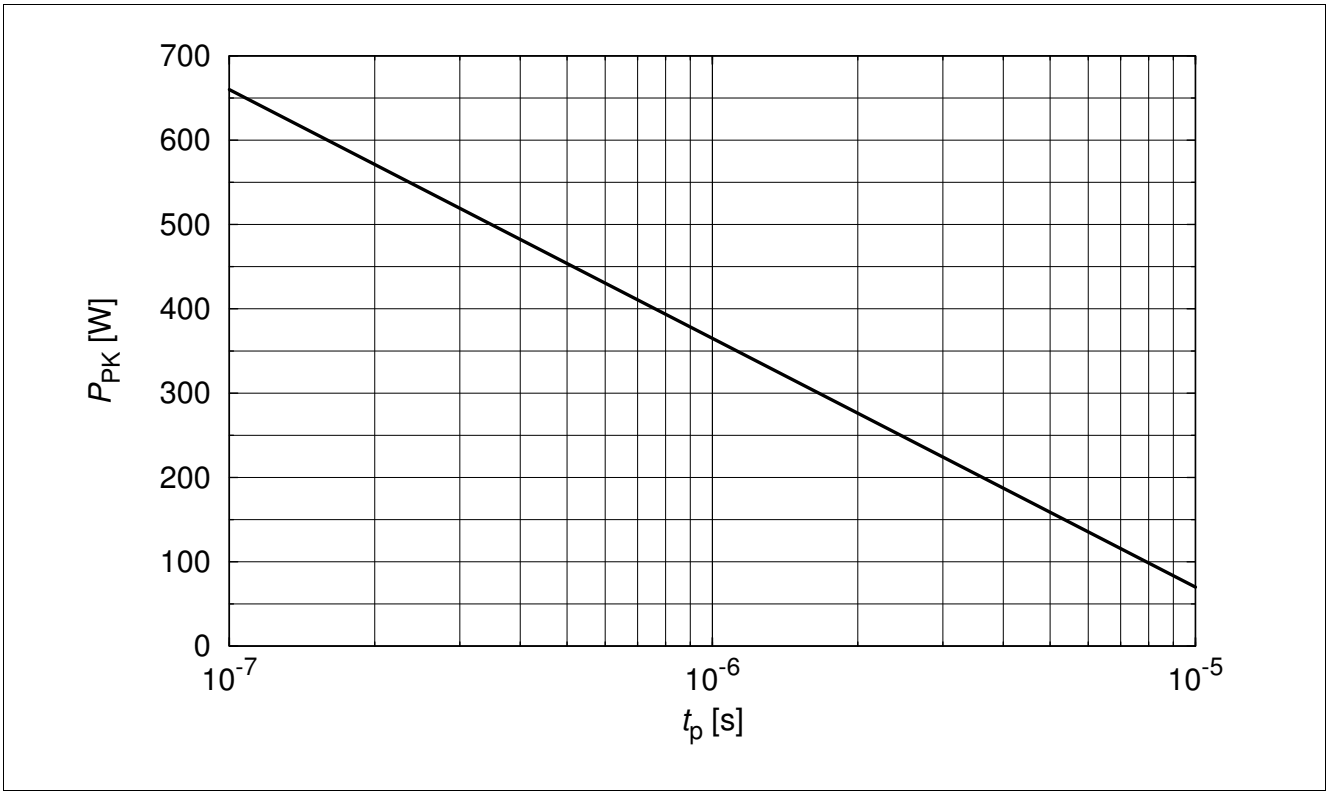

Figure 6 **Peak pulse power: $P_{PK} = f(t_p)$**

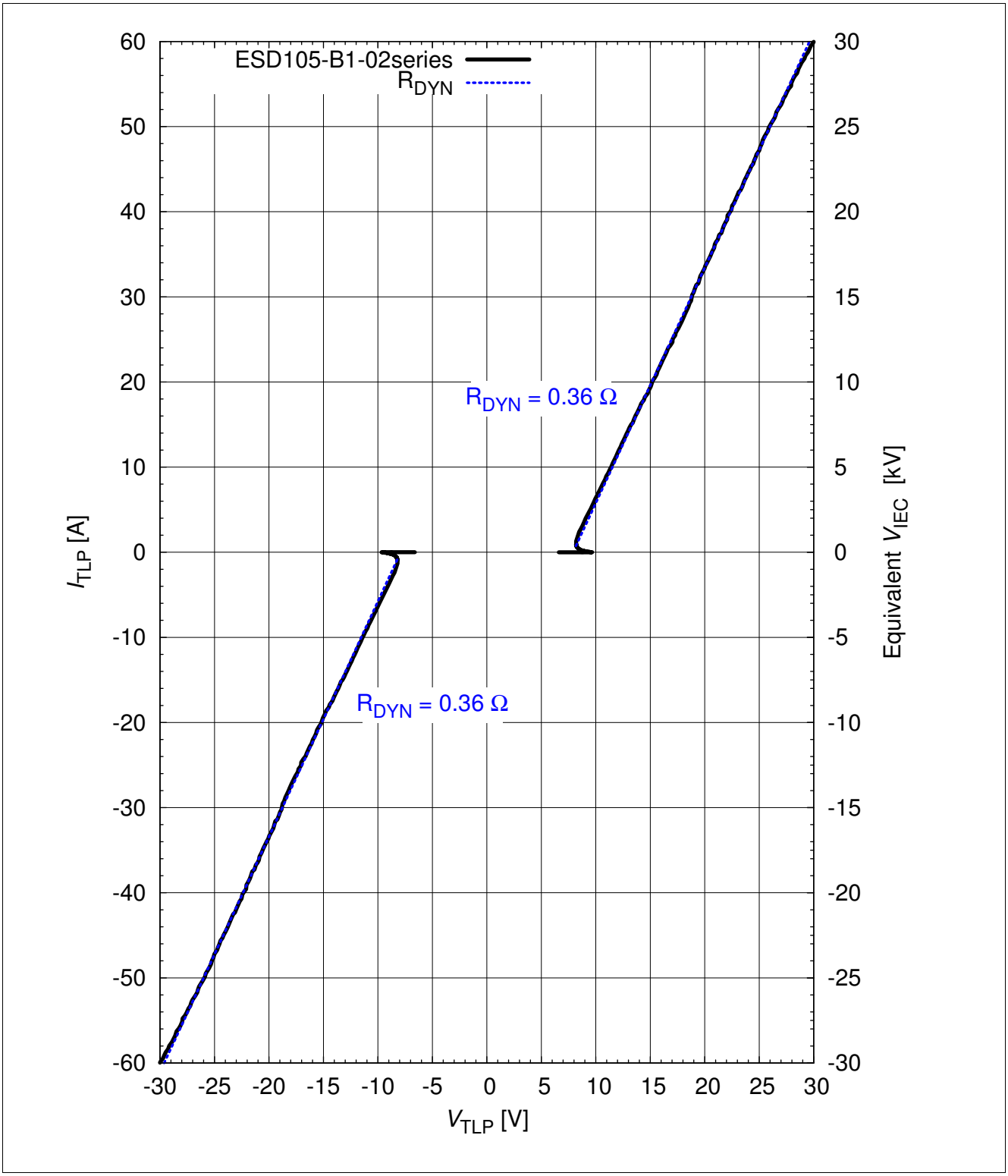

Figure 7 **Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ according ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 0.6 ns, I_{TLP} and V_{TLP} averaging window: t_1 = ns to t_2 = 60 ns, extraction of dynamic resistance using squares fit to TLP characteristics between I_{TLP1} = 10 A and I_{TLP2} = 50 A. Please refer to Application Note AN210[1]**

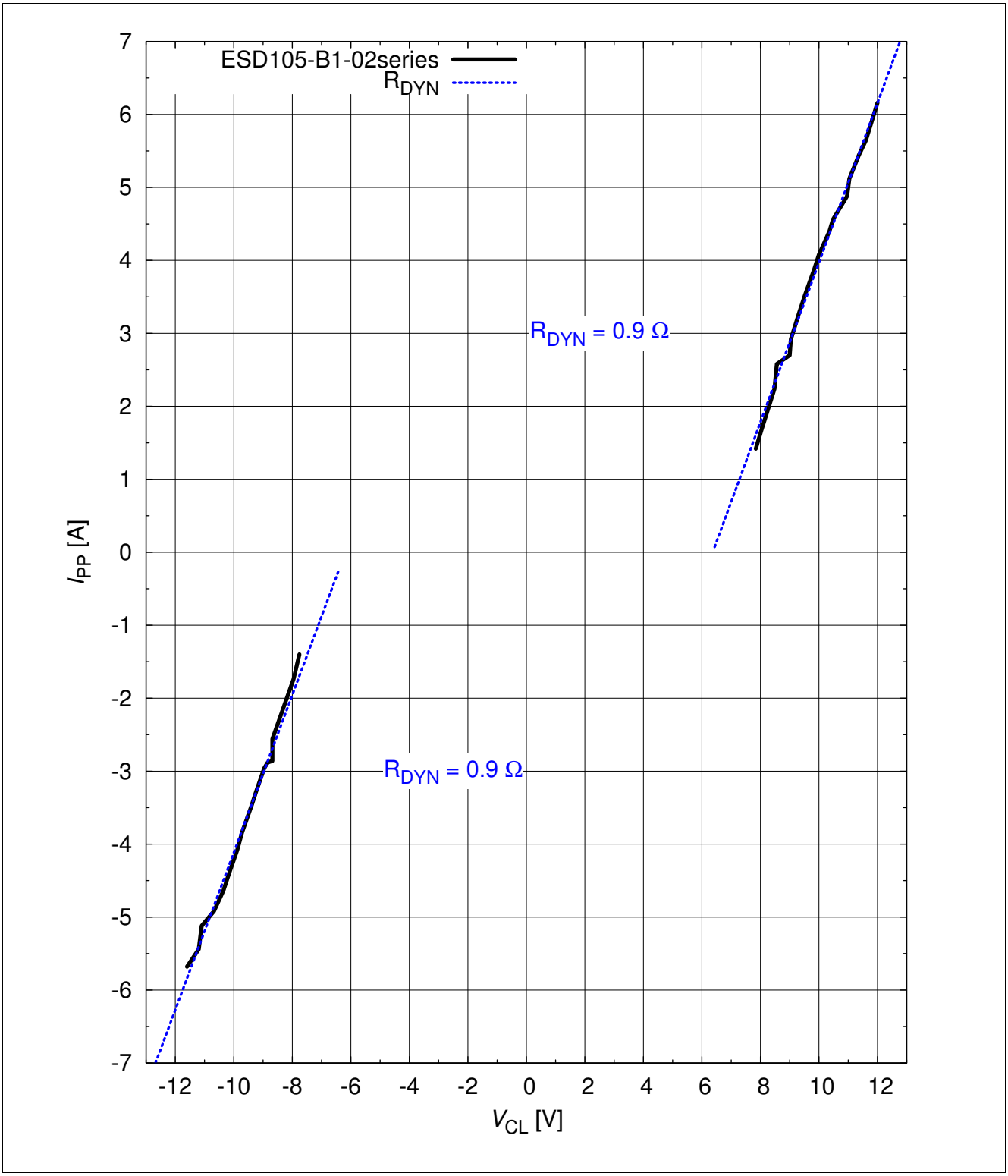

Figure 8 Pulse current (IEC61000-4-5) versus clamping voltage: $I_{PP} = f(V_{CL})$

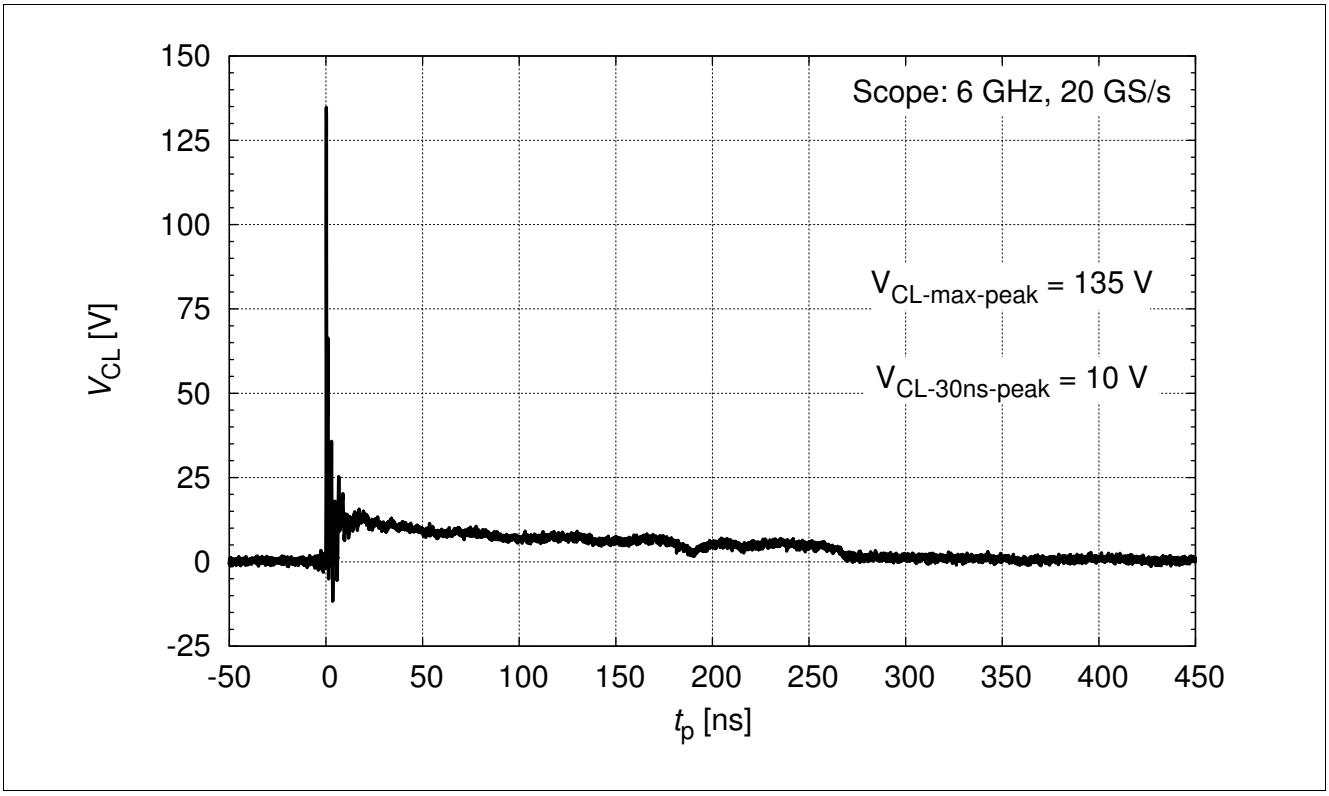

Figure 9 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

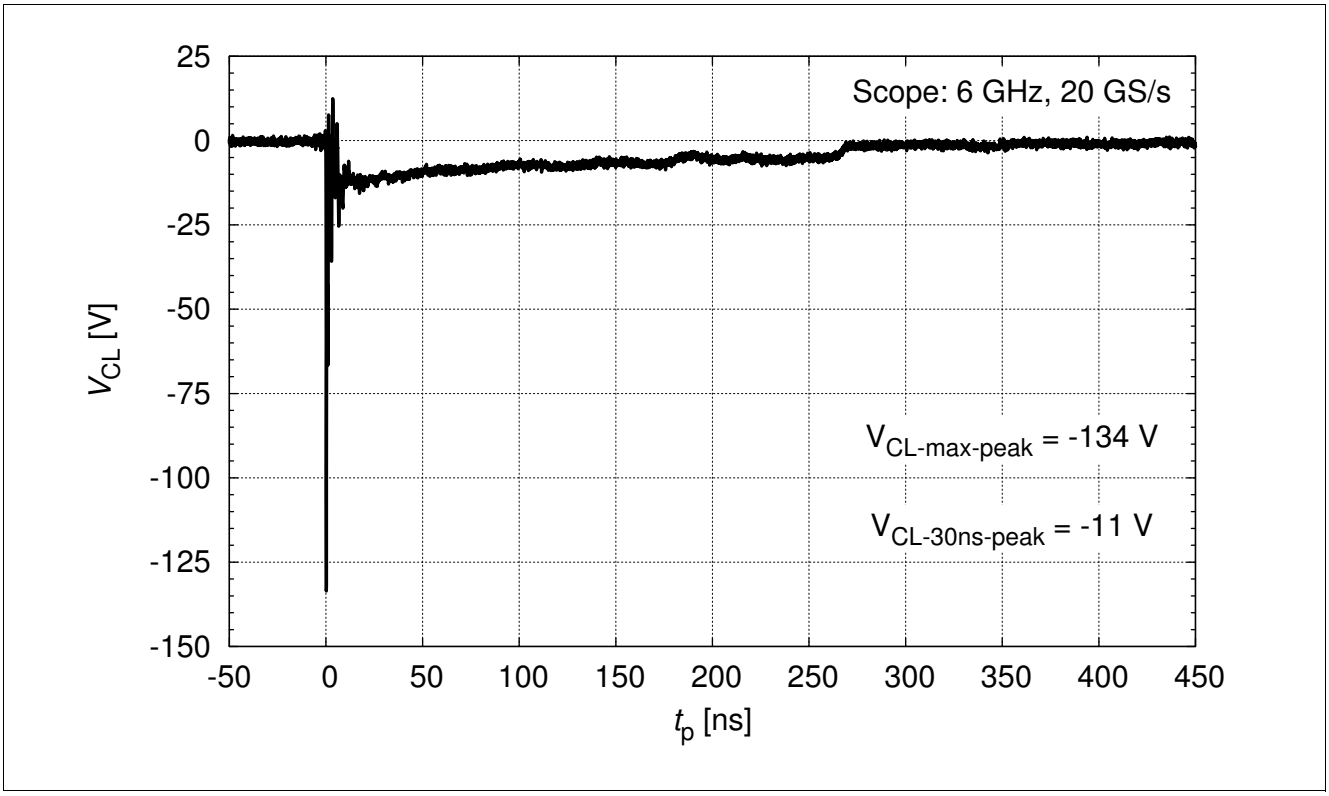

Figure 10 IEC61000-4-2: $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

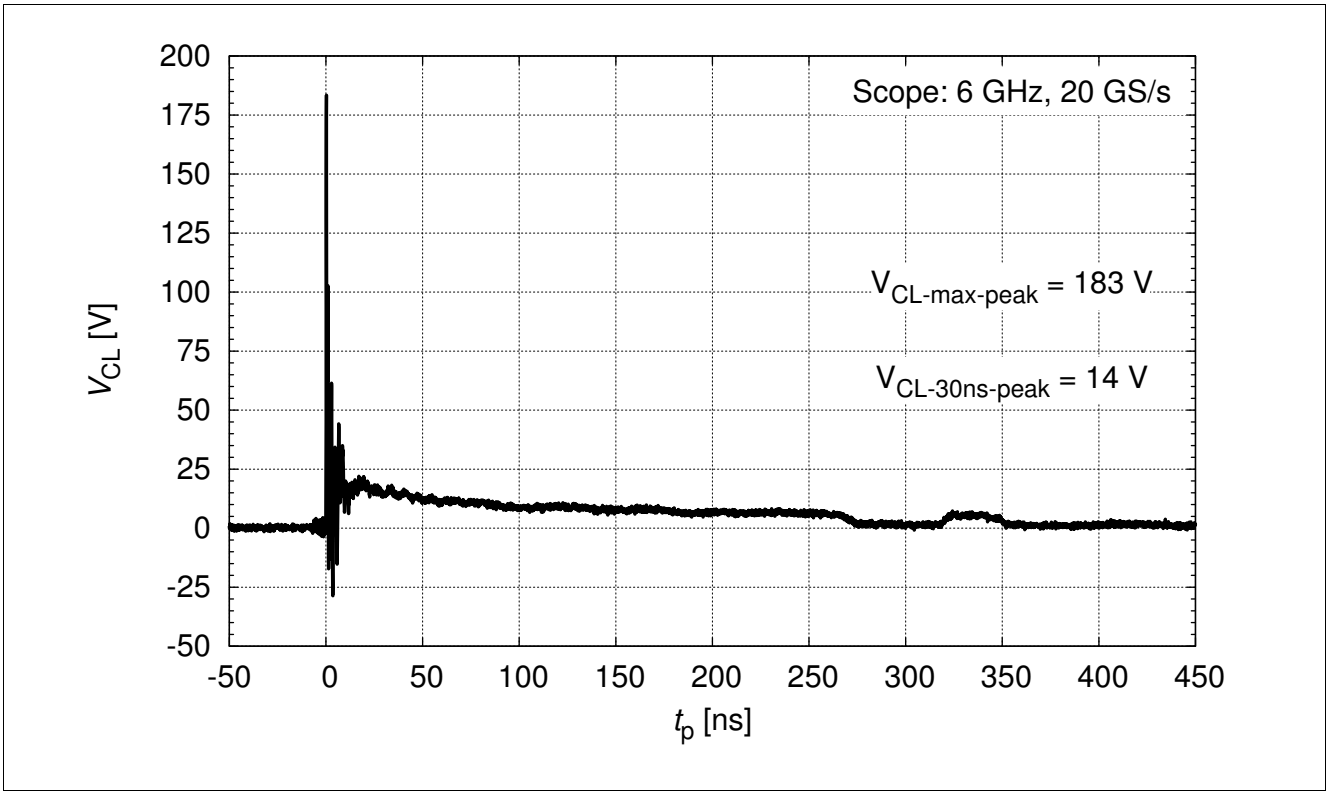

Figure 11 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

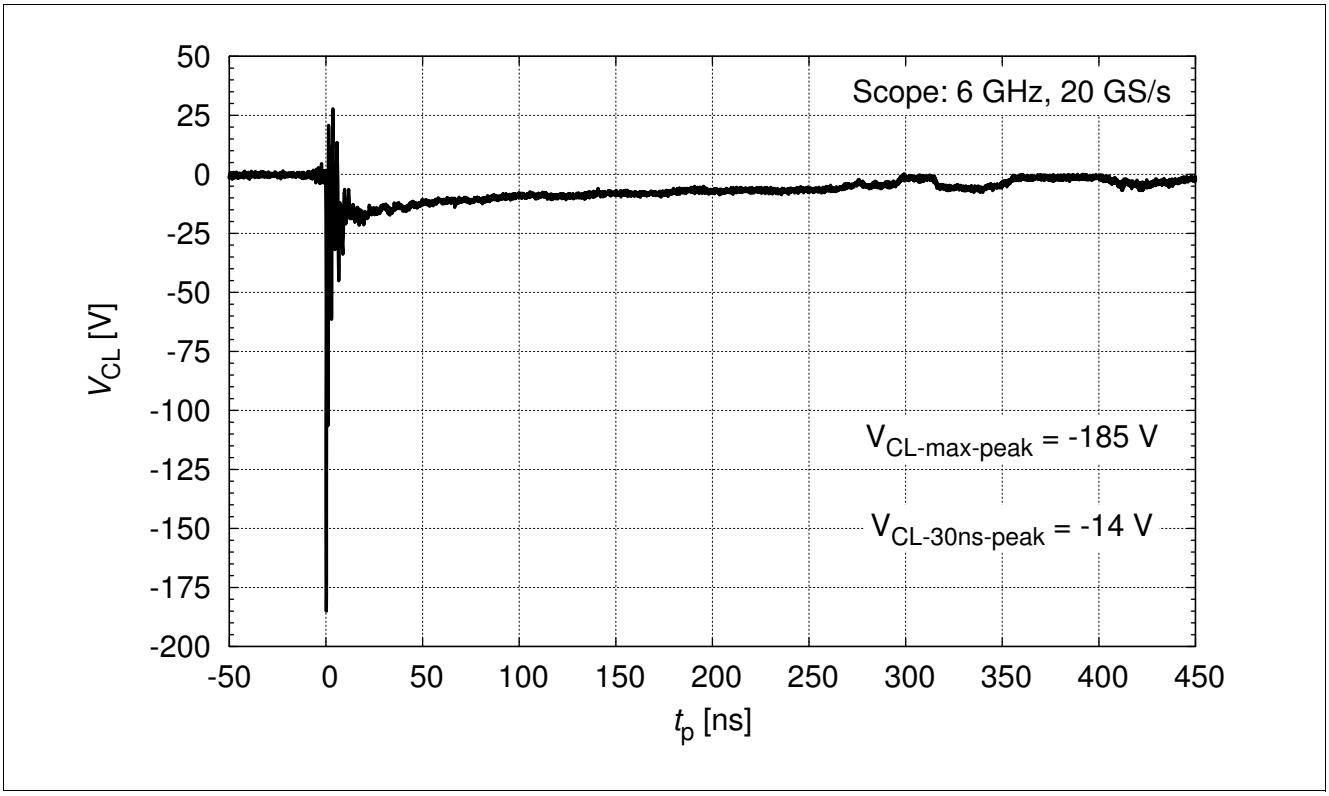

Figure 12 IEC61000-4-2: $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

4 Application Information

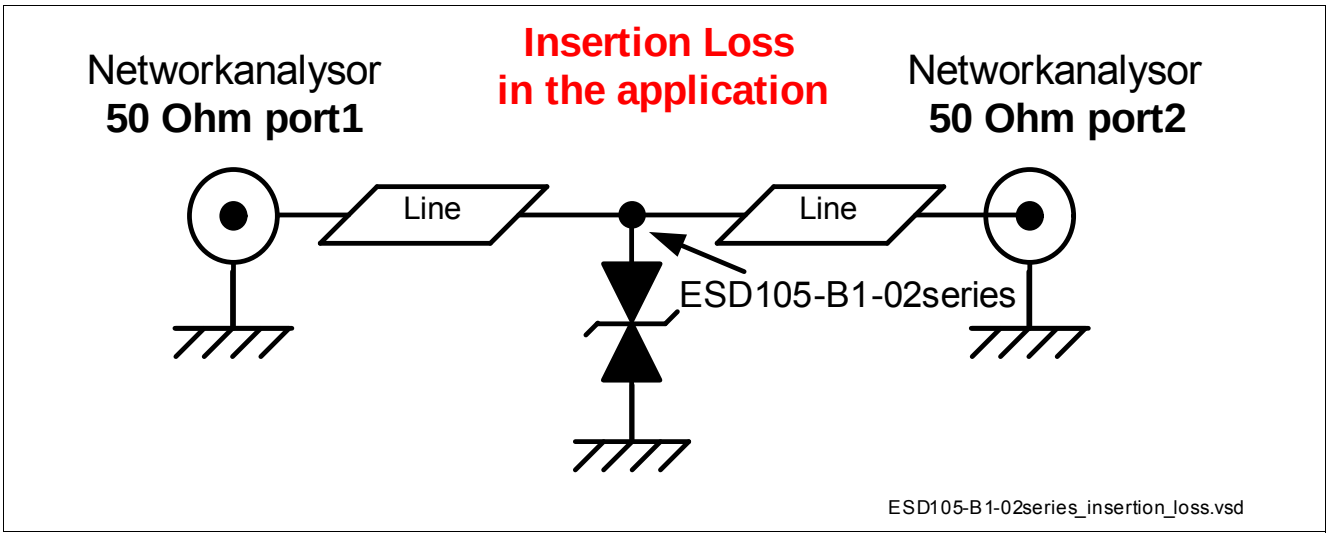

Figure 13 Insertion loss measured in 50 Ω environment

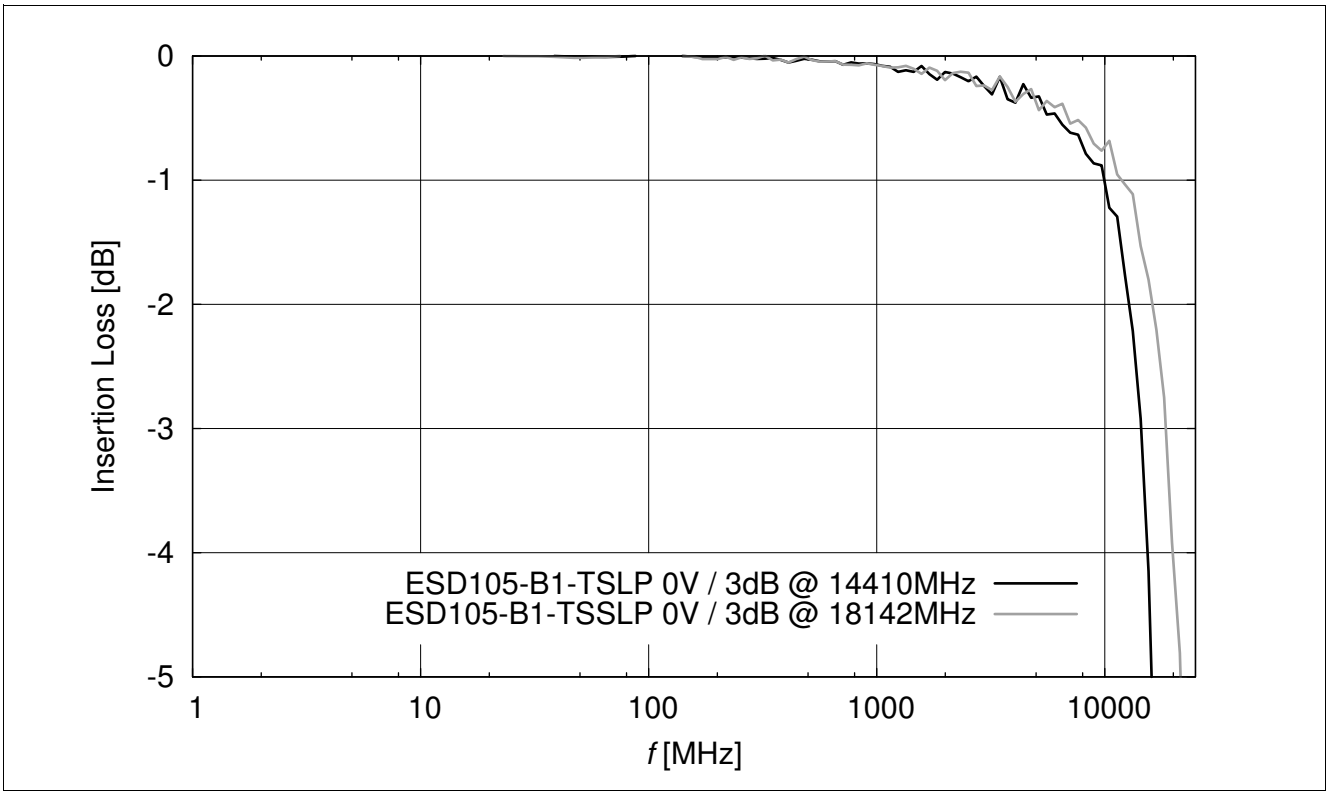

Figure 14 Insertion loss vs. frequency of ESD105-B1-02xx in a 50 Ω system

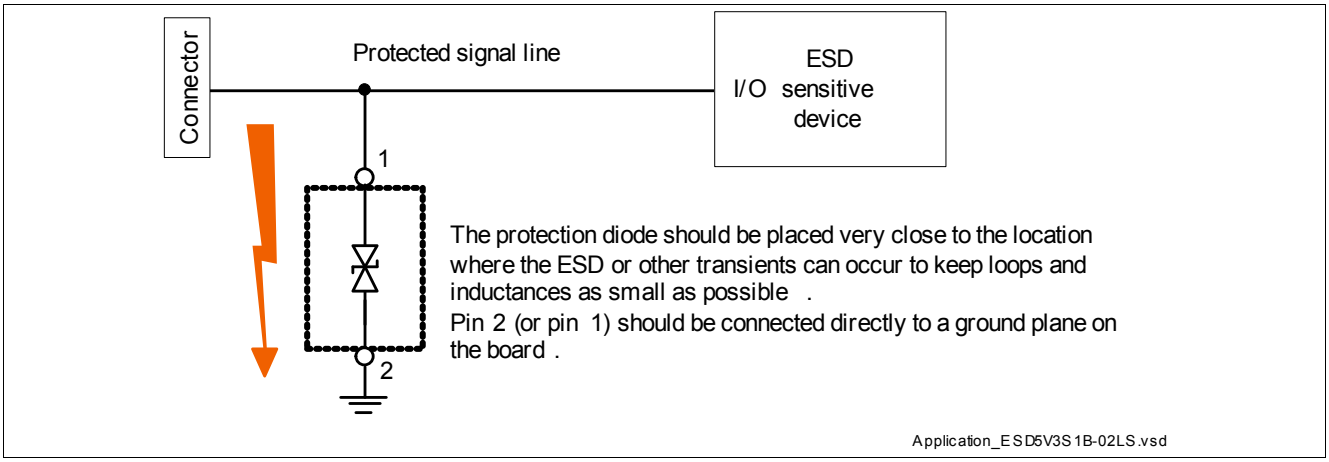

Figure 15 Single line, bi-directional ESD / Transient protection

5 Package Information

5.1 TSSLP-2-4

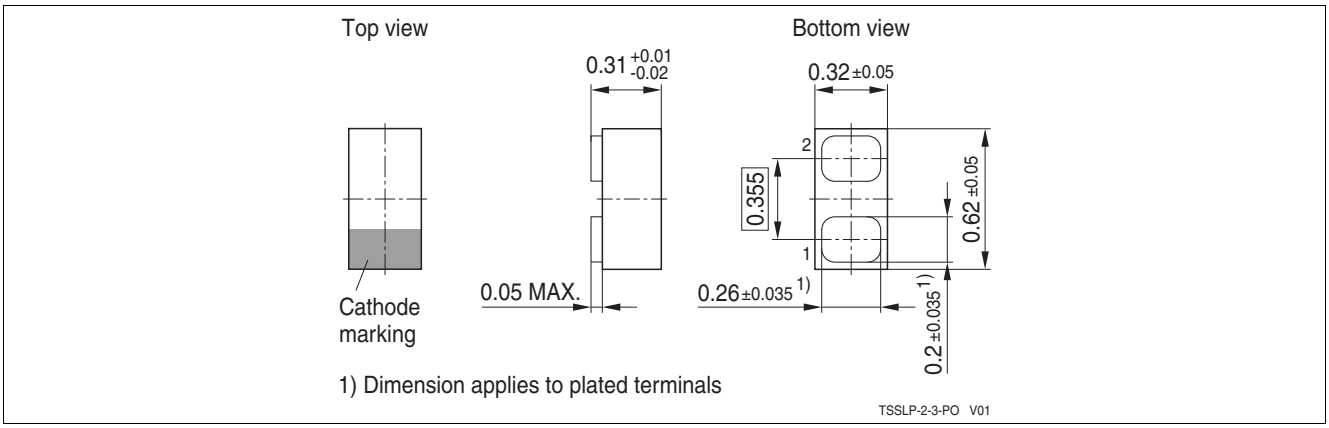

Figure 16 TSSLP-2-4 Package outline

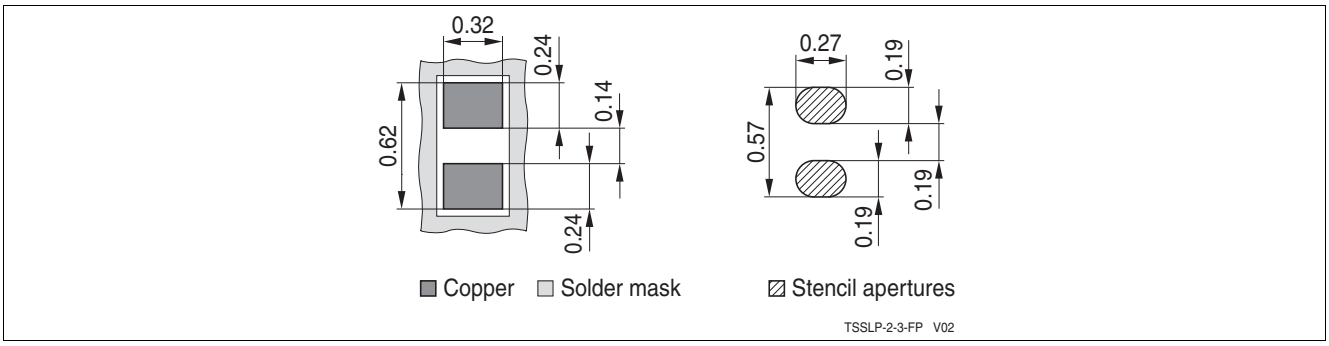

Figure 17 TSSLP-2-4 Footprint

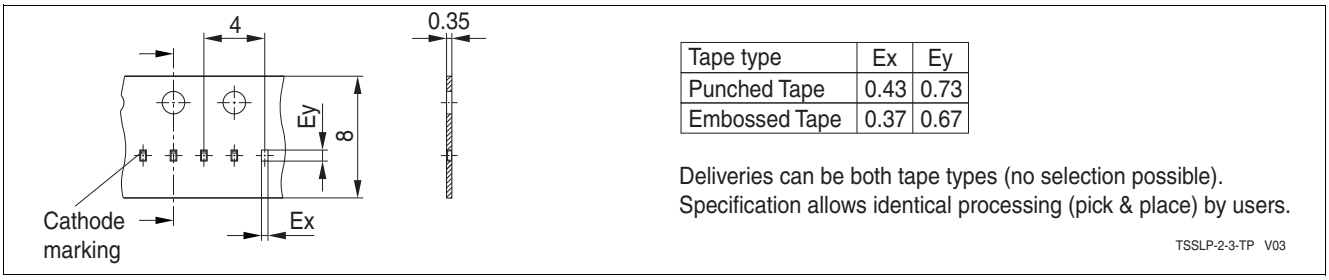

Figure 18 TSSLP-2-4 Packing

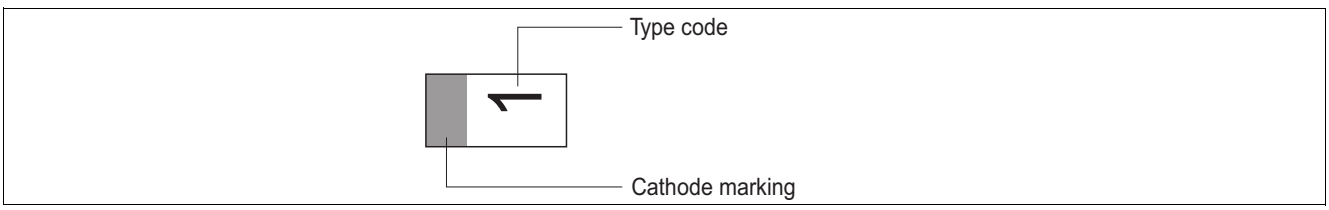

Figure 19 TSSLP-2-4 Marking (example)

5.2 TSLP-2-20

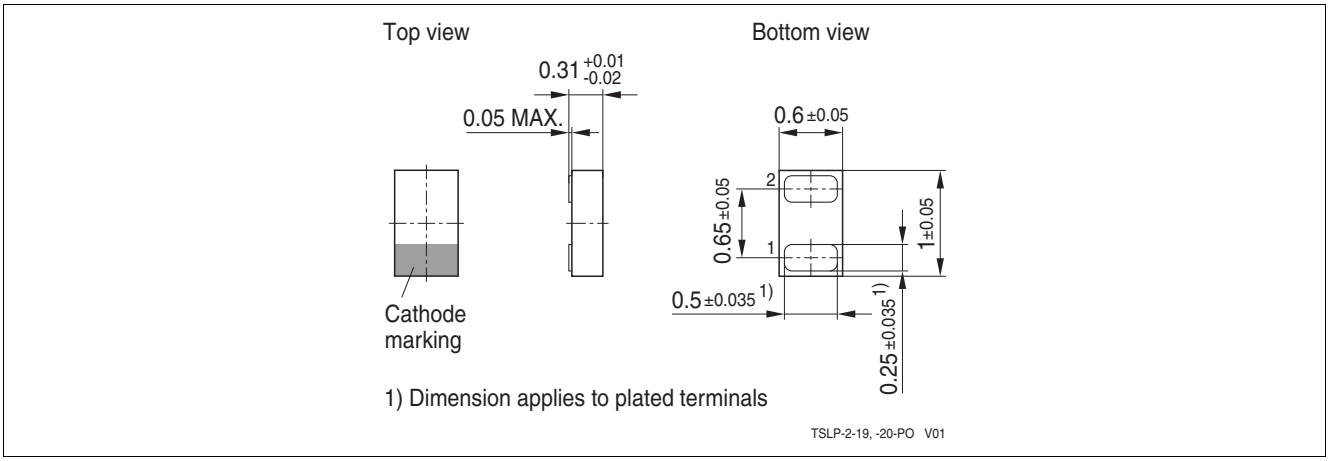

Figure 20 TSLP-2-20 Package outline

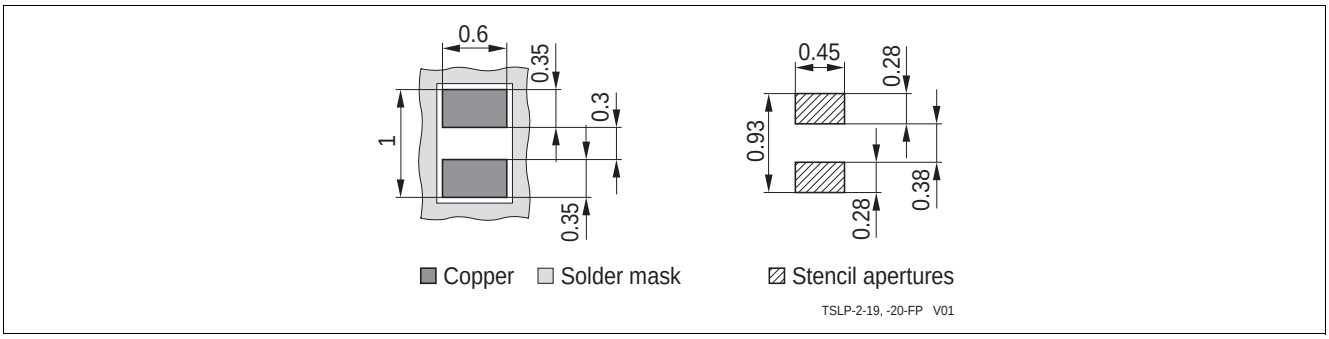

Figure 21 TSLP-2-20 Footprint

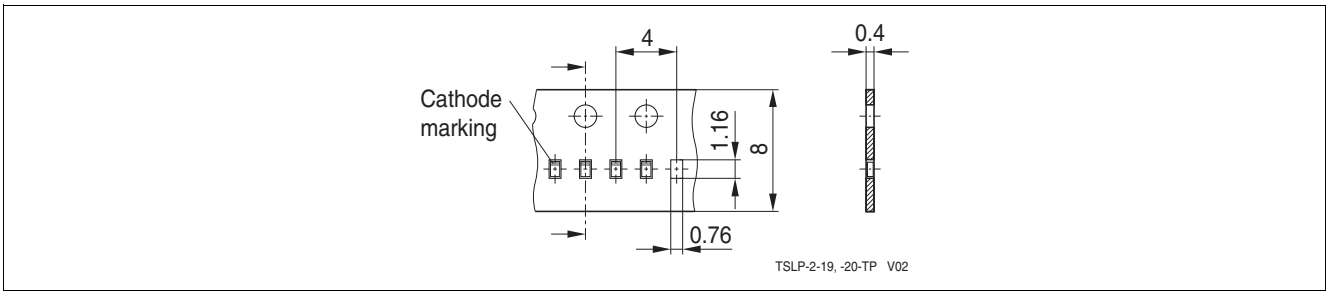

Figure 22 TSLP-2-20 Packing

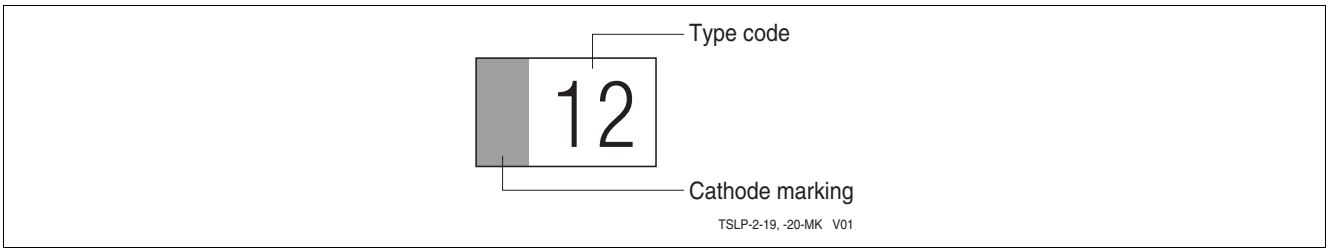

Figure 23 TSLP-2-20 Marking (example)

References

[1] Infineon Technologies AG, “Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology”, Application Note 210, RF and Protection Devices, April 22, 2010, Rev.1.0

[2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

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