

# TLF80511TF

Low Dropout Linear Fixed Voltage Regulator

TLF80511TFV50  
TLF80511TFV33

## Data Sheet

Rev. 1.0, 2014-01-28

# Automotive Power

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## 1 Overview

### Features

- Output Voltage 5 V and 3.3 V
- Output Voltage Precision  $\pm 2\%$
- Output Current up to 400 mA
- Ultra Low Current Consumption 38  $\mu\text{A}$
- Very Low Dropout Voltage: 100 mV at 100 mA Output Current
- Extended Operating Range Starting at 3.3 V
- Small Output Capacitor 1  $\mu\text{F}$
- Output Current Limitation
- Overtemperature Shutdown
- Suitable for Use in Automotive Electronics
- Wide Temperature Range from  $-40\text{ }^\circ\text{C}$  up to  $150\text{ }^\circ\text{C}$
- Green Product (RoHS compliant)
- AEC Qualified



PG-TO252-3

### Description

The TLF80511TF is a linear low dropout voltage regulator for load currents up to 400 mA. An input voltage of up to 40 V is regulated to  $V_{Q,nom} = 5\text{ V}$  (TLF80511TFV50) or  $V_{Q,nom} = 3.3\text{ V}$  (TLF80511TFV33) with  $\pm 2\%$  precision.

The TLF80511TF with a typical quiescent current of 38  $\mu\text{A}$ , is the ideal solution for systems requiring very low operating currents, such as those permanently connected to a battery.

It features a very low dropout voltage of 100 mV, when the output current is less than 100 mA. In addition, the dropout region begins at input voltages of 3.3 V (extended operating range). This makes the TLF80511TF suitable to supply automotive systems.

In addition, the TLF80511's new fast regulation concept requires only a single, 1  $\mu\text{F}$  output capacitor to maintain stable regulation.

The device is designed for the harsh environment of automotive applications. Therefore standard features like output current limitation and overtemperature shutdown are implemented and protect the device against failures like output short circuit to GND, over-current and over-temperatures. The TLF80511TF can be also used in all other applications requiring a stabilized 5 V or 3.3 V supply voltage.

| Type          | Package    | Marking |
|---------------|------------|---------|
| TLF80511TFV50 | PG-TO252-3 | 80511V5 |
| TLF80511TFV33 | PG-TO252-3 | 80511V3 |

## 2 Block Diagram

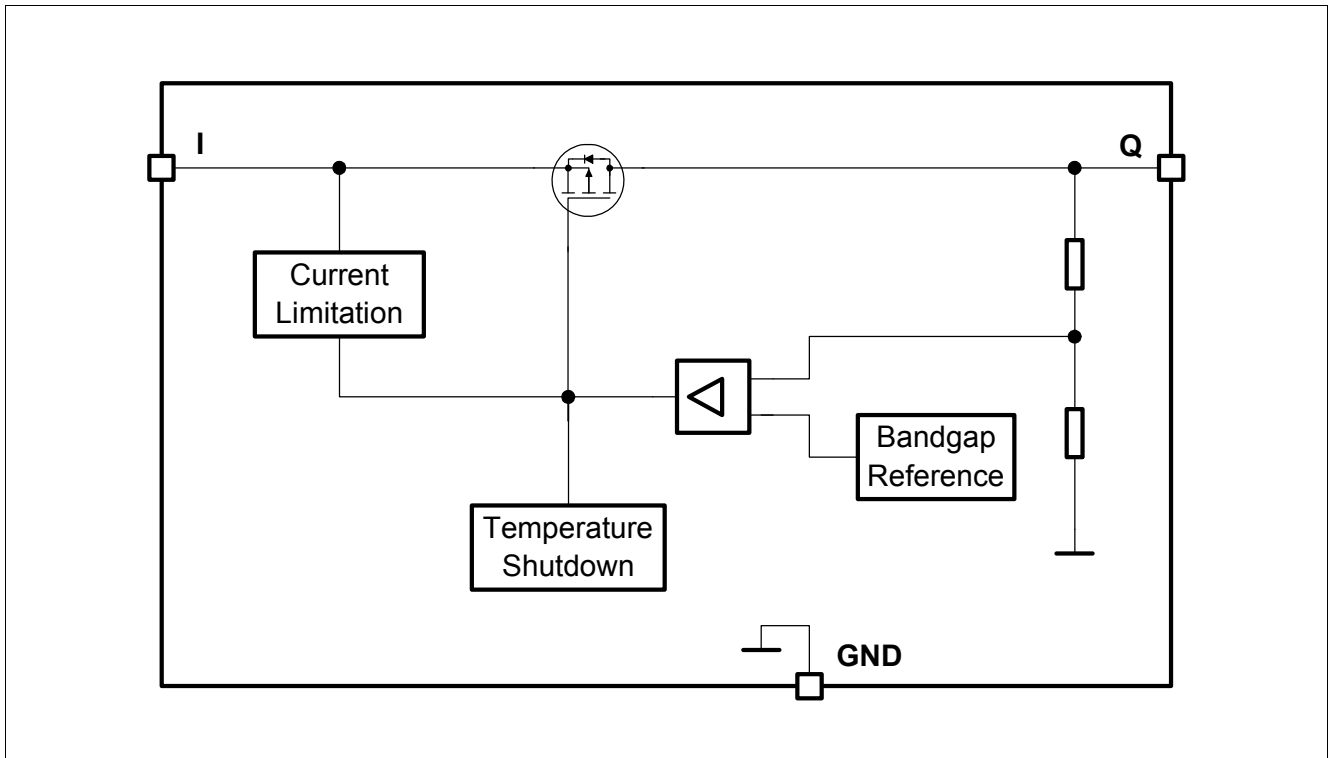


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment PG-TO252-3

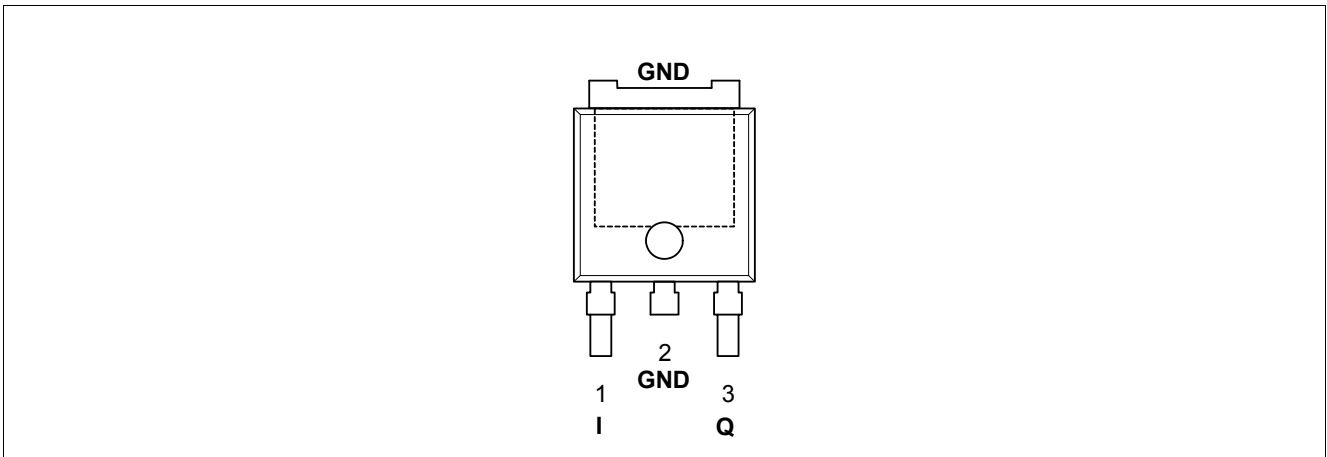


Figure 2 Pin Configuration

#### 3.2 Pin Definitions and Functions PG-TO252-3

| Pin | Symbol | Function  |
|-----|--------|---|
| 1   | I      | <b>Input</b><br>for compensating line influences, a capacitor to GND close to the IC terminals is recommended   |
| 2   | GND    | <b>Ground</b>   |
| 3   | Q      | <b>Output</b><br>block to GND with a capacitor close to the IC terminals, respecting the values given for its capacitance CQ and ESR in the table <b>“Functional Range” on Page 7</b> |
| Tab | GND    | <b>Heat Slug</b><br>connect to heatsink area;<br>connect with GND on PCB  |

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings** <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter                 | Symbol    | Values |      |      | Unit | Note / Test Condition | Number  |
|---------------------------|-----------|--------|------|------|------|-----------------------|---------|
|                           |           | Min.   | Typ. | Max. |      |                       |         |
| <b>Input I</b>            |           |        |      |      |      |                       |         |
| Voltage                   | $V_I$     | -0.3   | –    | 45   | V    | –                     | P_4.1.1 |
| <b>Output Q</b>           |           |        |      |      |      |                       |         |
| Voltage                   | $V_Q$     | -0.3   | –    | 7    | V    | –                     | P_4.1.2 |
| <b>Temperature</b>        |           |        |      |      |      |                       |         |
| Junction Temperature      | $T_j$     | -40    | –    | 150  | °C   | –                     | P_4.1.3 |
| Storage Temperature       | $T_{stg}$ | -55    | –    | 150  | °C   | –                     | P_4.1.4 |
| <b>ESD Susceptibility</b> |           |        |      |      |      |                       |         |
| ESD Susceptibility        | $V_{ESD}$ | -4     | –    | 4    | kV   | HBM <sup>2)</sup>     | P_4.1.5 |
| ESD Susceptibility        | $V_{ESD}$ | -1.5   | –    | 1.5  | kV   | CDM <sup>3)</sup>     | P_4.1.6 |

1) Not subject to production test, specified by design.

2) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS001 (1.5k  $\Omega$ , 100 pF)

3) ESD susceptibility, Charged Device Model "CDM" according JEDEC JESD22-C101

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 2 Functional Range**

| Parameter                                     | Symbol      | Values               |      |      | Unit | Note / Test Condition     | Number  |
|---|-------------|----------------------|------|------|------|---------------------------|---------|
|   |             | Min.                 | Typ. | Max. |      |                           |         |
| Input Voltage Range for Normal Operation      | $V_I$       | $V_{Q,nom} + V_{dr}$ | –    | 40   | V    | –                         | P_4.2.1 |
| Extended Input Voltage Range                  | $V_{I,ext}$ | 3.3                  | –    | 40   | V    | $T_j > 25\text{ °C}^{1)}$ | P_4.2.2 |
| Output Capacitor's Requirements for Stability | $C_Q$       | 1                    | –    | –    | μF   | – <sup>2)</sup>           | P_4.2.3 |
| Output Capacitor's Requirements for Stability | $ESR(C_Q)$  | –                    | –    | 5    | Ω    | – <sup>3)</sup>           | P_4.2.4 |
| Junction Temperature                          | $T_j$       | -40                  | –    | 150  | °C   | –                         | P_4.2.5 |

1) Between min. value and  $V_{Q,nom} + V_{dr}$ :  $V_Q = V_I - V_{dr}$ . Below min. value:  $V_Q = 0\text{ V}$

2) the minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

3) relevant ESR value at  $f = 10\text{ kHz}$

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

## 4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).*

**Table 3 Thermal Resistance**

| Parameter                         | Symbol     | Values |      |      | Unit | Note / Test Condition                                  | Number  |
|-----------------------------------|------------|--------|------|------|------|--|---------|
|                                   |            | Min.   | Typ. | Max. |      |  |         |
| <b>Package Version PG-TO252-3</b> |            |        |      |      |      |  |         |
| Junction to Case <sup>1)</sup>    | $R_{thJC}$ | –      | 4    | –    | K/W  | –  | P_4.3.1 |
| Junction to Ambient               | $R_{thJA}$ | –      | 27   | –    | K/W  | <sup>2)</sup>  | P_4.3.2 |
| Junction to Ambient               | $R_{thJA}$ | –      | 95   | –    | K/W  | footprint only <sup>3)</sup>                           | P_4.3.3 |
| Junction to Ambient               | $R_{thJA}$ | –      | 52   | –    | K/W  | 300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> | P_4.3.4 |
| Junction to Ambient               | $R_{thJA}$ | –      | 39   | –    | K/W  | 600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> | P_4.3.5 |

1) Not subject to production test, specified by design

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70μm Cu, 2 x 35μm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 1 copper layer (1 x 70μm Cu).

## 5 Block Description and Electrical Characteristics

### 5.1 Voltage Regulation

The output voltage  $V_Q$  is divided by a resistor network. This fractional voltage is compared to an internal voltage reference and drives the pass transistor accordingly.

The control loop stability depends on the output capacitor  $C_Q$ , the load current, the chip temperature and the internal circuit design. To ensure stable operation, the output capacitor's capacitance and its equivalent series resistor ESR requirements given in **Table 2 "Functional Range" on Page 7** must be maintained. For details see the typical performance graph **"Stability Region: Equivalent Serial Resistor ESR versus Output Current  $I_Q$ " on Page 11**. Since the output capacitor is used to buffer load steps, it should be sized according to the application's needs.

An input capacitor  $C_I$  is not required for stability, but is recommended to compensate line fluctuations. An additional reverse polarity protection diode and a combination of several capacitors for filtering should be used. Connect the capacitors close to the regulator terminals.

Whenever the load current exceeds the specified limit, e.g. in case of a short circuit, the output current is limited and the output voltage decreases.

The overtemperature shutdown circuit prevents the IC from immediate destruction under fault conditions (e.g. output continuously short-circuited) by switching off the power stage. After the chip has cooled, the regulator restarts. This oscillatory thermal behaviour causes the junction temperature to exceed the 150° C maximum and significantly reducing the IC's life.

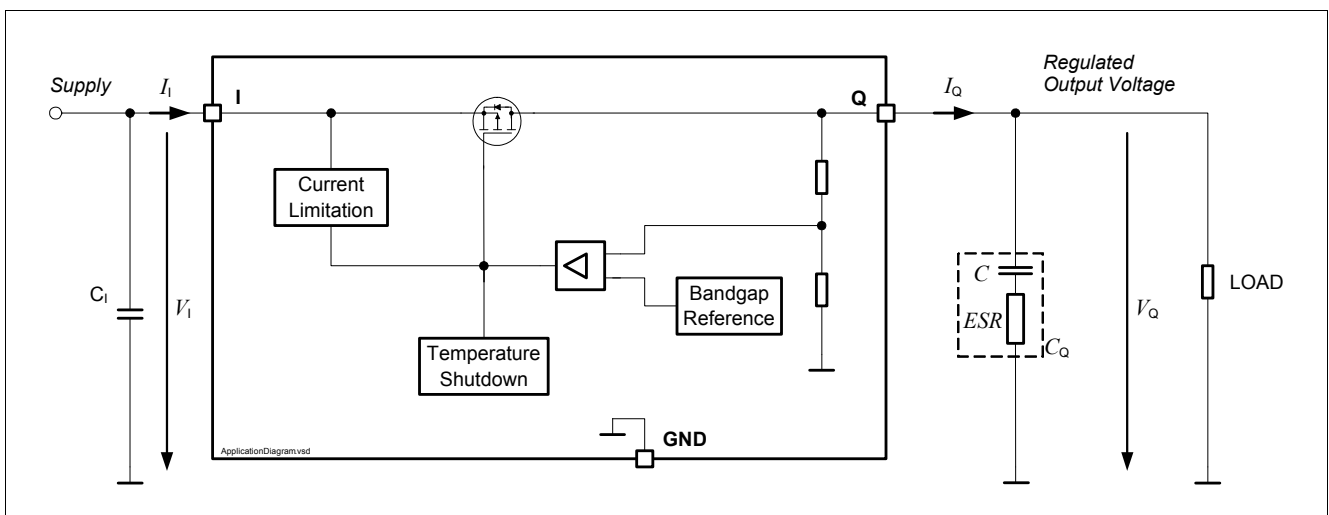


Figure 3 Block Diagram Voltage Regulation



**Block Description and Electrical Characteristics**
**Table 4 Electrical Characteristics Voltage Regulator 5 V and 3.3 V version**
 $V_1 = 13.5 \text{ V}$ ;  $T_j = -40 \text{ }^\circ\text{C}$  to  $+150 \text{ }^\circ\text{C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

| Parameter  | Symbol              | Values |      |      | Unit             | Note / Test Condition  | Number   |
|--|---------------------|--------|------|------|------------------|--|----------|
|  |                     | Min.   | Typ. | Max. |                  |  |          |
| Output Voltage Precision<br>TLF80511TFV50                              | $V_Q$               | 4.9    | 5.0  | 5.1  | V                | $0.05 \text{ mA} < I_Q < 400 \text{ mA}$<br>$6 \text{ V} < V_1 < 28 \text{ V}$   | P_5.1.1  |
| Output Voltage Precision<br>TLF80511TFV50                              | $V_Q$               | 4.9    | 5.0  | 5.1  | V                | $0.05 \text{ mA} < I_Q < 200 \text{ mA}$<br>$5.5 \text{ V} < V_1 < 40 \text{ V}$ | P_5.1.2  |
| Output Voltage Precision<br>TLF80511TFV33                              | $V_Q$               | 3.23   | 3.3  | 3.37 | V                | $0.05 \text{ mA} < I_Q < 400 \text{ mA}$<br>$4.4 \text{ V} < V_1 < 28 \text{ V}$ | P_5.1.3  |
| Output Voltage Precision<br>TLF80511TFV33                              | $V_Q$               | 3.23   | 3.3  | 3.37 | V                | $0.05 \text{ mA} < I_Q < 200 \text{ mA}$<br>$3.9 \text{ V} < V_1 < 40 \text{ V}$ | P_5.1.4  |
| Output Current Limitation  | $I_{Q,max}$         | 401    | 600  | 900  | mA               | $0 \text{ V} < V_Q < 4.8 \text{ V}$  | P_5.1.5  |
| Load Regulation<br>steady-state  | $ \Delta V_Q,load $ | –      | 20   | 50   | mV               | $I_Q = 0.05 \text{ mA}$ to $400 \text{ mA}$<br>$V_1 = 6 \text{ V}$               | P_5.1.6  |
| Line Regulation<br>steady-state  | $ \Delta V_Q,line $ | –      | 10   | 30   | mV               | $V_1 = 8 \text{ V}$ to $32 \text{ V}$<br>$I_Q = 5 \text{ mA}$                    | P_5.1.7  |
| Dropout Voltage <sup>1)</sup><br>$V_{dr} = V_1 - V_Q$<br>TLF80511TFV50 | $V_{dr}$            | –      | 250  | 500  | mV               | $I_Q = 250 \text{ mA}$   | P_5.1.8  |
| Dropout Voltage<br>$V_{dr} = V_1 - V_Q$<br>TLF80511TFV50               | $V_{dr}$            | –      | 100  | –    | mV               | $I_Q = 100 \text{ mA}$   | P_5.1.9  |
| Dropout Voltage<br>$V_{dr} = V_1 - V_Q$<br>TLF80511TFV33               | $V_{dr}$            | –      | 320  | 650  | mV               | $I_Q = 250 \text{ mA}$   | P_5.1.10 |
| Dropout Voltage<br>$V_{dr} = V_1 - V_Q$<br>TLF80511TFV33               | $V_{dr}$            | –      | 130  | –    | mV               | $I_Q = 100 \text{ mA}$   | P_5.1.11 |
| Power Supply Ripple Rejection <sup>2)</sup><br>TLF80511TFV50           | $PSRR$              | –      | 55   | –    | dB               | $f_{ripple} = 100 \text{ Hz}$<br>$V_{ripple} = 0.5 \text{ Vpp}$                  | P_5.1.12 |
| Overtemperature Shutdown<br>Threshold                                  | $T_{j,sd}$          | 151    | 175  | 200  | $^\circ\text{C}$ | $T_j$ increasing <sup>2)</sup>   | P_5.1.13 |
| Overtemperature Shutdown<br>Threshold Hysteresis                       | $T_{j,sdh}$         | –      | 15   | –    | K                | $T_j$ decreasing <sup>2)</sup>   | P_5.1.14 |

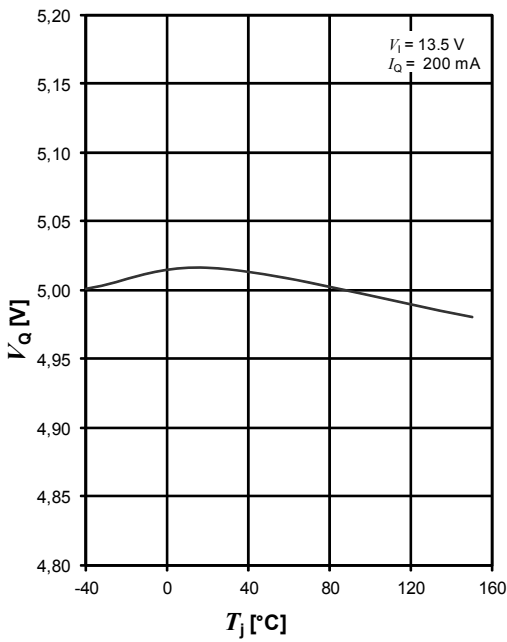
1) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_1 = 13.5\text{V}$ 

2) Not subject to production test, specified by design

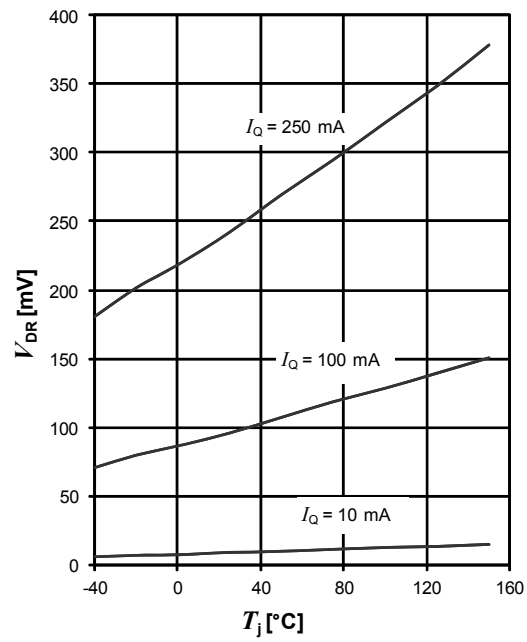
## 5.2 Typical Performance Characteristics Voltage Regulator

### Typical Performance Characteristics

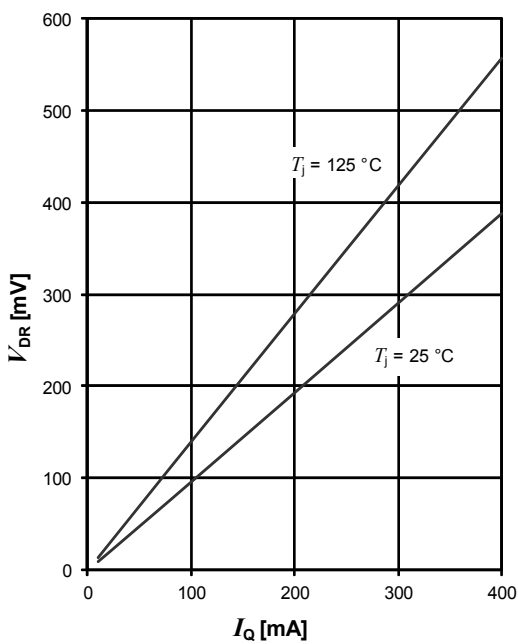
Output Voltage  $V_Q$  versus Junction Temperature  $T_j$  (TLF80511TFV50)



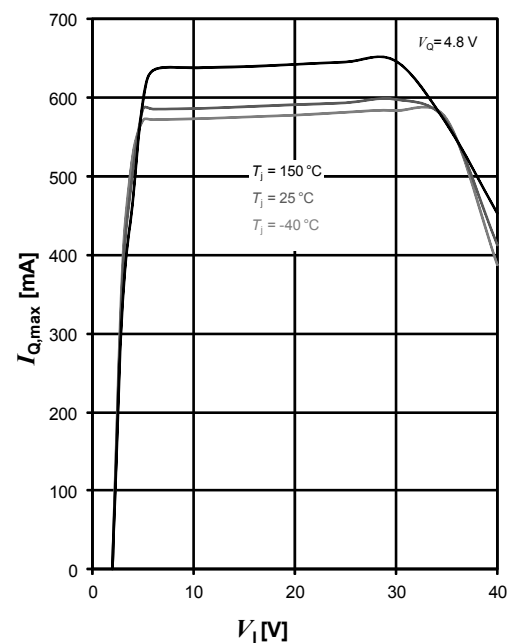
Dropout Voltage  $V_{dr}$  versus Junction Temperature  $T_j$  (TLF80511TFV50)



Dropout Voltage  $V_{dr}$  versus Output Current  $I_Q$  (TLF80511TFV50)

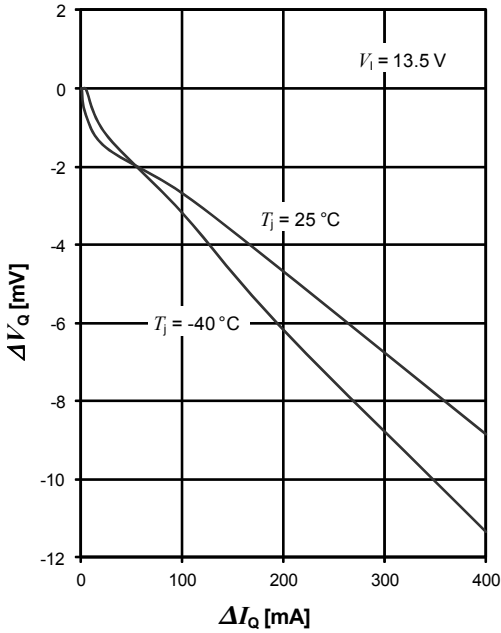


Maximum Output Current  $I_{Q,max}$  versus Input Voltage  $V_I$  (TLF80511TFV50)

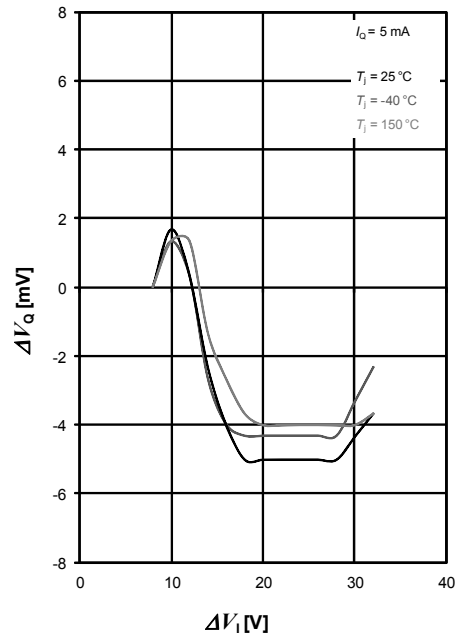


Block Description and Electrical Characteristics

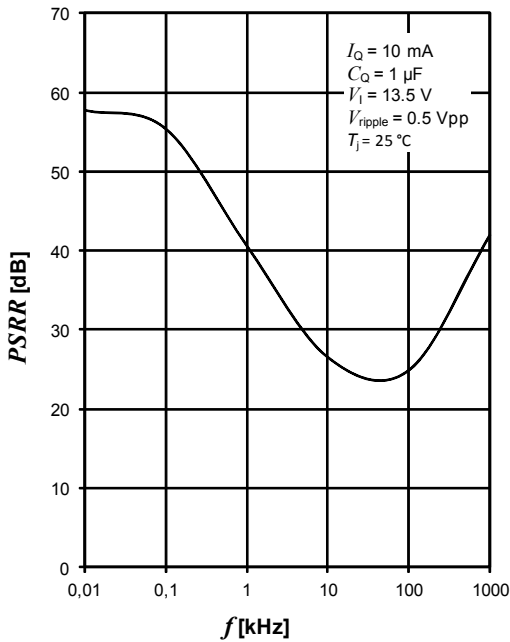
**Load Regulation  $\Delta V_{Q,load}$  versus Output Current Change  $\Delta I_Q$**



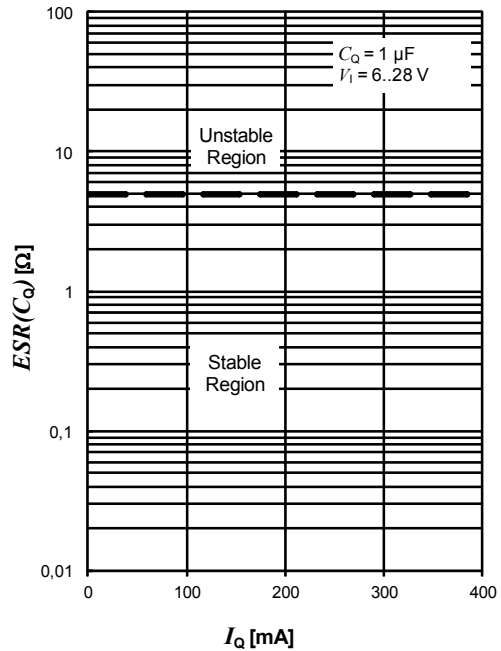
**Line Regulation  $\Delta V_{Q,line}$  versus Input Voltage  $\Delta V_I$**



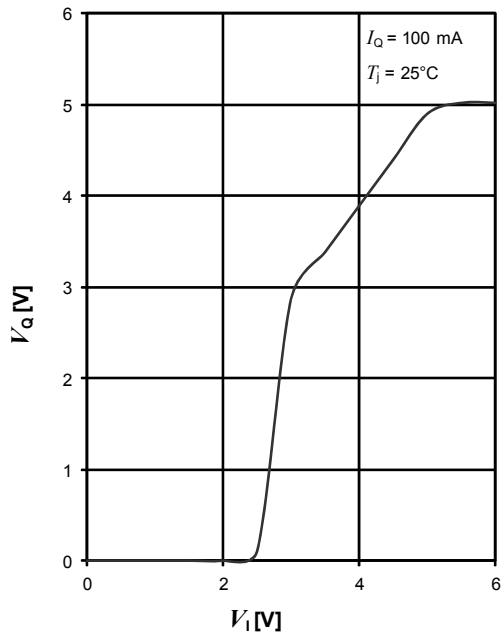
**Power Supply Ripple Rejection versus Frequency (TLF80511TFV50)**



**Stability Region: Equivalent Serial Resistor  $ESR$  versus Output Current  $I_Q$**



**Output Voltage  $V_Q$  versus  
Input Voltage  $V_I$  (TLF80511TFV50)**



### 5.3 Current Consumption

**Table 5 Electrical Characteristics Current Consumption**

$V_1 = 13.5\text{ V}$ ;  $T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

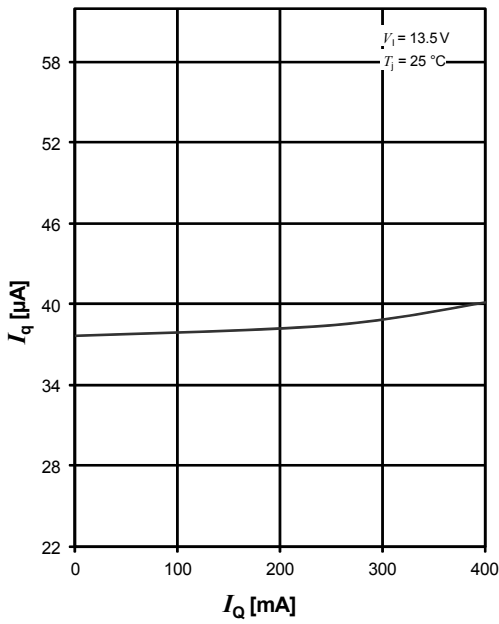
| Parameter                                | Symbol | Values |      |      | Unit          | Note / Test Condition                               | Number  |
|--|--------|--------|------|------|---------------|---|---------|
|  |        | Min.   | Typ. | Max. |               |   |         |
| Current Consumption<br>$I_q = I_1 - I_Q$ | $I_q$  | –      | 38   | 46   | $\mu\text{A}$ | $I_Q = 0.05\text{ mA}$<br>$T_j < 25\text{ °C}$      | P_5.3.1 |
| Current Consumption<br>$I_q = I_1 - I_Q$ | $I_q$  | –      | –    | 75   | $\mu\text{A}$ | $I_Q = 0.05\text{ mA}$<br>$T_j < 125\text{ °C}$     | P_5.3.2 |
| Current Consumption<br>$I_q = I_1 - I_Q$ | $I_q$  | –      | 67   | 80   | $\mu\text{A}$ | $I_Q = 400\text{ mA}$<br>$T_j < 125\text{ °C}^{1)}$ | P_5.3.3 |

1) Not subject to production test, specified by design.

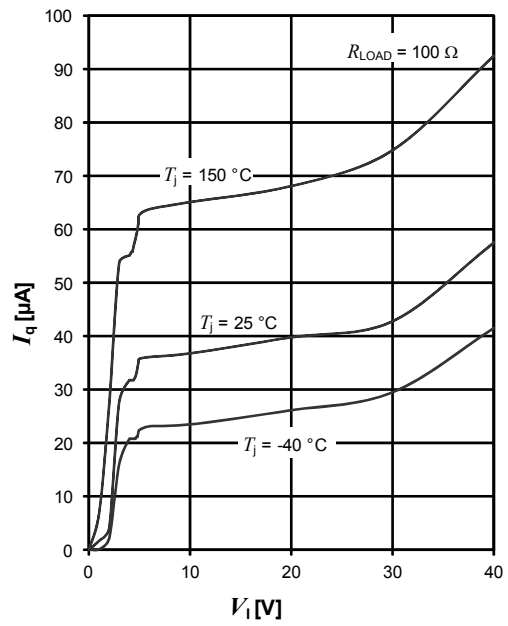
### 5.4 Typical Performance Characteristics Current Consumption

#### Typical Performance Characteristics

Current Consumption  $I_q$  versus Output Current  $I_Q$



Current Consumption  $I_q$  versus Input Voltage  $V_i$



## 6 Application Information

### 6.1 Application Diagram

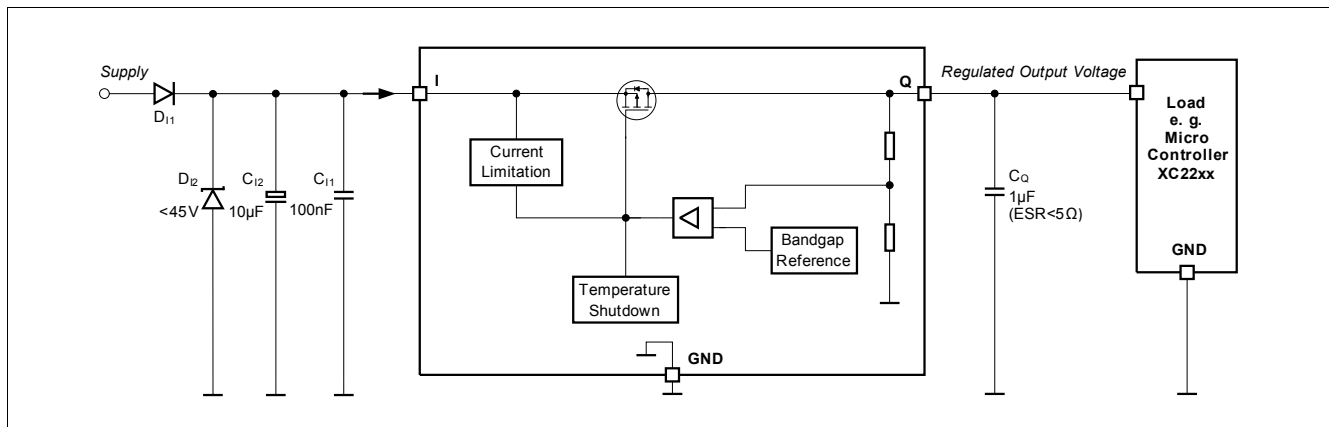


Figure 4 Application Diagram

### 6.2 Selection of External Components

#### 6.2.1 Input Pin

The typical input circuitry for a linear voltage regulator is shown in the application diagram above.

A ceramic capacitor at the input, in the range of 100nF to 470nF, is recommended to filter out the high frequency disturbances imposed by the line e.g. ISO pulses 3a/b. This capacitor must be placed very close to the input pin of the linear voltage regulator on the PCB.

An aluminum electrolytic capacitor in the range of 10µF to 470µF is recommended as an input buffer to smooth out high energy pulses, such as ISO pulse 2a. This capacitor should be placed close to the input pin of the linear voltage regulator on the PCB.

An overvoltage suppressor diode can be used to further suppress any high voltage beyond the maximum rating of the linear voltage regulator and protect the device against any damage due to over-voltage above 45 V.

The external components at the input are not mandatory for the operation of the voltage regulator, but they are recommended in order to protect the voltage regulator against external disturbances and damages.

#### 6.2.2 Output Pin

An output capacitor is mandatory for the stability of linear voltage regulators.

The requirement to the output capacitor is given in **“Functional Range” on Page 7**. The graph **“Stability Region: Equivalent Serial Resistor ESR versus Output Current IQ” on Page 11** shows the stable operation range of the device.

TLF80511TF is designed to be stable with extremely low ESR capacitors. According to the automotive requirements, ceramic capacitors with X5R or X7R dielectrics are recommended.

The output capacitor should be placed as close as possible to the regulator’s output and GND pins and on the same side of the PCB as the regulator itself.

In case of rapid transients of input voltage or load current, the capacitance should be dimensioned in accordance and verified in the real application that the output stability requirements are fulfilled.

### 6.3 Thermal Considerations

Knowing the input voltage, the output voltage and the load profile of the application, the total power dissipation can be calculated:

$$P_D = (V_I - V_Q) \times I_Q + V_I \times I_q \quad (1)$$

with

- $P_D$ : continuous power dissipation
- $V_I$ : input voltage
- $V_Q$ : output voltage
- $I_Q$ : output current
- $I_q$ : quiescent current

The maximum acceptable thermal resistance  $R_{thJA}$  can then be calculated:

$$R_{thJA,max} = (T_{j,max} - T_a) / P_D \quad (2)$$

with

- $T_{j,max}$ : maximum allowed junction temperature
- $T_a$ : ambient temperature

Based on the above calculation the proper PCB type and the necessary heat sink area can be determined with reference to the specification in [“Thermal Resistance” on Page 7](#).

#### Example

Application conditions:

$$V_I = 13.5V$$

$$V_Q = 5V$$

$$I_Q = 150mA$$

$$T_a = 85^\circ C$$

Calculation of  $R_{thJA,max}$ :

$$\begin{aligned} P_D &= (V_I - V_Q) \times I_Q + V_I \times I_q && (V_I \times I_q \text{ can be neglected because of very low } I_q) \\ &= (13.5V - 5V) \times 150mA \\ &= 1.275W \end{aligned}$$

$$\begin{aligned} R_{thJA,max} &= (T_{j,max} - T_a) / P_D \\ &= (150^\circ C - 85^\circ C) / 1.275W = 50.98K/W \end{aligned}$$

As a result, the PCB design must ensure a thermal resistance  $R_{thJA}$  lower than 50.98 K/W. According to [“Thermal Resistance” on Page 7](#), at least 600 mm<sup>2</sup> heatsink area is needed on the FR4 1s0p PCB, or the FR4 2s2p board can be used.



## 6.4 Reverse Polarity Protection

TLF80511TF is not self protected against reverse polarity faults and must be protected by external components against negative supply voltage. An external reverse polarity diode is needed. The absolute maximum ratings of the device as specified in **“Absolute Maximum Ratings” on Page 6** must be kept.

## 6.5 Further Application Information

- For further information you may contact <http://www.infineon.com/>

7 Package Outlines

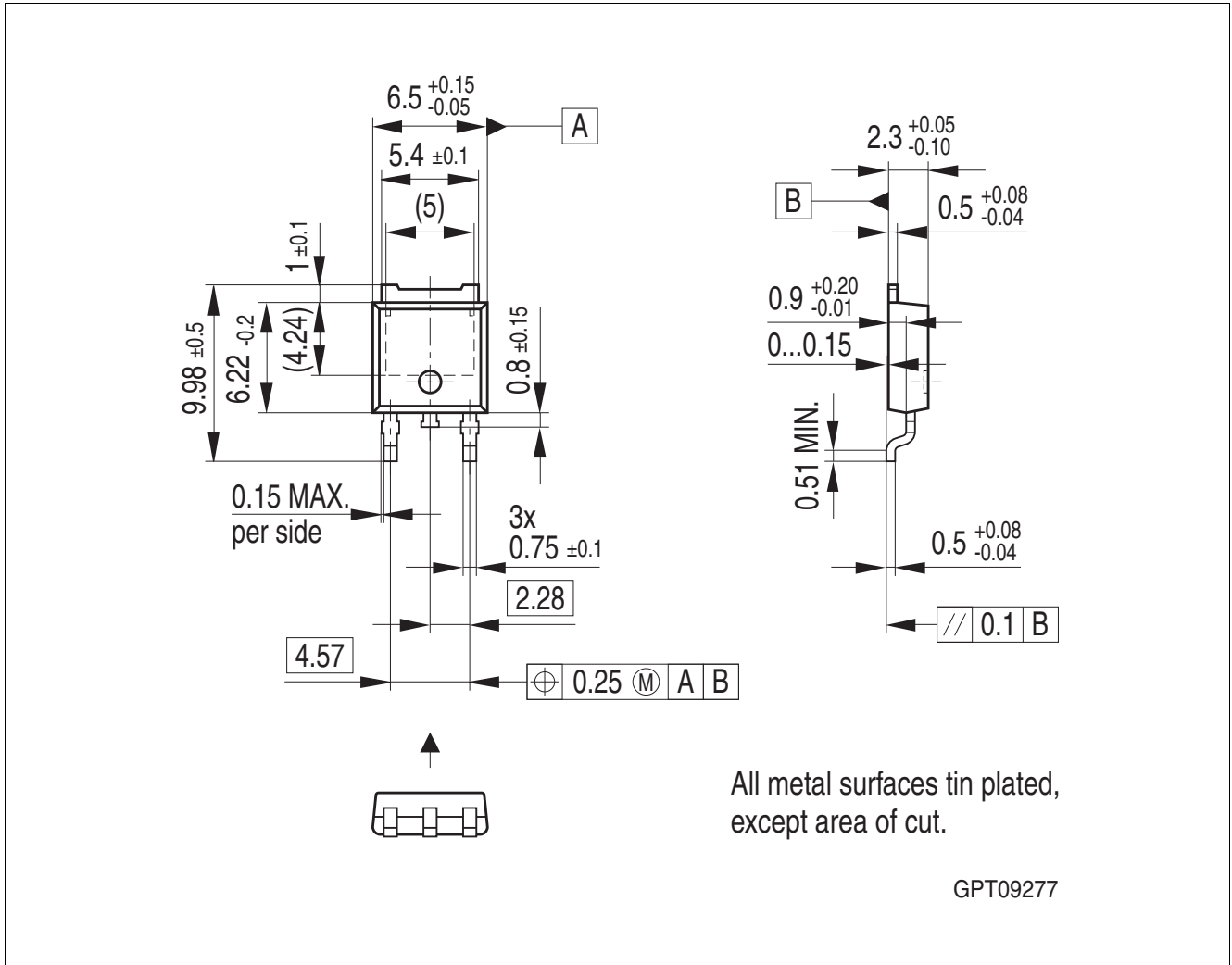


Figure 5 PG-T0252-3

## 8 Revision History

| Revision | Date       | Changes                      |
|----------|------------|------------------------------|
| 1.0      | 2014-01-28 | Data Sheet - Initial version |

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