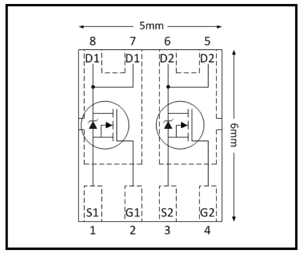
Features
- Advanced Process Technology
- Dual N-Channel MOSFET
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

V_{DSS}		40V
$R_{DS(on)}$	typ.	4.8mΩ
	max	5.9mΩ
I_D (Silicon Limited)		70A ⑩
I_D (Package Limited)		50A

Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast swithcing speed and improved repetitive avalanche rating. These features combine to make this product an extremely efficient and reliable device for use in Automotive and wide variety of other applications.



DUAL PQFN 5X6 mm

G	D	S
Gate	Drain	Source

Applications
- 12V Automotive Systems
- Brushed DC Motor
- Braking
- Transmission

Base Part Number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFN8459	Dual PQFN 5mm x 6mm	Tape and Reel	4000	AUIRFN8459TR

Absolute Maximum Ratings
Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I_D @ $T_{C\,(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V ⑩	70	A
I_D @ $T_{C\,(Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V	50	
I_D @ $T_{C\,(Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V (Package Limited)	50	
I_{DM}	Pulsed Drain Current ①	320	
P_D @$T_{C\,(Bottom)}$ = 25°C	Power Dissipation	50	W
	Linear Derating Factor	0.33	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	66	mJ
E_{AS} (Tested)	Single Pulse Avalanche Energy ⑨	110	
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E_{AR}	Repetitive Avalanche Energy ①		
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C

HEXFET® is a registered trademark of International Rectifier.

*Qualification standards can be found at http://www.irf.com/

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ⑧	——	3.0	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ⑧	——	45	
$R_{\theta JA}$	Junction-to-Ambient ⑦	——	40	

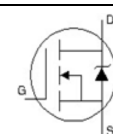
Static Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.037	——	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	4.8	5.9	mΩ	V_{GS} = 10V, I_D = 40A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	V_{DS} = V_{GS}, I_D = 50μA
gfs	Forward Transconductance	66	——	——	S	V_{DS} = 10V, I_D = 40A
R_G	Internal Gate Resistance	——	1.9	——	Ω	
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 40V, V_{GS} = 0V
		——	——	150		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
Q_g	Total Gate Charge	——	40	60	nC	I_D = 40A
Q_{gs}	Gate-to-Source Charge	——	13	——		V_{DS} = 20V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	14	——		V_{GS} = 10V
Q_{sync}	Total Gate Charge Sync. (Q_g - Q_{gd})	——	26	——		I_D = 40A, V_{DS} =0V, V_{GS} = 10V
$t_{d(on)}$	Turn-On Delay Time	——	10	——	ns	V_{DD} = 26V
t_r	Rise Time	——	55	——		I_D = 40A
$t_{d(off)}$	Turn-Off Delay Time	——	25	——		R_G = 2.7Ω
t_f	Fall Time	——	42	——		V_{GS} = 10V
C_{iss}	Input Capacitance	——	2250	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	340	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	215	——		f = 1.0 MHz
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	——	400	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑥
C_{oss} eff. (TR)	Effective Output Capacitance (Time Related)	——	490	——		V_{GS} = 0V, V_{DS} = 0V to 32V ⑤

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	70⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ②	——	——	320	A	
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 40A, V_{GS} = 0V ④
dv/dt	Peak Diode Recovery ③	——	7.0	——	V/ns	T_J = 175°C, I_S= 40A, V_{DS} = 40V
t_{rr}	Reverse Recovery Time	——	22	——	ns	T_J = 25°C; V_R = 34V, I_F = 40A, di/dt = 100A/μs ④
		——	23	——		T_J = 125°C
Q_{rr}	Reverse Recovery Charge	——	17	——	nC	T_J = 25°C
		——	17	——		T_J = 125°C
I_{RRM}	Reverse Recovery Current	——	1.0	——	A	T_J = 25°C

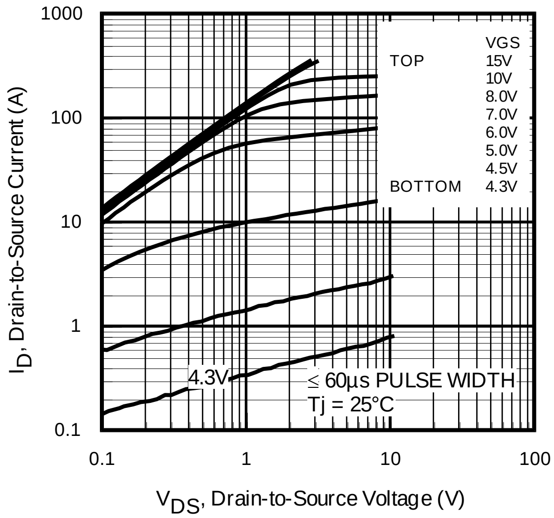


Fig. 1 Typical Output Characteristics

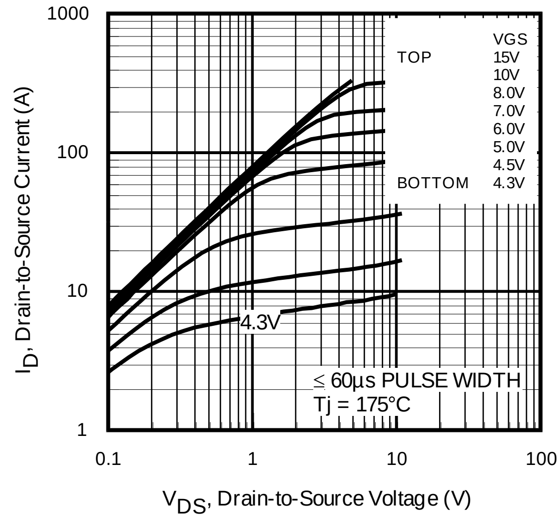


Fig. 2 Typical Output Characteristics

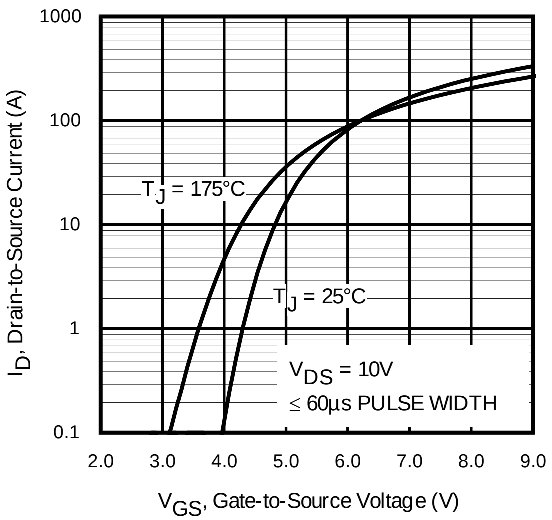


Fig. 3 Typical Transfer Characteristics

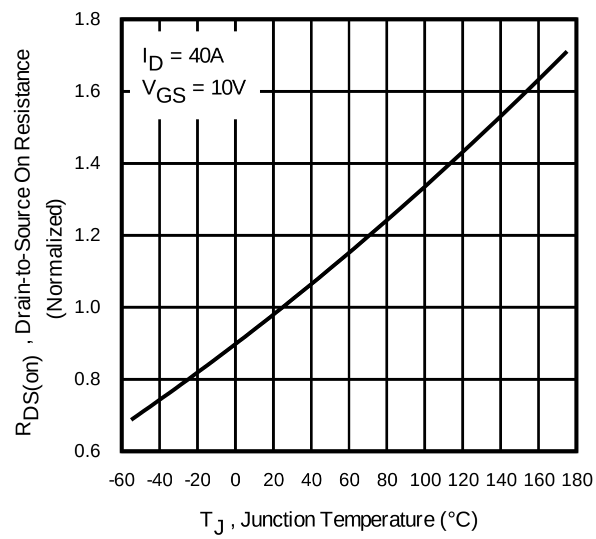


Fig. 4 Normalized On-Resistance vs. Temperature

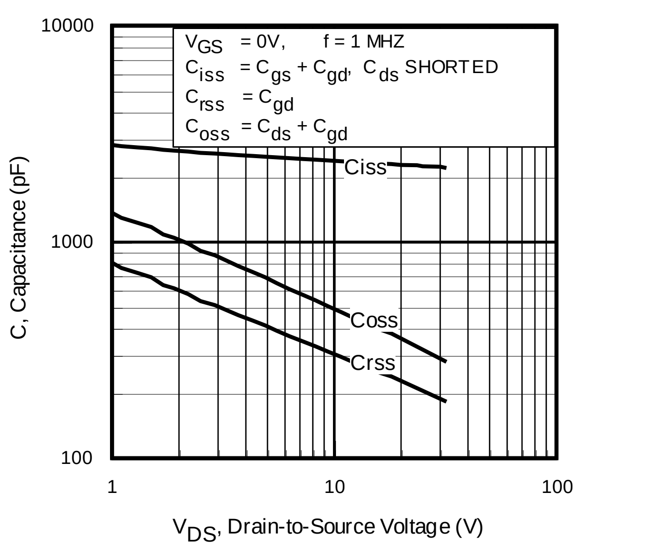


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

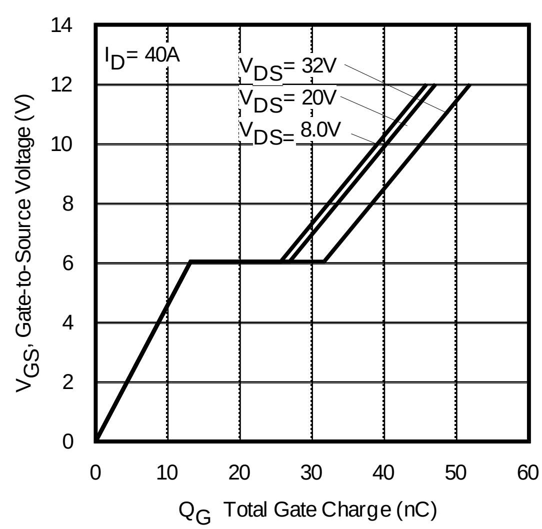


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

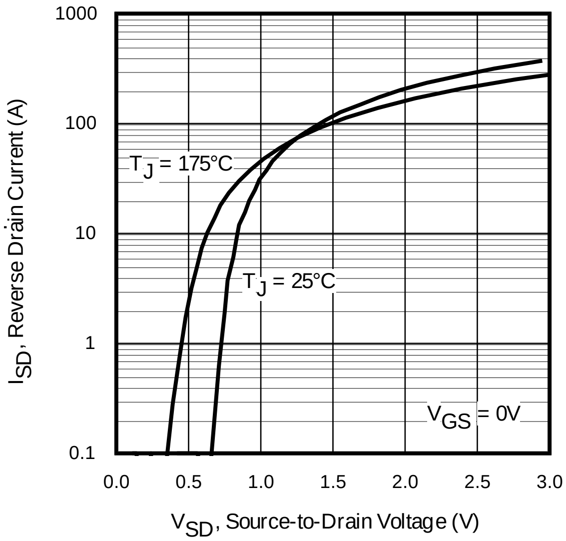


Fig. 7 Typical Source-to-Drain Diode

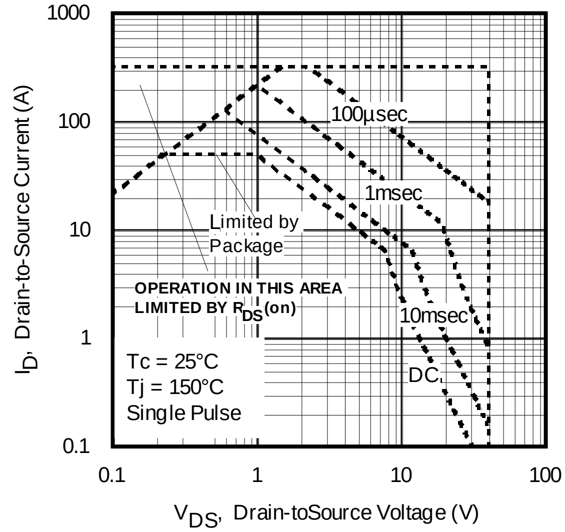


Fig 8. Maximum Safe Operating Area

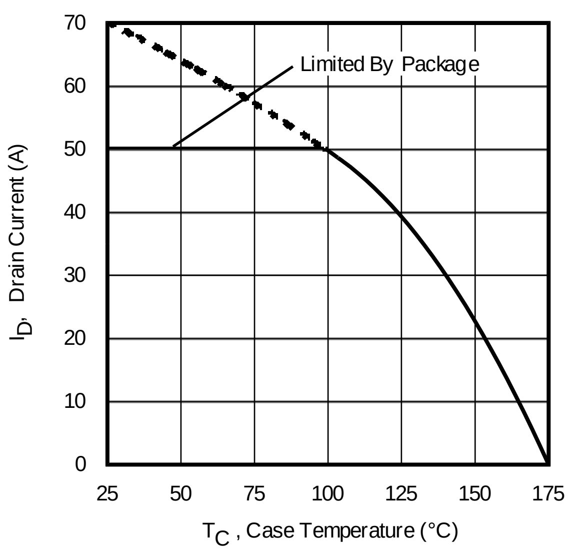


Fig 9. Maximum Drain Current vs. Case Temperature

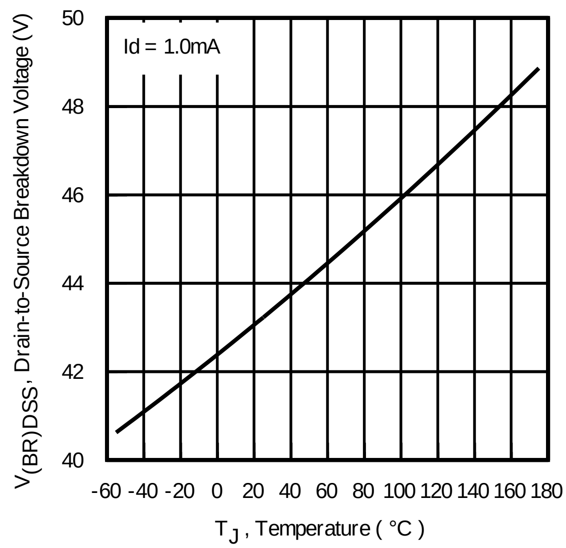


Fig 10. Drain-to–Source Breakdown Voltage

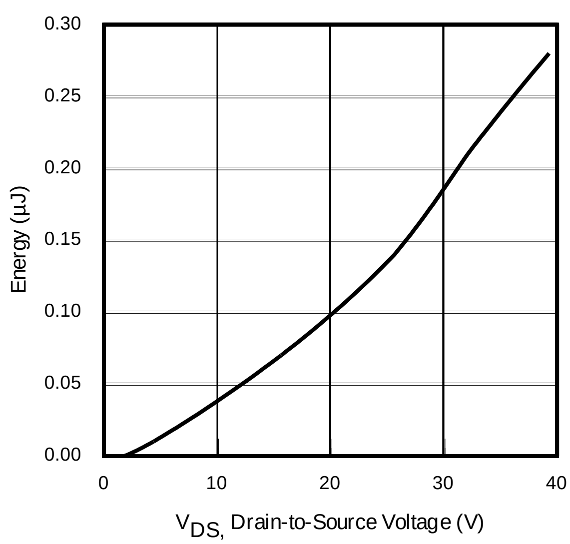


Fig 11. Typical C_{oss} Stored Energy

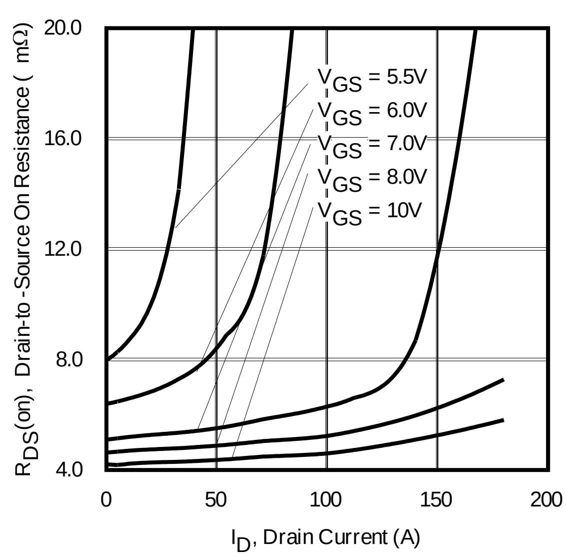


Fig 12. Typical On-Resistance vs. Drain Current

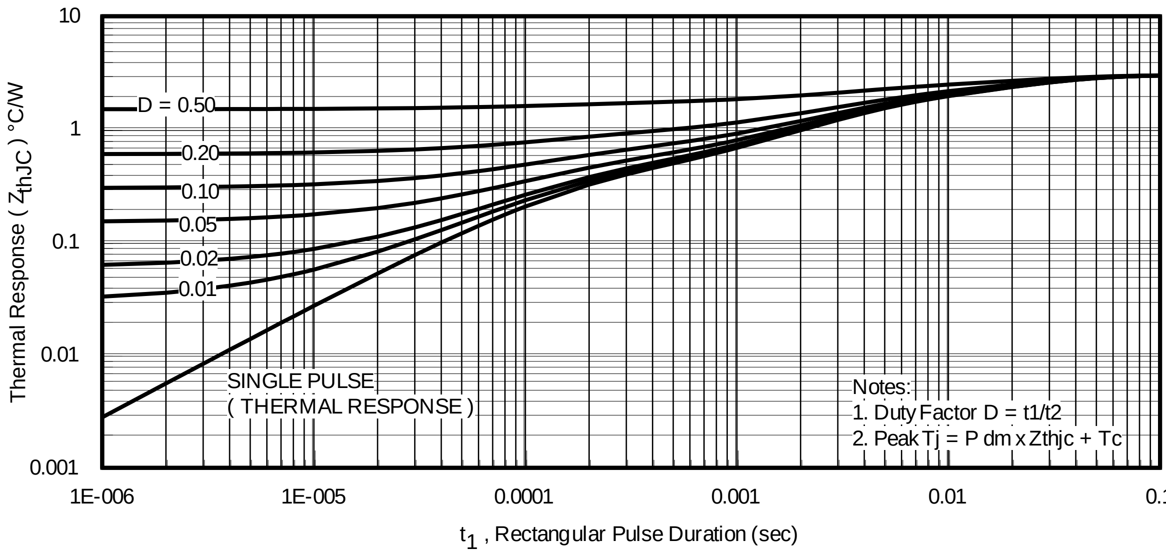


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

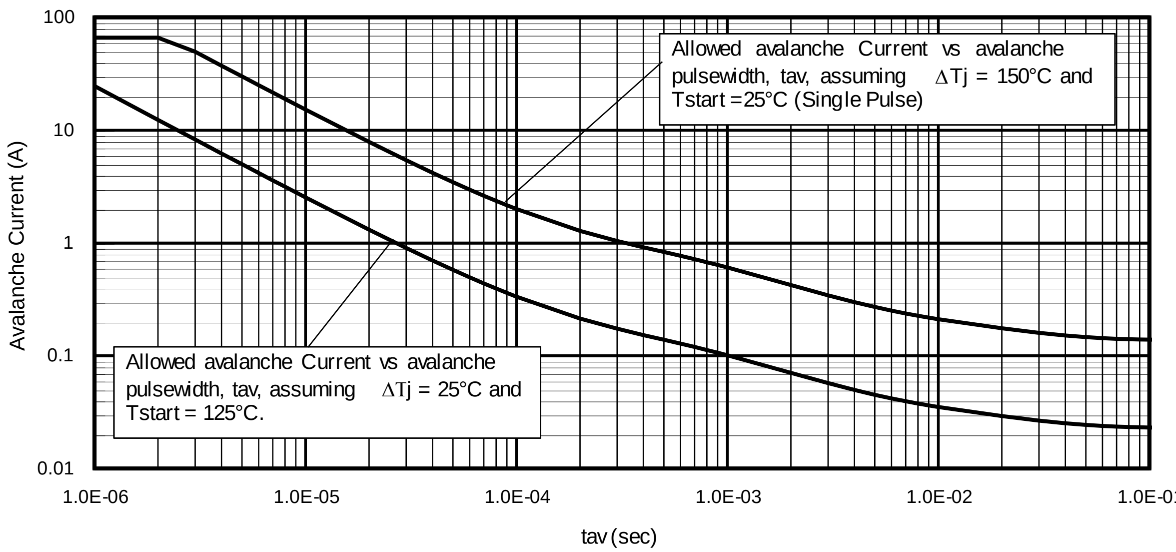


Fig 14. Avalanche Current vs. Pulse Width Current

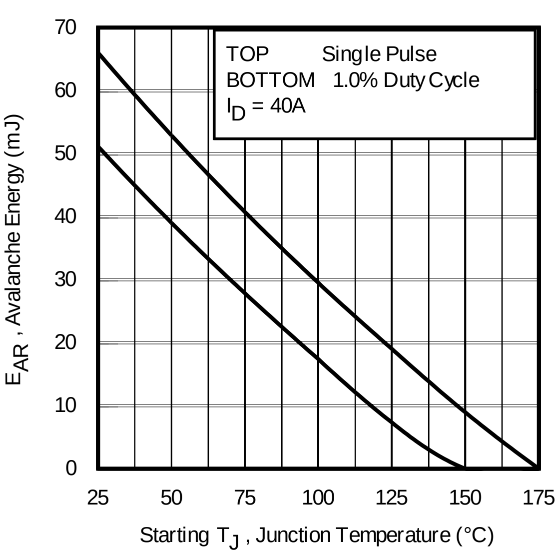


Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1.Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 22a, 22b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
t_{av} = Average time in avalanche.
D = Duty cycle in avalanche = $t_{av} \cdot f$
$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$PD\ (ave) = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\ (AR)} = P_{D\ (ave)} \cdot t_{av}$$

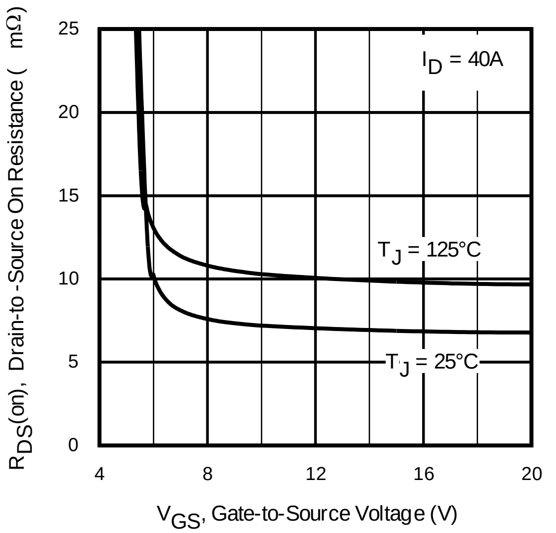


Fig 16. Typical On-Resistance vs. Gate Voltage

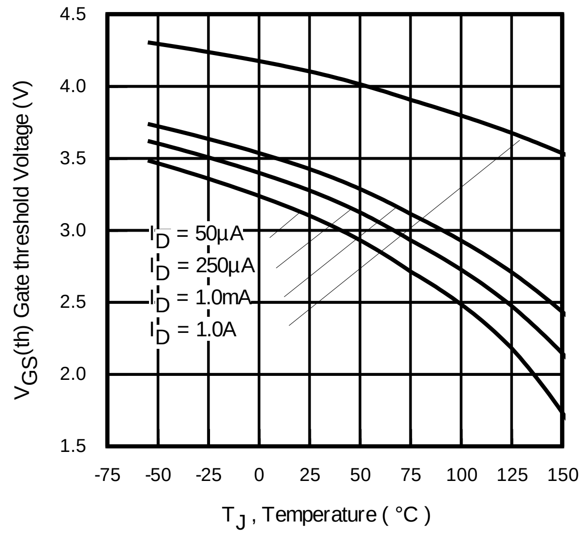


Fig 17. Threshold Voltage vs. Temperature

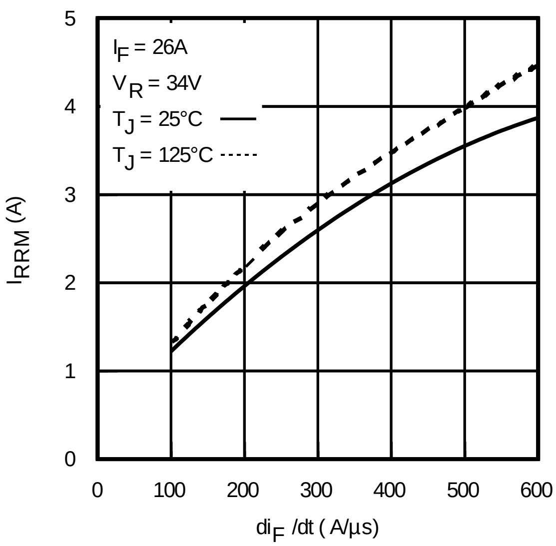


Fig 18. Typical Recovery Current vs. dif/dt

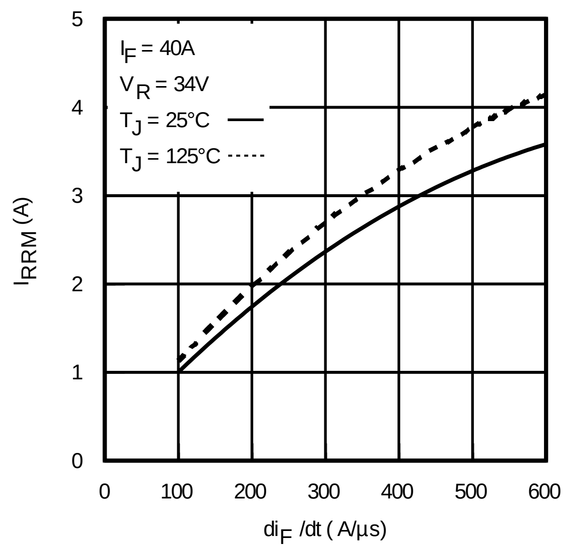


Fig 19. Typical Stored Charge vs. dif/dt

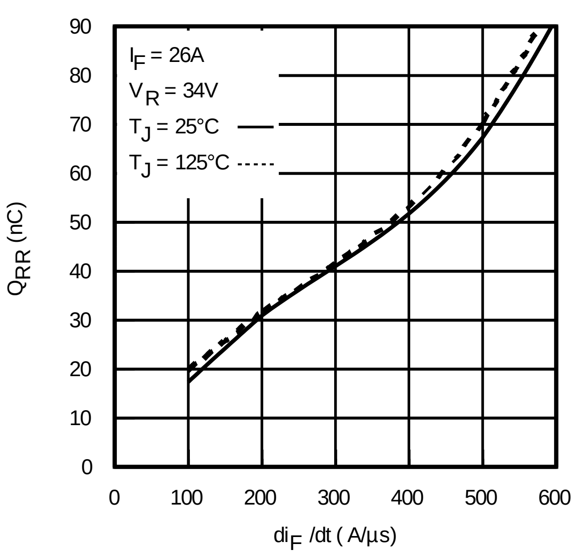


Fig 20. Typical Recovery Current vs. dif/dt

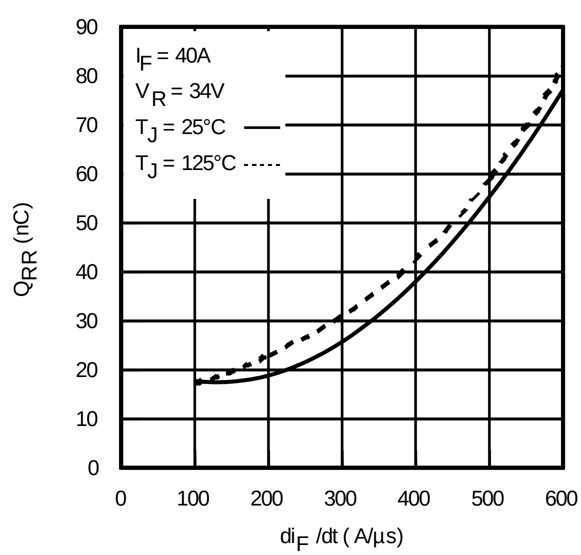


Fig 21. Typical Stored Charge vs. dif/dt

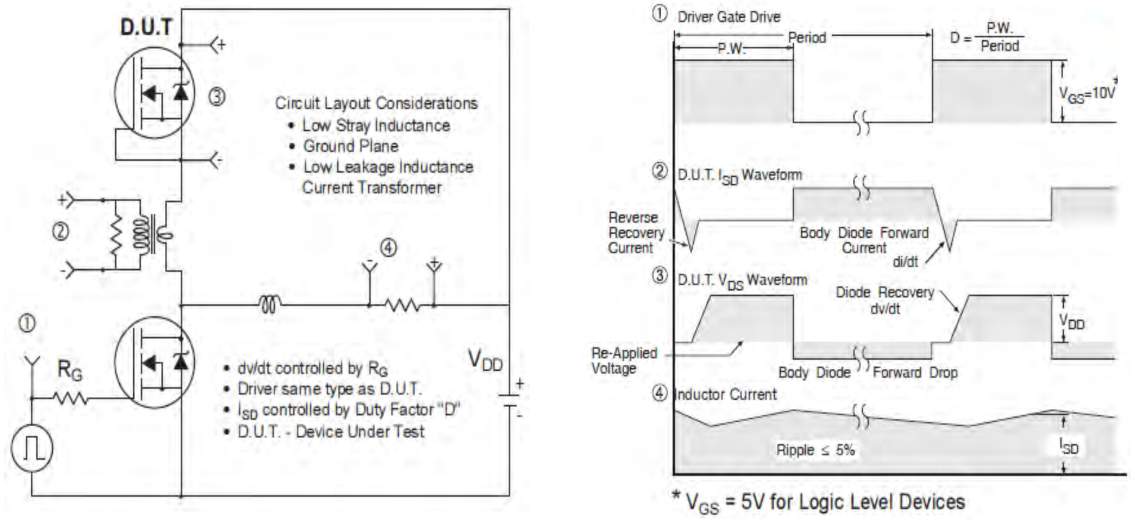


Fig 22. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

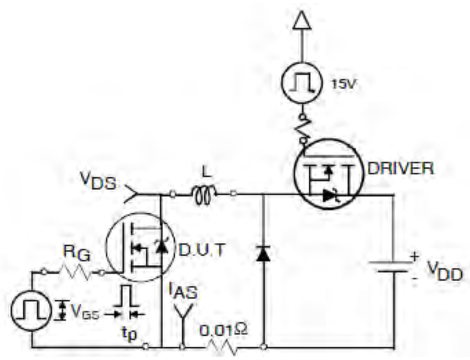


Fig 22a. Unclamped Inductive Test Circuit

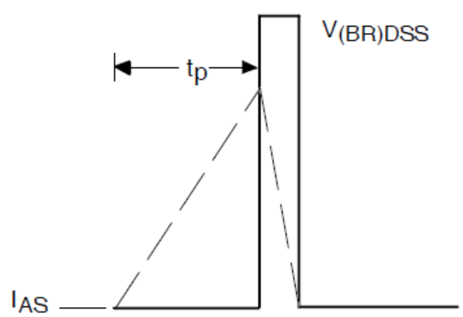


Fig 22b. Unclamped Inductive Waveforms

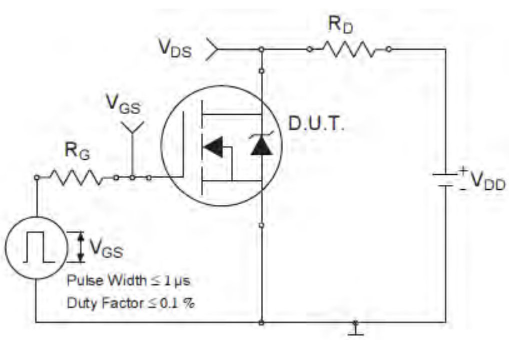


Fig 23a. Switching Time Test Circuit

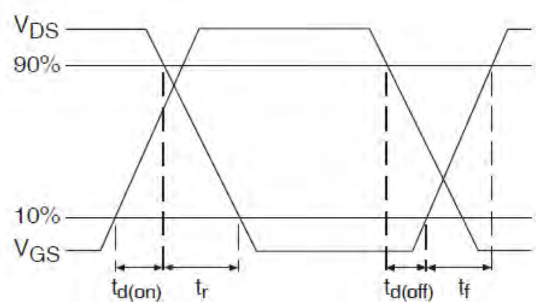


Fig 23b. Switching Time Waveforms

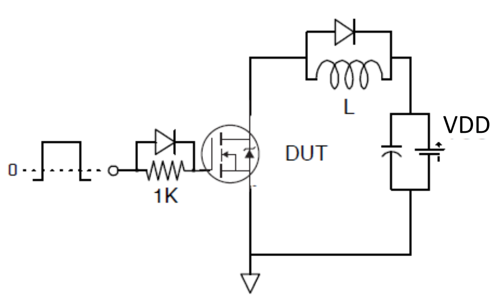


Fig 24a. Gate Charge Test Circuit

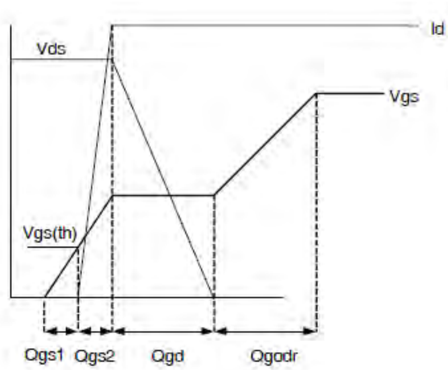
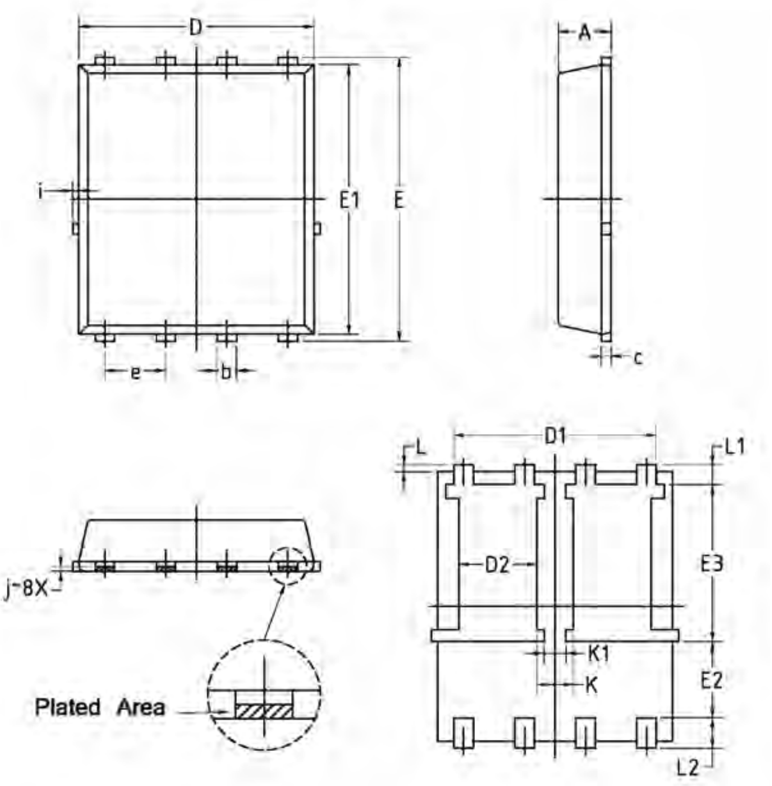


Fig 24b. Gate Charge Waveform

Dual PQFN 5x6 Package Details



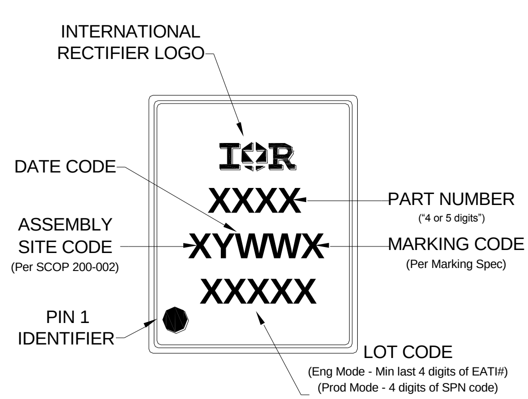
SYMBOL	COMMON			
	MM		INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.00	1.20	0.039	0.047
b	0.30	0.50	0.012	0.020
c	0.203 BSC		0.008 BSC	
D	4.80	5.00	0.189	0.197
D1	4.06	4.36	0.160	0.172
D2	1.47	1.77	0.058	0.070
E	5.90	6.20	0.232	0.244
E1	5.65	5.85	0.222	0.230
E2	1.45	—	0.057	—
E3	3.20	3.50	0.126	0.138
e	1.27 BSC		0.05 BSC	
L	0.05	0.25	0.002	0.010
L1	0.325	0.525	0.013	0.021
L2	0.500	0.800	0.020	0.031
i	—	0.20	—	0.008
K	0.61	0.91	0.024	0.036
K1	0.31	0.60	0.012	0.024
j	0.1015 BSC		0.004BSC	

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf

For more information on package inspection techniques, please refer to application note AN-1154:

http://www.irf.com/technical-info/appnotes/an-1154.pdf

Dual PQFN 5x6 Part Marking



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		Dual PQFN 5mm x 6mm	MSL1
ESD	Human Body Model	Class H1B(+/- 1000V)††	
		AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1000V)††	
		AEC-Q101-005	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site: http//www.irf.com/

†† Highest passing voltage.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J = 25°C, L =75µH, R_G = 50Ω, I_{AS} = 40A, V_{GS} = 10V.

③ $I_{SD} \leq$ 50A, di/dt $\leq$ 650A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq$ 175°C.

④ Pulse width $\leq$ 400µs; duty cycle $\leq$ 2%.

⑤ $C_{oss\ eff.\ (TR)}$ is a fixed capacitance that gives the same charging time as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ $C_{oss\ eff.\ (ER)}$ is a fixed capacitance that gives the same energy as Coss while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994: http://www.irf.com/technical-info/appnotes/an-994.pdf

⑧ R_θ is measured at T_J of approximately 90°C.

⑨ This value determined from sample failure population, starting T_J = 25°C, L= 75µH, R_G = 50Ω, I_{AS} = 40A, V_{GS} =10V.

⑩ Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 50A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements

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http://www.irf.com/technical-info/

WORLD HEADQUARTERS:

101 N. Sepulveda Blvd., El Segundo, California 90245

Tel: (310) 252-7105