

Protection Device

TVS (Transient Voltage Suppressor)

ESD221-U1-02EL

Uni-directional, 5.3 V, 38 pF, 0402, RoHS and Halogen Free compliant

ESD221-U1-02EL

Data Sheet

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Final

Power Management & Multimarket

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1 Product Overview

1.1 Features

- ESD / transient protection of data and V_{BUS} lines according to:
 - IEC61000-4-2 (ESD): ± 25 kV (air) ± 20 kV (contact)
 - IEC61000-4-4 (EFT): ± 2.5 kV / ± 50 A (5/50 ns)
 - IEC61000-4-5 (Surge): ± 5.5 A (8/20 μ s)
- Uni-directional, working voltage up to $V_{RWM} = \pm 5.3$ V
- Medium capacitance: $C_L = 38$ pF (typical)
- Very low clamping voltage $V_{CL} = +10 / -5$ V (typical) at $I_{TLP} = 16$ A
- Low reverse current $I_R < 100$ nA at $V_R = 3.3$ V
- Pb-free (RoHS compliant) and halogen free package



1.2 Application Examples

- V_{BUS} line protection in USB ports
- Keypad, touchpad, buttons, convenience keys
- LCD displays, Camera, audio lines, mobile communication, Consumer products (E-Book, MP3, DVD, DSC...)
- Notebooks tablets and desktop computers and their peripherals

1.3 Product Description

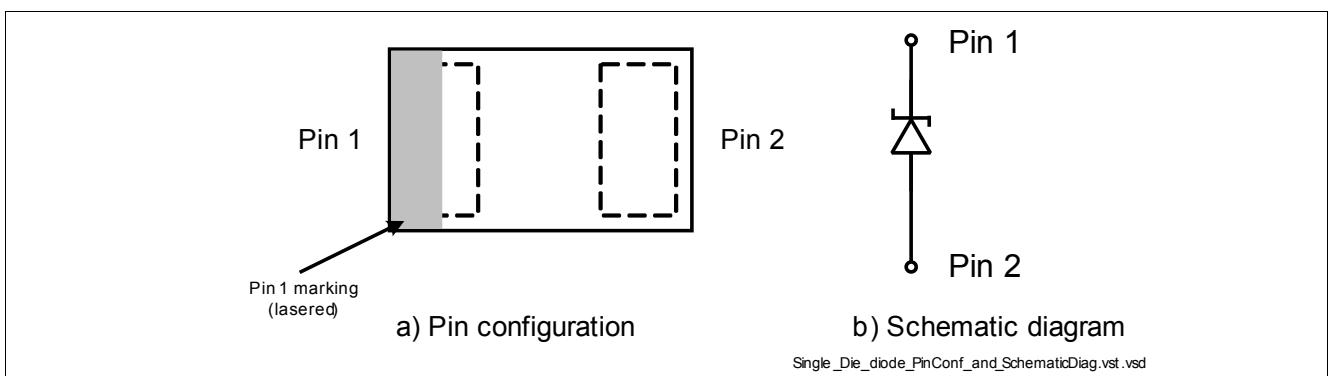


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD221-U1-02EL	TSLP-2-19	1 line, uni-directional	E

2 Maximum Ratings

Table 2-1 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values	Unit
ESD air discharge ¹⁾	V_{ESD}	± 25	kV
ESD contact discharge ¹⁾		± 20	
Peak pulse power ²⁾	P_{PK}	60	W
Peak pulse current ²⁾	I_{PP}	± 5.5	A
Operating temperature range	T_{OP}	-55 to 125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2

2) Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

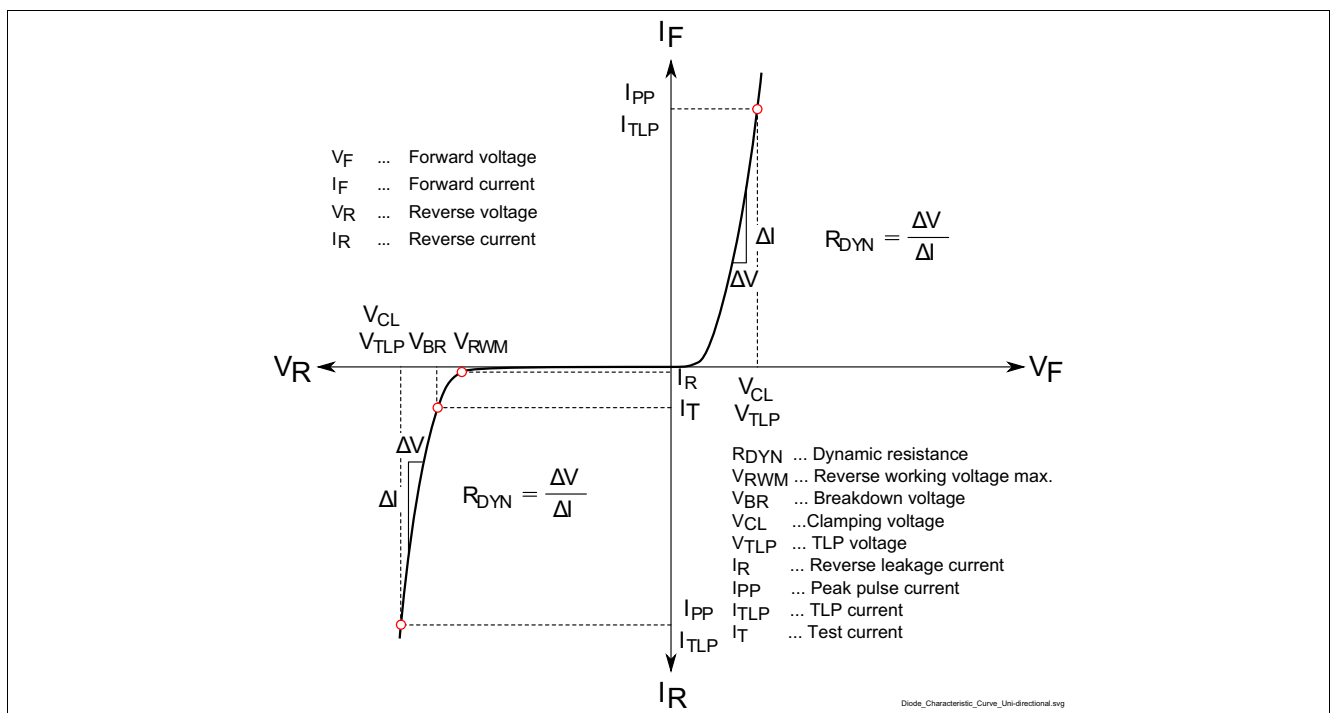


Figure 3-1 Definitions of electrical characteristics

Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified
Table 3-1 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	5.3	V	from Pin 1 to Pin 2
Breakdown voltage	V_{BR}	5.7	6.4	7.5	V	$I_T = 1\text{ mA}$
Reverse current	I_R	–	–	100	nA	$V_R = 3.3\text{ V}$

Table 3-2 AC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	38	–	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
		–	20	–		$V_R = 2.5\text{ V}, f = 1\text{ MHz}$
Series inductance	L_S	–	0.4	–	nH	

Table 3-3 ESD and Surge Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ¹⁾	V_{CL}	–	10	–	V	$I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$, Pin 1 to Pin 2
		–	14	–		$I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$, Pin 1 to Pin 2
		–	5	–		$I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$, Pin 2 to Pin 1
		–	7	–		$I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$, Pin 2 to Pin 1
Clamping voltage ²⁾	V_{CL}	–	7	9		$I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin 1 to Pin 2
		–	8	10		$I_{PP} = 3.5\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin 1 to Pin 2
		–	9	11		$I_{PP} = 5.5\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin 1 to Pin 2
		–	1.2	2		$I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin 2 to Pin 1
		–	2	3		$I_{PP} = 3.5\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin 2 to Pin 1
		–	2.5	3.5		$I_{PP} = 5.5\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin 2 to Pin 1
		–	–	–		$I_{PP} = 5.5\text{ A}, t_p = 8/20\text{ }\mu\text{s}$, Pin 2 to Pin 1
Dynamic resistance ¹⁾	R_{DYN}	–	0.3	–	Ω	$t_p = 100\text{ ns}$

 1) Please refer to Application Note AN210[1] TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$.

 2) Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_A = 25^\circ\text{C}$, unless otherwise specified

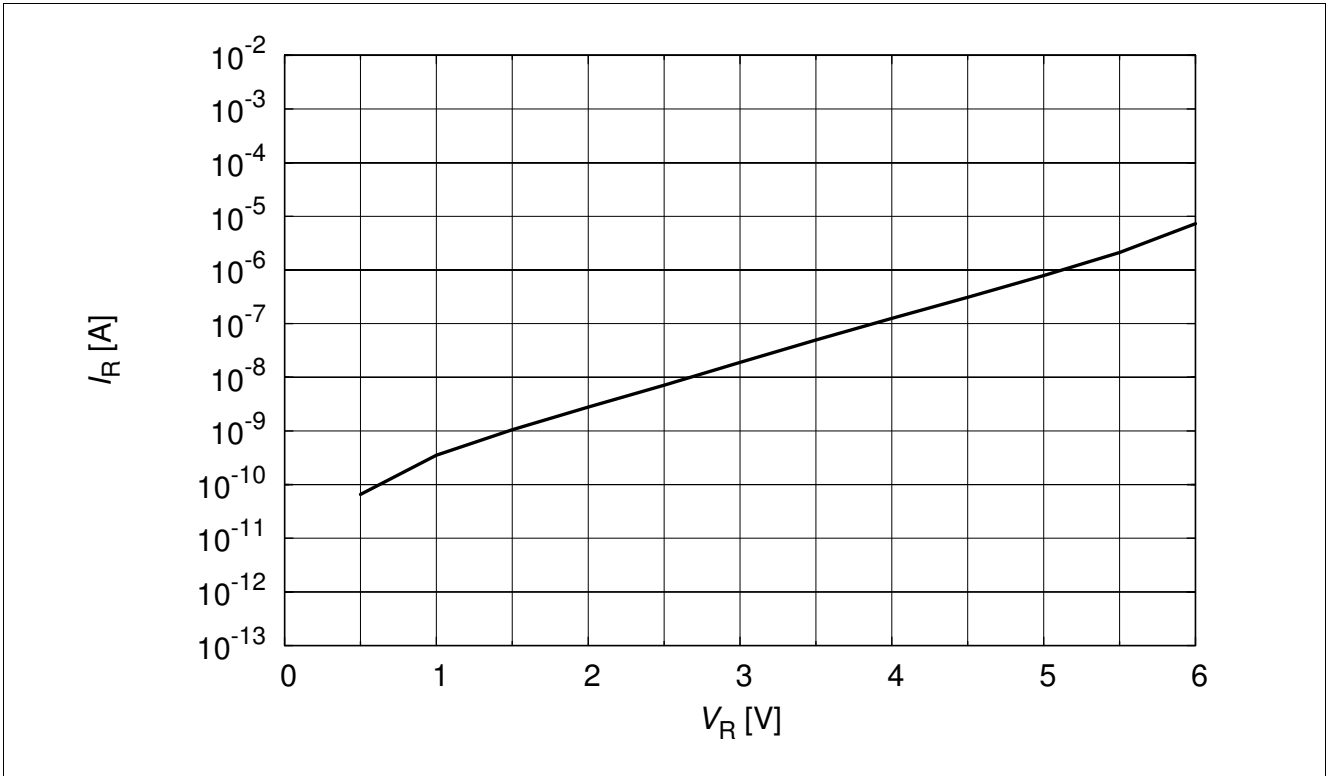


Figure 4-1 Reverse leakage current: $I_R = f(V_R)$

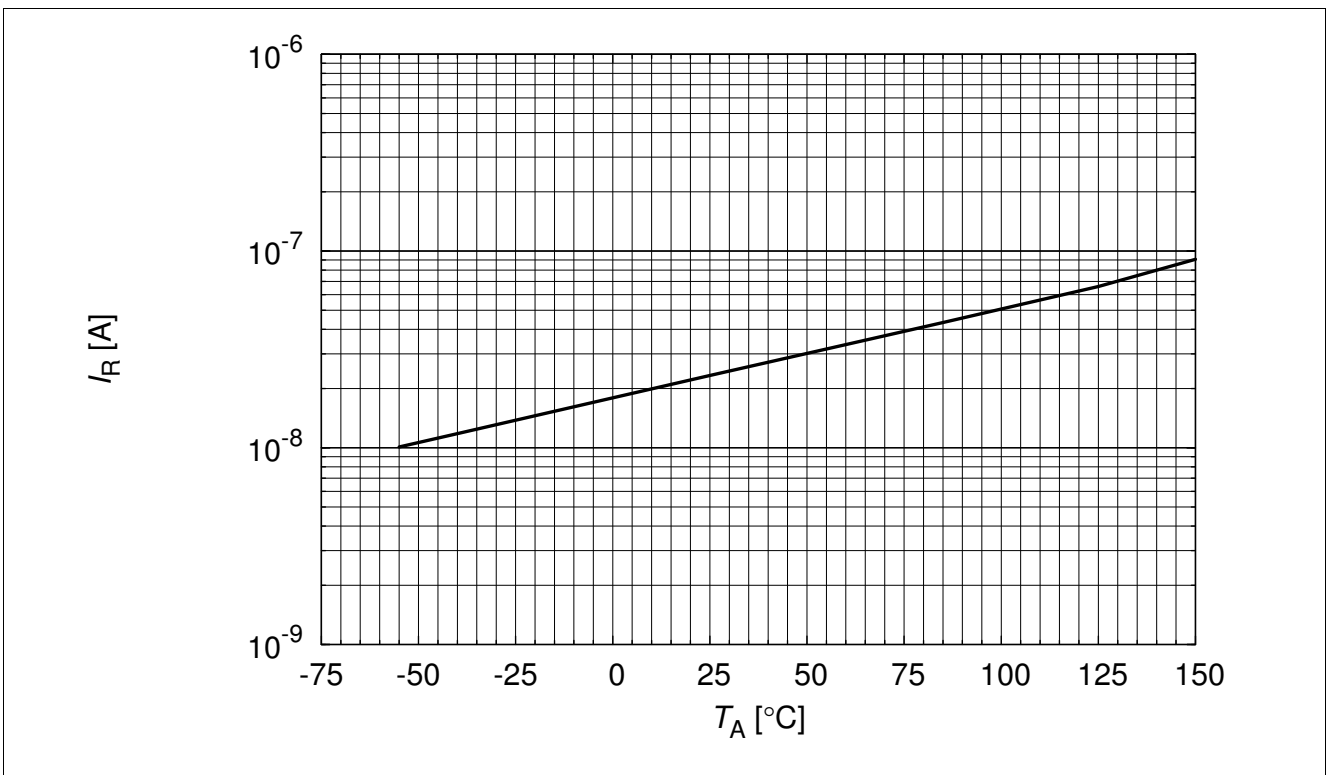


Figure 4-2 Reverse leakage current: $I_R = f(T_A)$, $V_R = 3.3\text{ V}$

Typical Characteristics Diagrams

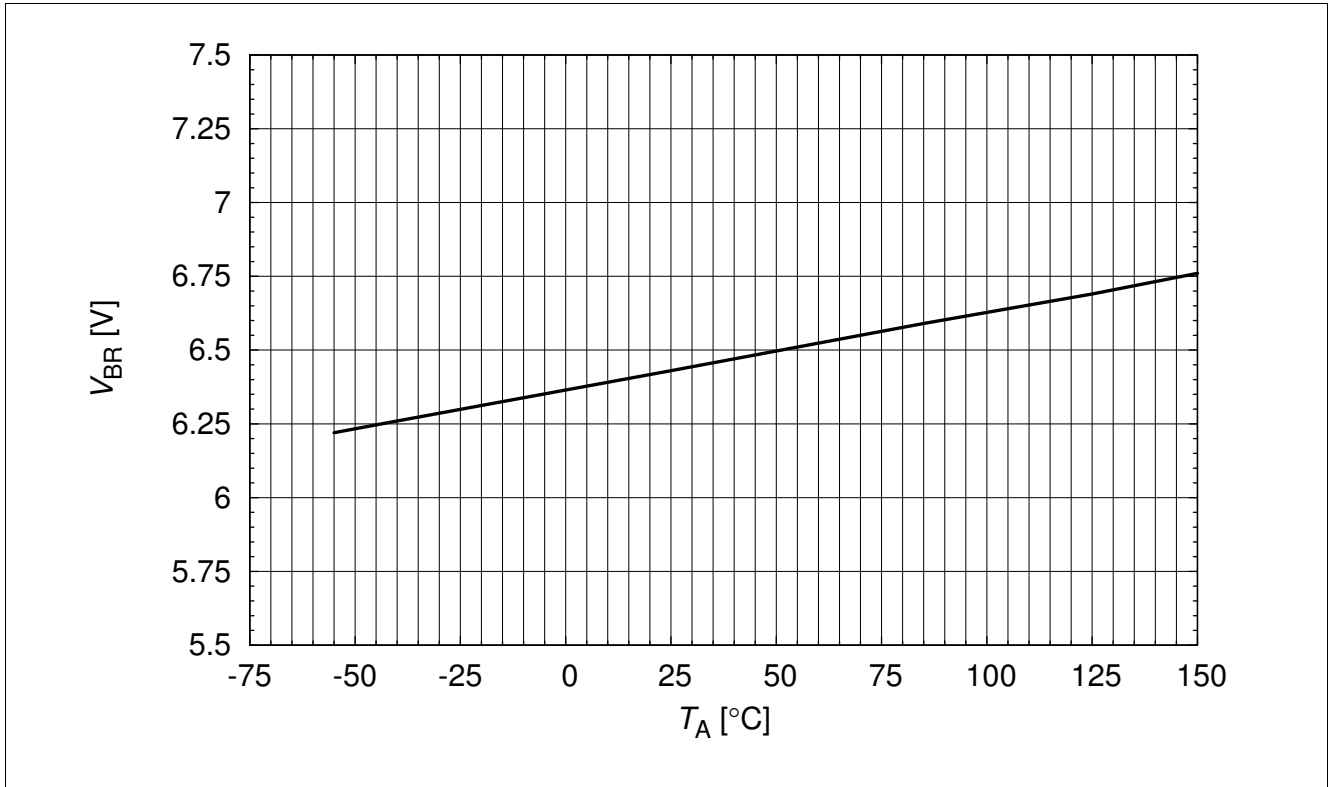


Figure 4-3 Breakdown voltage: $V_{BR} = f(T_A)$, $I_R = 1 \text{ mA}$

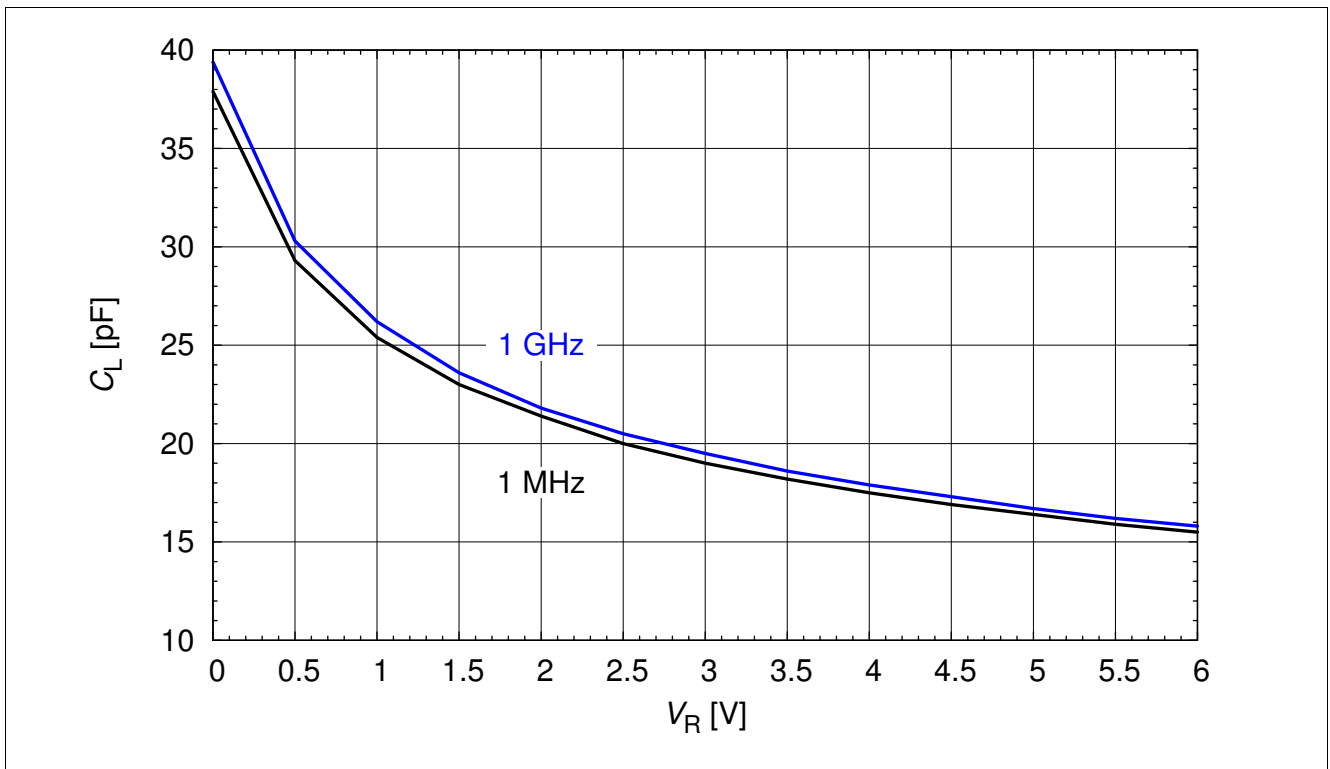


Figure 4-4 Line capacitance: $C_L = f(V_R)$

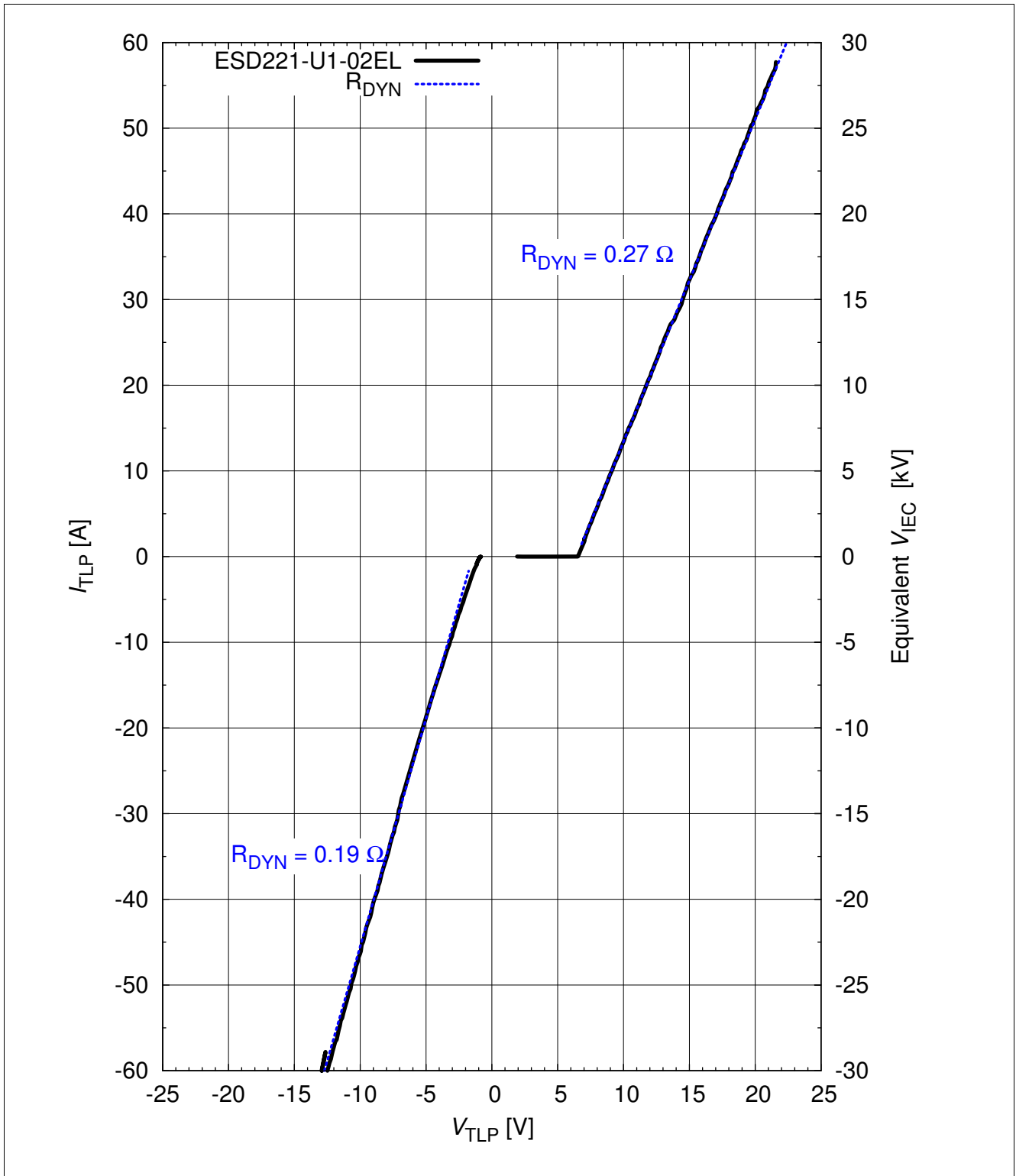


Figure 4-5 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

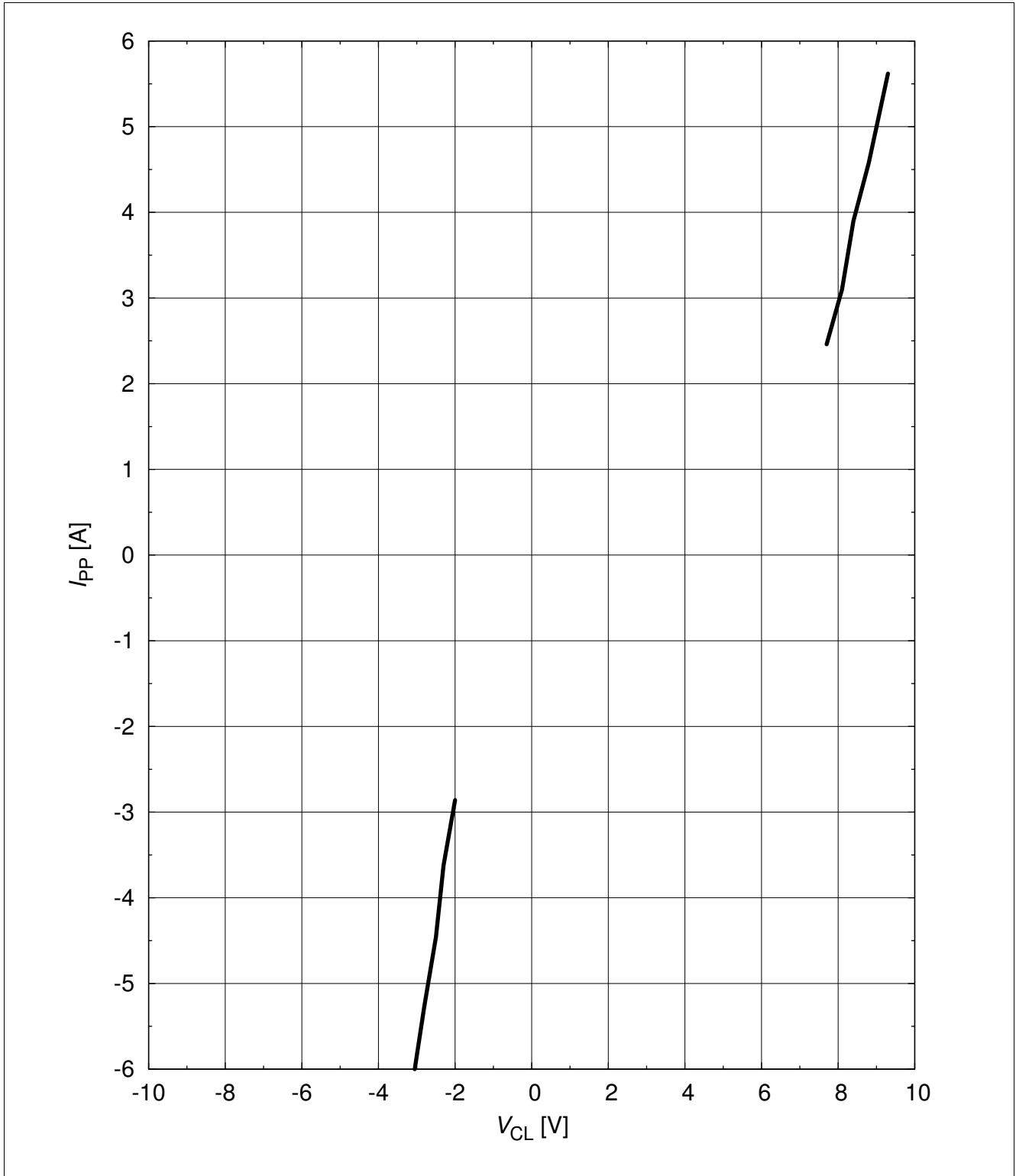


Figure 4-6 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ [1], pin 1 to pin 2

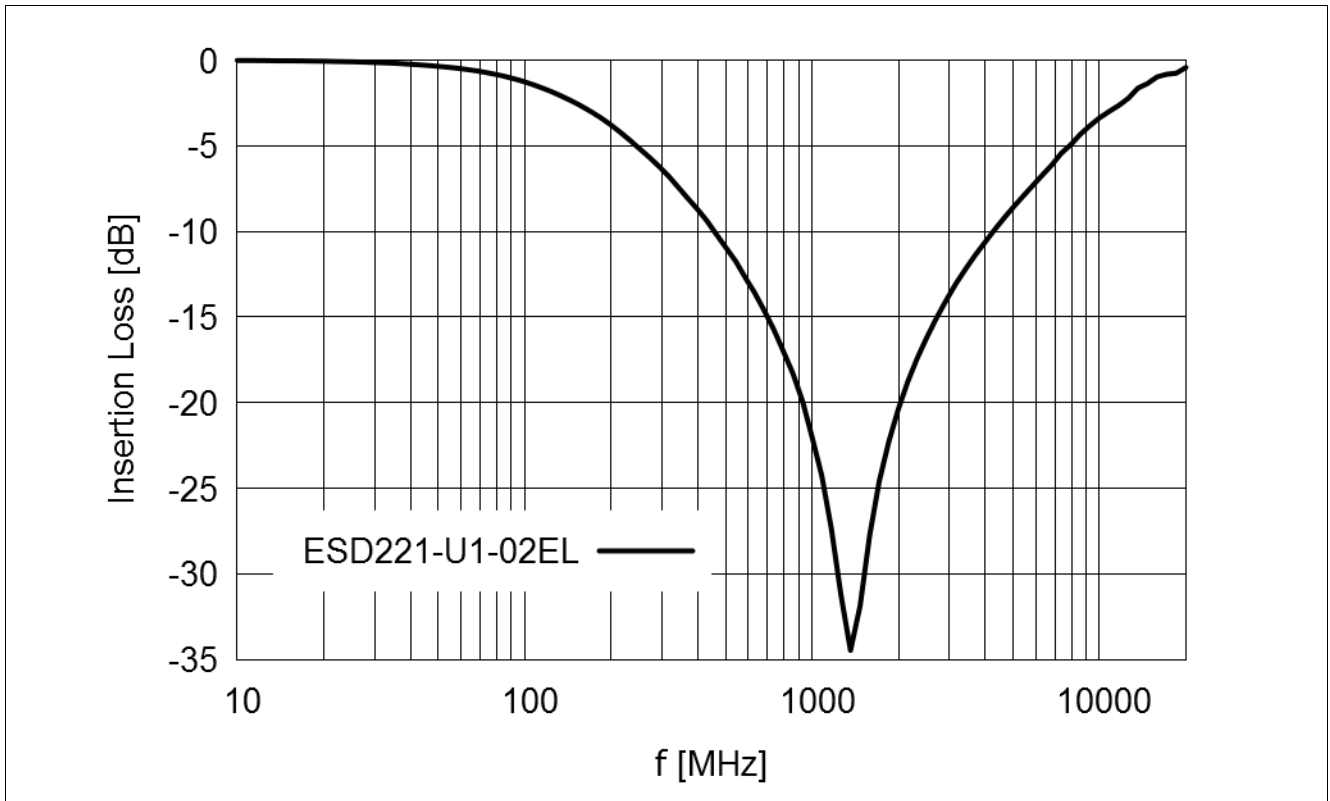


Figure 4-7 Insertion loss vs. frequency in a 50 Ω system

5 Package Information

5.1 TSLP-2-19

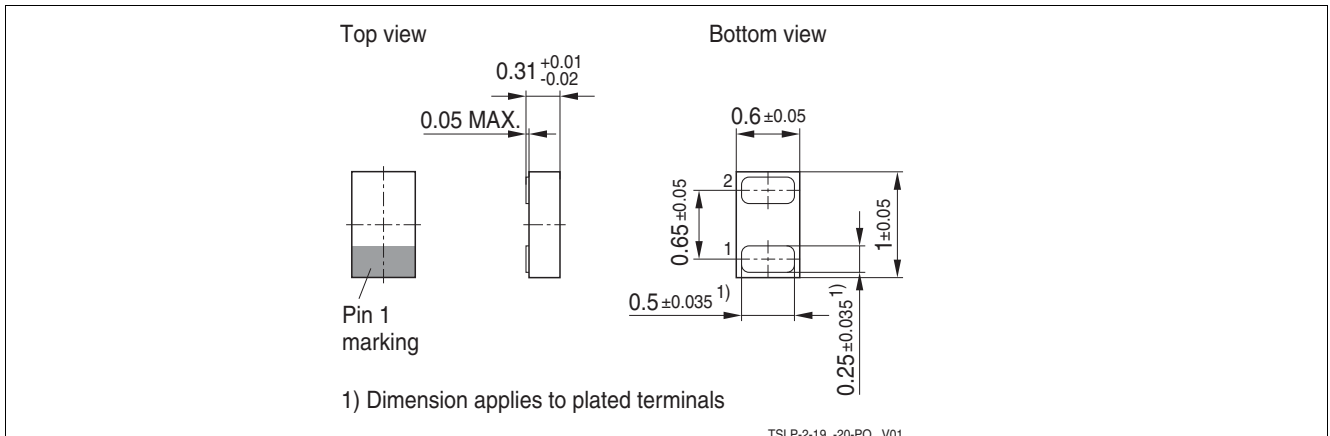


Figure 5-1 TSLP-2-19: Package outline

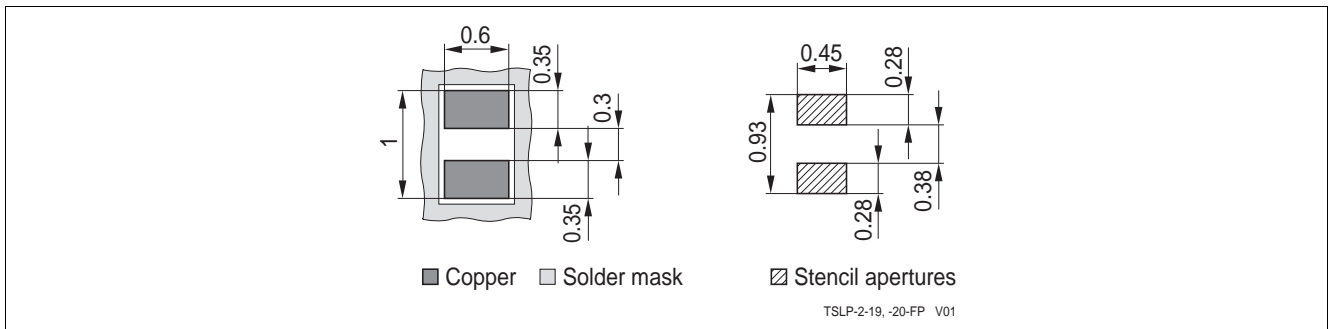


Figure 5-2 TSLP-2-19: Footprint

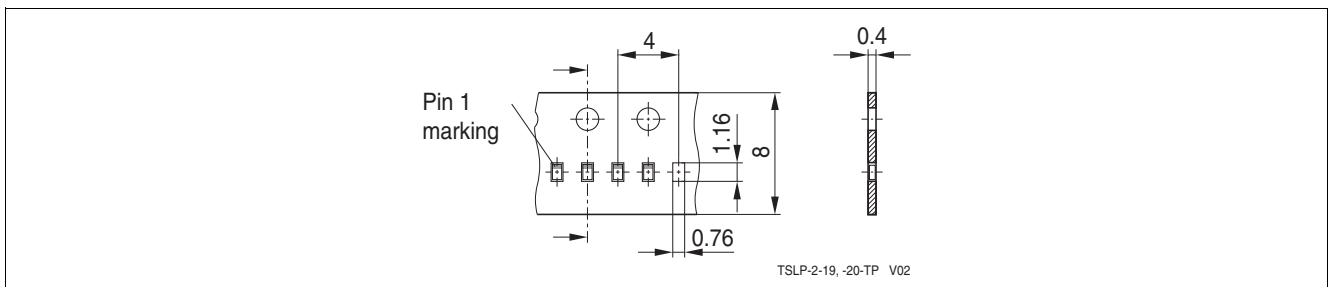


Figure 5-3 TSLP-2-19: Packing

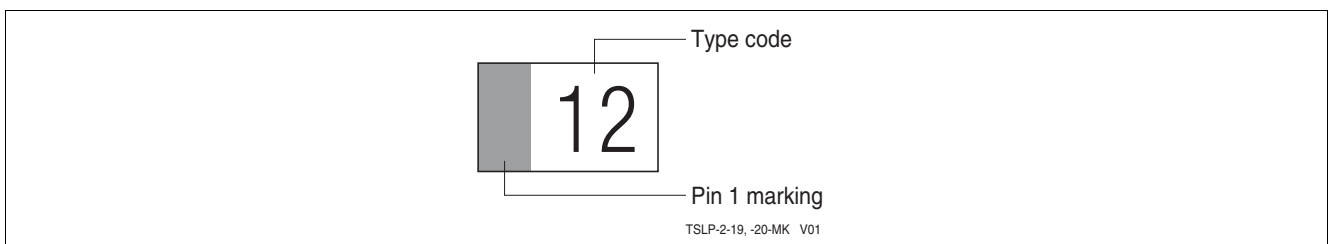


Figure 5-4 TSLP-2-19: Marking example, Type code see: [Table 1-1 "Part Information" on Page 3](#)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages

Revision History

Page or Item	Subjects (major changes since previous revision)
Revision 1.0, 2014-05-20	
5	Update of Table 2-2)

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