

OptiMOS™3 Power MOS Transistor Chip

Type	$V_{(BR)DSS}$	$R_{DS(on)}$	Die size	Thickness
IPC313N10N3R	100 V	2.7 mΩ ¹⁾	6 * 5.2 mm ²	220 μm

DESCRIPTION

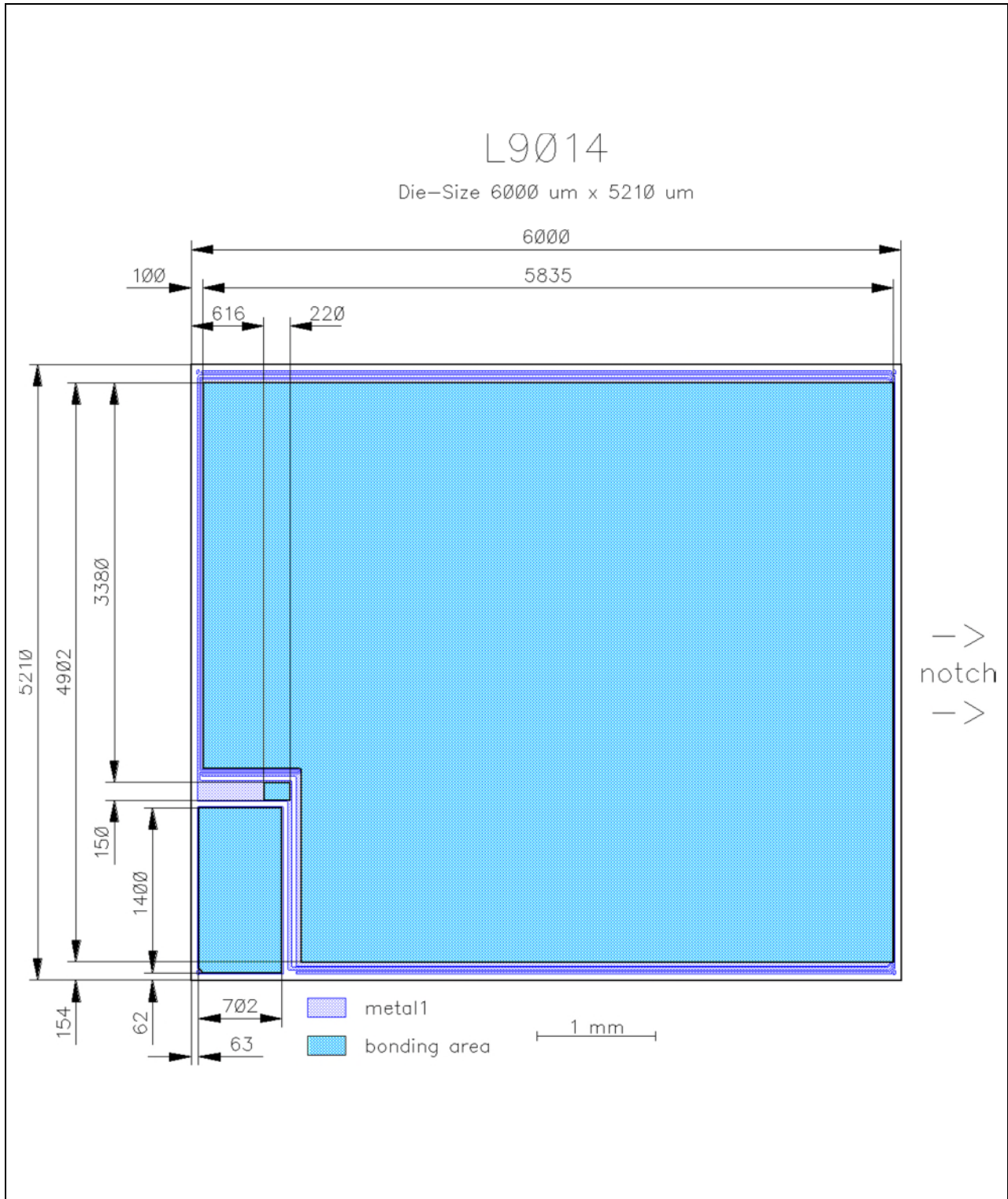
- N-channel enhancement mode
- For dynamic characterization refer to the datasheet of IPB027N10N3 G²⁾
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to JEDEC
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AlCu system
- Passivation: nitride (only on edge structure)

Electrical Characteristics on Wafer Level

at $T_j = 25\text{ °C}$, unless otherwise specified.

Parameter	Symbol	Value			Unit	Conditions
		min.	typ.	max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	2.7	3.5	V	$V_{DS} = V_{GS}$ $I_D = 275\text{ μA}$
Zero gate voltage drain current	I_{DSS}	-	0.1	1	μA	$V_{GS} = 0\text{ V}$ $V_{DS} = 100\text{ V}$
Gate-source leakage current	I_{GSS}	-	1	100	nA	$V_{GS} = 20\text{ V}$ $V_{DS} = 0\text{ V}$
Drain-source on-resistance	$R_{DS(on)}$	-	1.9 ³⁾	100 ⁴⁾	mΩ	$V_{GS} = 10\text{ V}$ $I_D = 2.0\text{ A}$
Reverse diode forward on-voltage	V_{SD}	-	1.0	1.2	V	$V_{GS} = 0\text{ V}$ $I_F = 1\text{ A}$
Internal gate resistance	R_G	-	8	-	Ω	
Avalanche energy, single pulse	E_{AS}	-	45 ⁵⁾	-	mJ	$I_D = 30\text{ A}$, $R_{GS} = 25\text{ Ω}$

Chip-Layout:



¹⁾ packaged in a P-TO263-3 (see ref. product)

²⁾ IPB027N10N3 G dynamic characterization does not include the internal added R_G

³⁾ typical bare die $R_{DS(on)}$; $V_{GS}=10V$

⁴⁾ limited by wafer test-equipment

⁵⁾ Wafer tested. For general avalanche capability refer to the datasheet of IPB027N10N3 G



IPC313N10N3R

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