

# MOSFET

## OptiMOS™ 5 Linear FET, 150 V

### Features

- Ideal for hot-swap and e-fuse applications
- Very low on-resistance  $R_{DS(on)}$
- Wide safe operating area SOA
- N-channel, normal level
- 100% avalanche tested
- Pb-free plating; RoHS compliant
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Halogen-free according to IEC61249-2-21



**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS}$	150	V
$R_{DS(on),max}$	4.8	m $\Omega$
$I_D$ (silicon limited)	182	A
$I_D$ (package limited)	120	A
$I_{pulse}$ ( $V_{DS}=56$ V, $t_p=10$ ms)	10.8	A



Type / Ordering Code	Package	Marking	Related Links
IPB048N15N5LF	PG-TO 263-3	048N15LF	-

<sup>1)</sup> J-STD20 and JESD22

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## 1 Maximum ratings

at  $T_C=25\text{ °C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	120 115 18	A	$V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$ , $T_C=25\text{ °C}$ , $R_{thJA}=40\text{ K/W}^{(1)}$
Pulsed drain current <sup>(2)</sup>	$I_{D,pulse}$	-	-	480	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse <sup>(3)</sup>	$E_{AS}$	-	-	30	mJ	$I_D=40\text{ A}$ , $R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	-
Power dissipation	$P_{tot}$	-	-	313	W	$T_C=25\text{ °C}$
Operating and storage temperature	$T_j$ , $T_{stg}$	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	0.25	0.4	K/W	-
Device on PCB, minimal footprint	$R_{thJA}$	-	-	62	K/W	-
Device on PCB, 6 cm <sup>2</sup> cooling area <sup>(1)</sup>	$R_{thJA}$	-	-	40	K/W	-

<sup>(1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

<sup>(2)</sup> See Diagram 3 for more detailed information

<sup>(3)</sup> See Diagram 13 for more detailed information

### 3 Electrical characteristics

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	150	-	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	3.3	4.1	4.9	V	$V_{DS}=V_{GS}$ , $I_D=255\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	1 10	2 100	$\mu\text{A}$	$V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ }^\circ\text{C}$ $V_{DS}=120\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ }^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	2 -2	5 -5	$\mu\text{A}$	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$ $V_{GS}=-10\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.9	4.8	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=100\text{ A}$
Gate resistance <sup>1)</sup>	$R_G$	-	25	38	$\Omega$	-
Transconductance	$g_{fs}$	17	34	-	S	$ V_{DS} >2 I_D R_{DS(on)max}$ , $I_D=100\text{ A}$

**Table 5 Dynamic characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	290	380	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	1400	1800	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Reverse transfer capacitance	$C_{rss}$	-	13	23	pF	$V_{GS}=0\text{ V}$ , $V_{DS}=75\text{ V}$ , $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	8	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=60\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Rise time	$t_r$	-	48	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=60\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	42	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=60\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$
Fall time	$t_f$	-	10	-	ns	$V_{DD}=75\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=60\text{ A}$ , $R_{G,ext}=1.6\text{ }\Omega$

**Table 6 Gate charge characteristics<sup>2)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	2	-	nC	$V_{DD}=75\text{ V}$ , $I_D=60\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge <sup>1)</sup>	$Q_{gd}$	-	56	-	nC	$V_{DD}=75\text{ V}$ , $I_D=60\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total <sup>1)</sup>	$Q_g$	-	84	-	nC	$V_{DD}=75\text{ V}$ , $I_D=60\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	7	-	V	$V_{DD}=75\text{ V}$ , $I_D=60\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Output charge <sup>1)</sup>	$Q_{oss}$	-	211	280	nC	$V_{DD}=75\text{ V}$ , $V_{GS}=0\text{ V}$

<sup>1)</sup> Defined by design. Not subject to production test.

<sup>2)</sup> See "Gate charge waveforms" for parameter definition

**Table 7 Reverse diode**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_S$	-	-	120	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	480	A	$T_C=25\text{ °C}$
Diode forward voltage	$V_{SD}$	-	0.93	1.2	V	$V_{GS}=0\text{ V}, I_F=100\text{ A}, T_j=25\text{ °C}$
Reverse recovery time <sup>1)</sup>	$t_{rr}$	-	60	-	ns	$V_R=75\text{ V}, I_F=60\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge <sup>1)</sup>	$Q_{rr}$	-	81	-	nC	$V_R=75\text{ V}, I_F=60\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

<sup>1)</sup> Defined by design. Not subject to production test.

### 4 Electrical characteristics diagrams

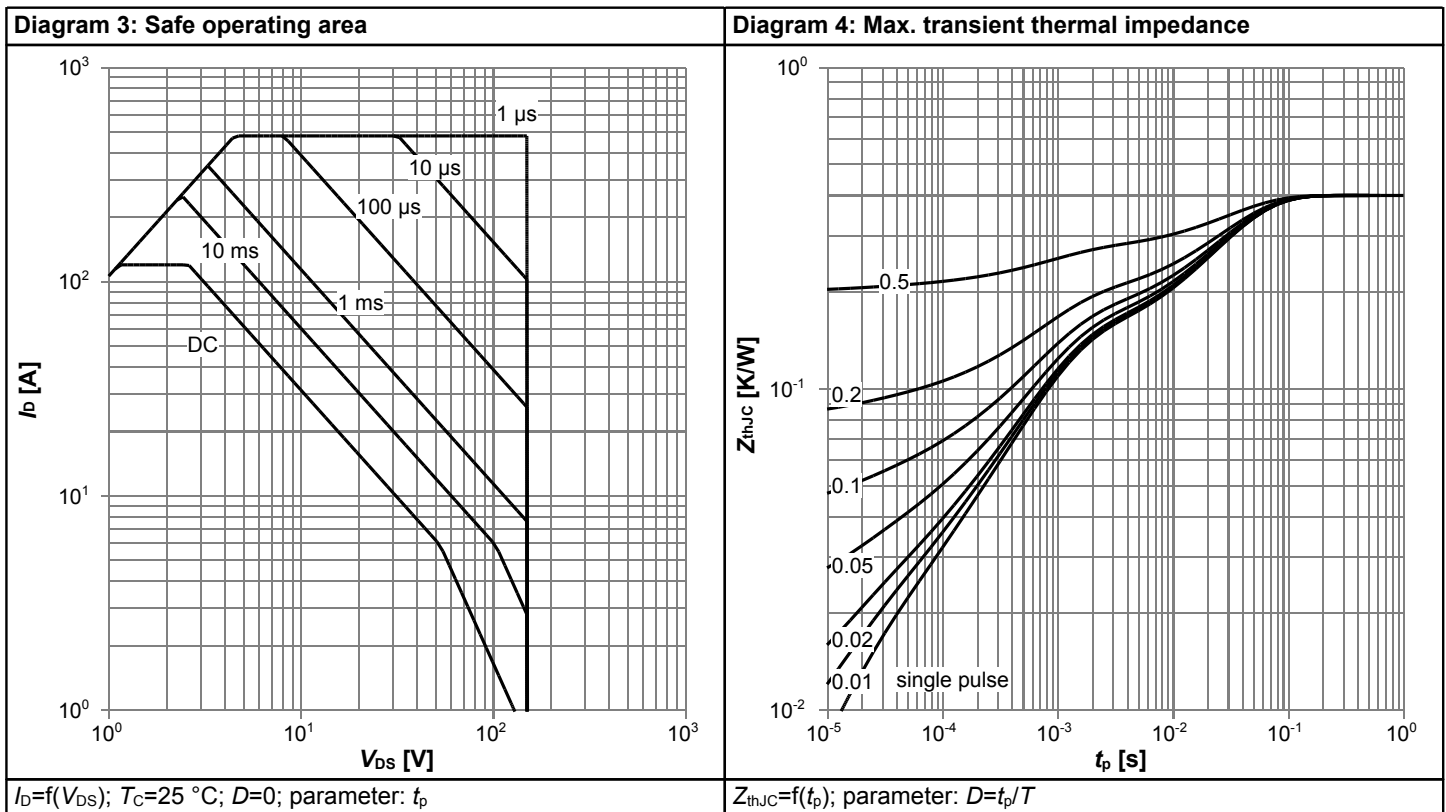
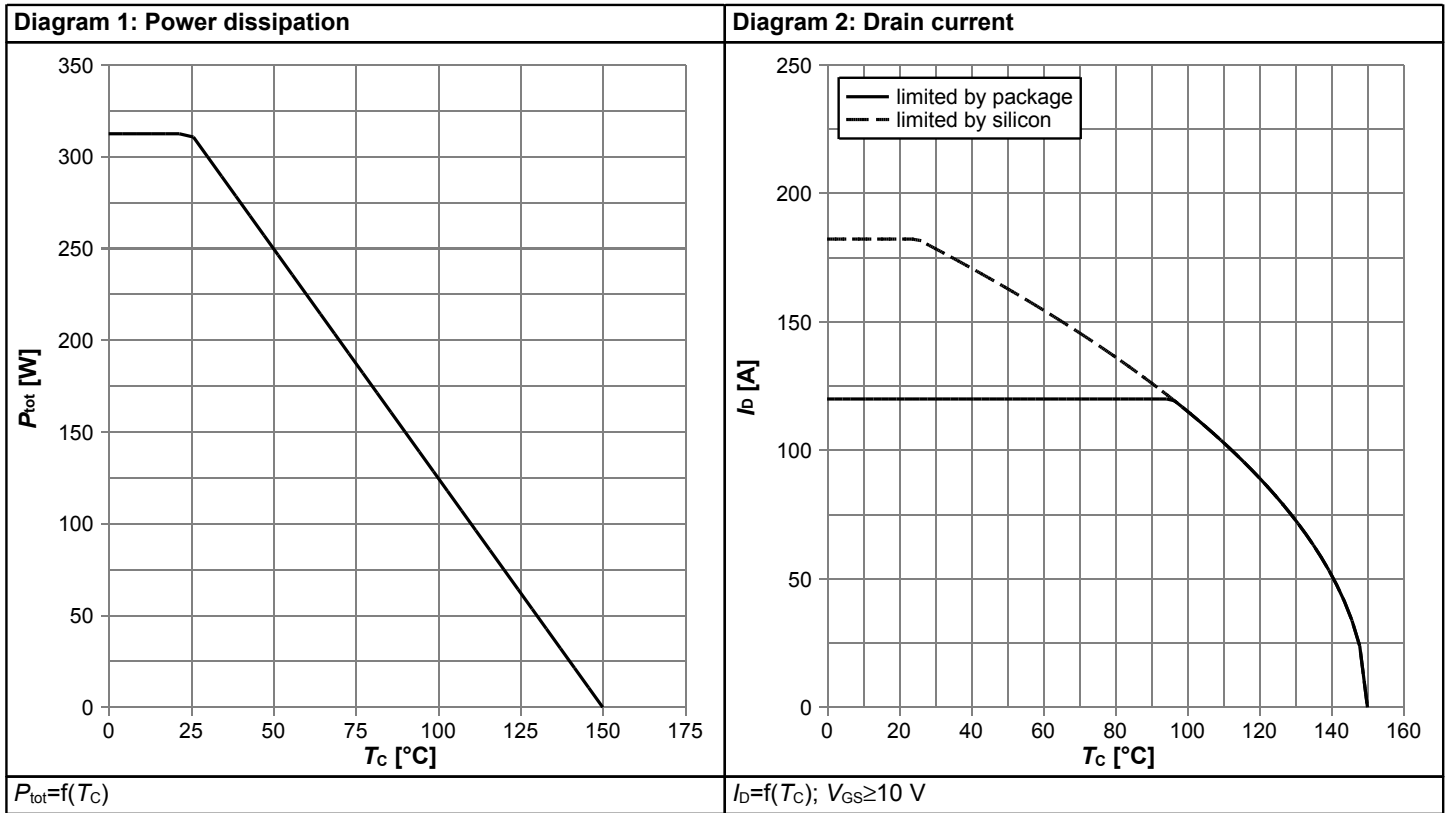
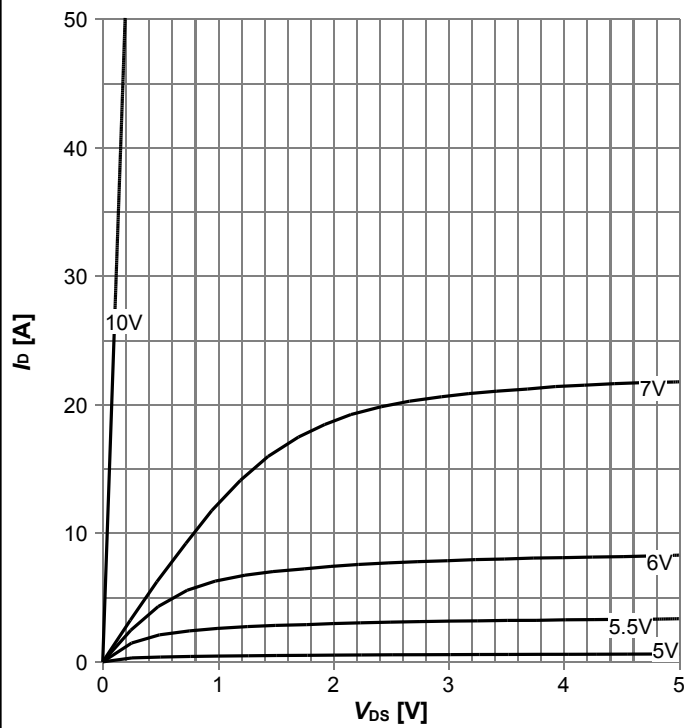
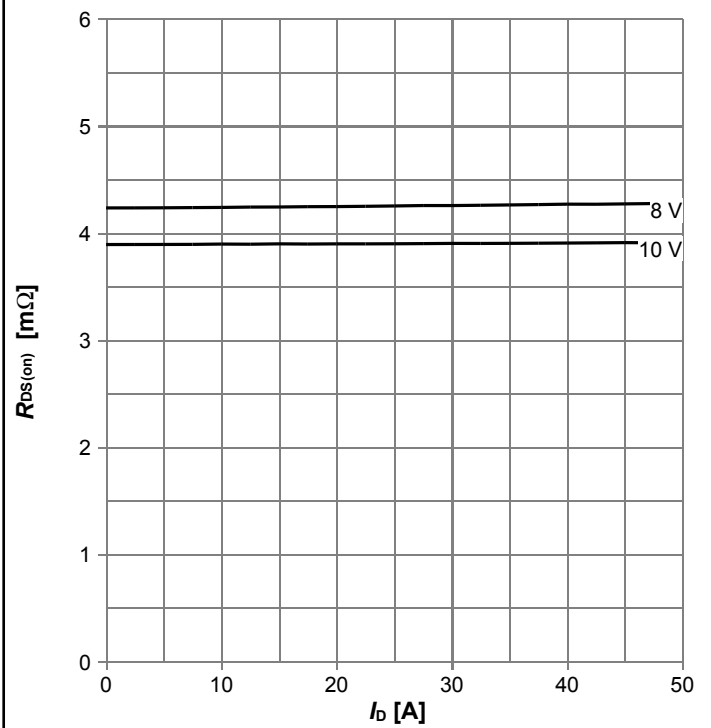


Diagram 5: Typ. output characteristics



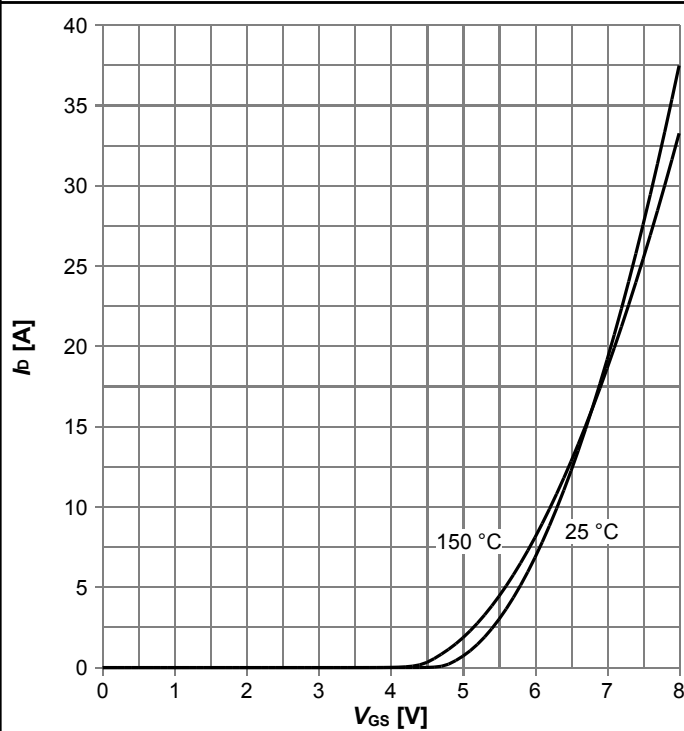
$I_D = f(V_{DS})$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 6: Typ. drain-source on resistance



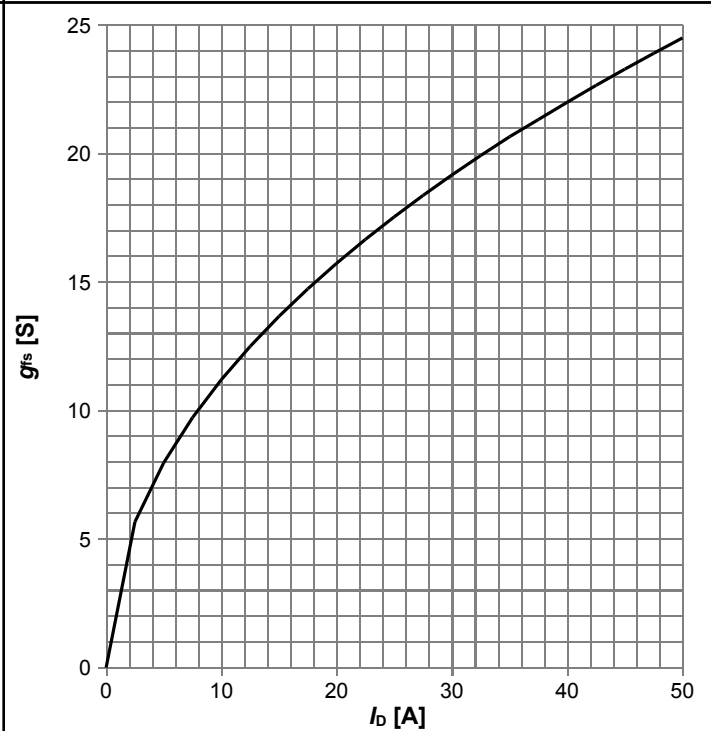
$R_{DS(on)} = f(I_D)$ ,  $T_j = 25\text{ °C}$ ; parameter:  $V_{GS}$

Diagram 7: Typ. transfer characteristics



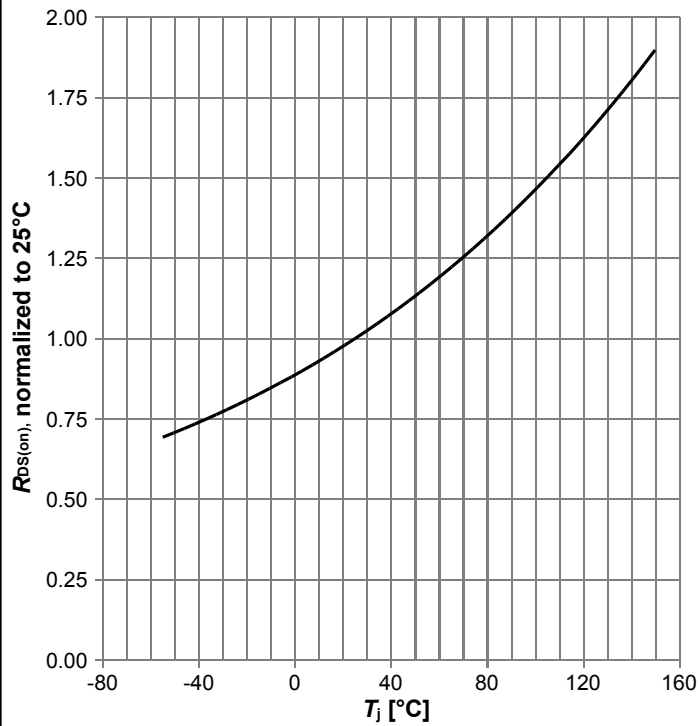
$I_D = f(V_{GS})$ ,  $|V_{DS}| > 2|I_D|R_{DS(on)max}$ ; parameter:  $T_j$

Diagram 8: Typ. forward transconductance



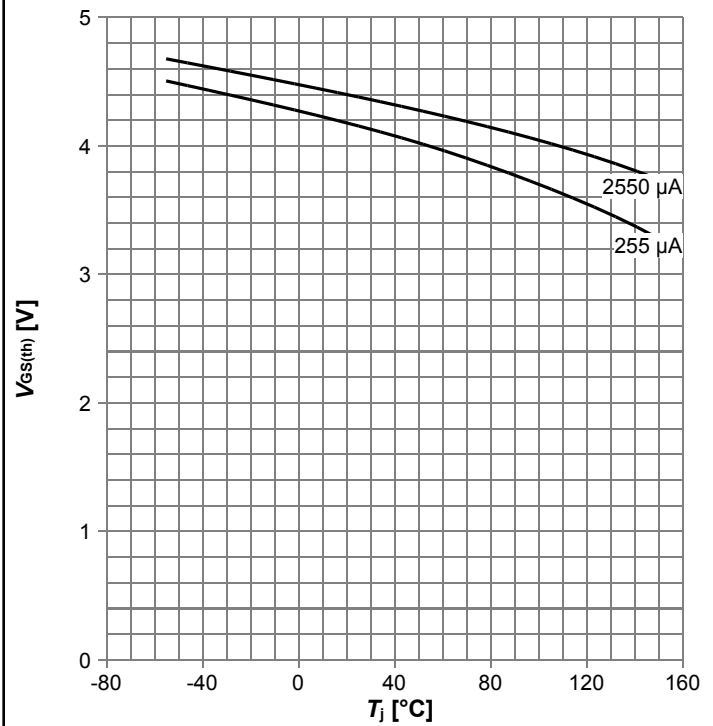
$g_{fs} = f(I_D)$ ,  $V_{DS} = 5\text{ V}$ ,  $T_j = 25\text{ °C}$

Diagram 9: Normalized drain-source on-state resistance



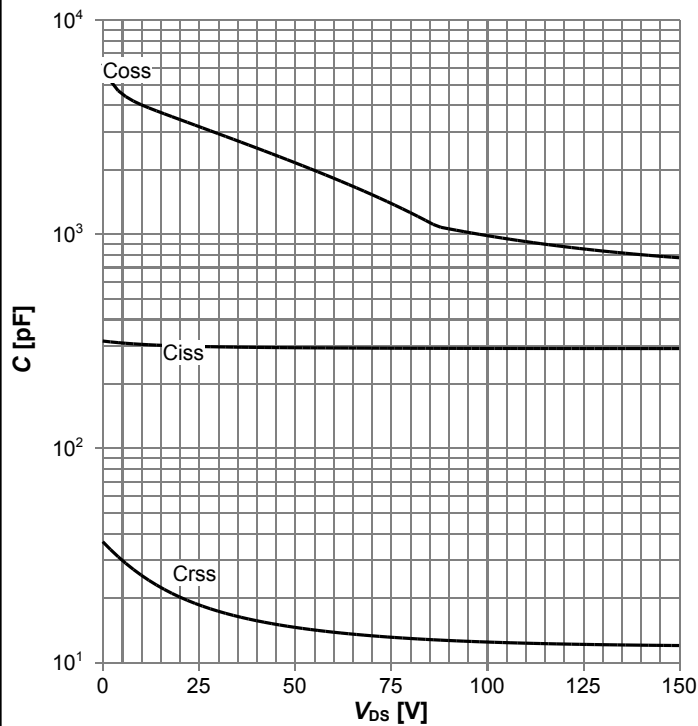
$R_{DS(on)}=f(T_j)$ ,  $I_D=100$  A,  $V_{GS}=10$  V

Diagram 10: Typ. gate threshold voltage



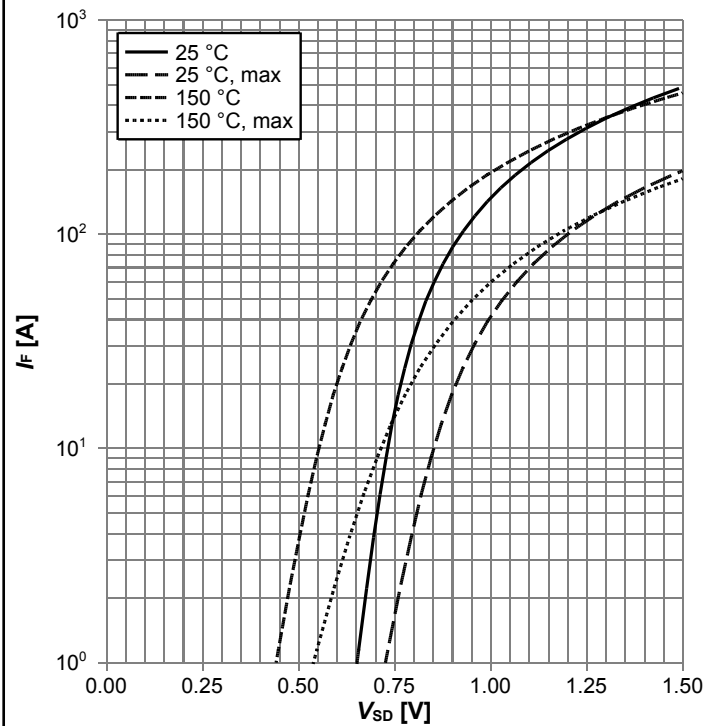
$V_{GS(th)}=f(T_j)$ ,  $V_{GS}=V_{DS}$ ; parameter:  $I_D$

Diagram 11: Typ. capacitances



$C=f(V_{DS})$ ;  $V_{GS}=0$  V;  $f=1$  MHz

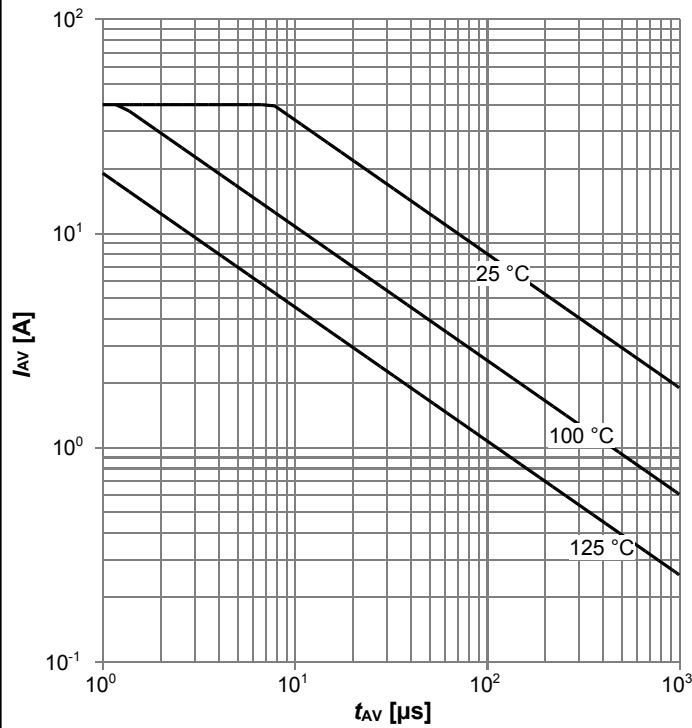
Diagram 12: Forward characteristics of reverse diode



$I_F=f(V_{SD})$ ; parameter:  $T_j$

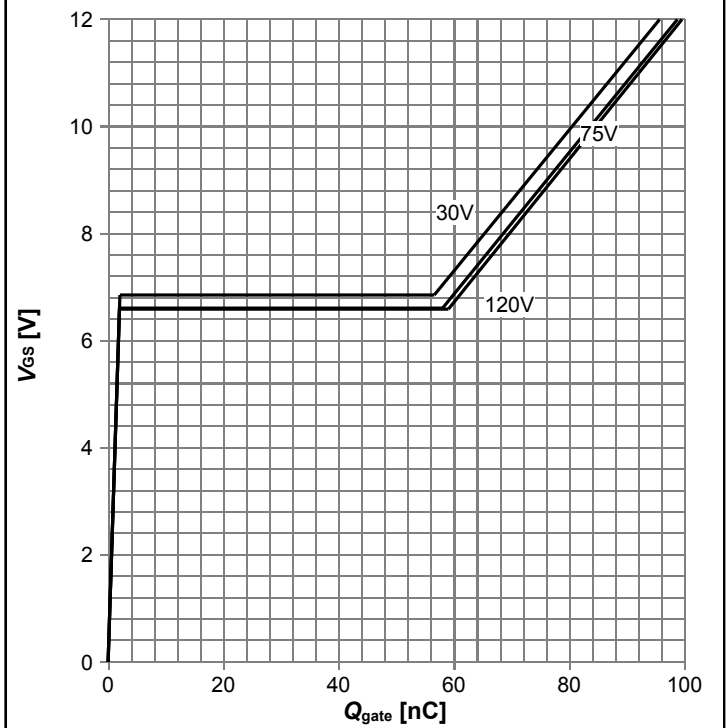


Diagram 13: Avalanche characteristics



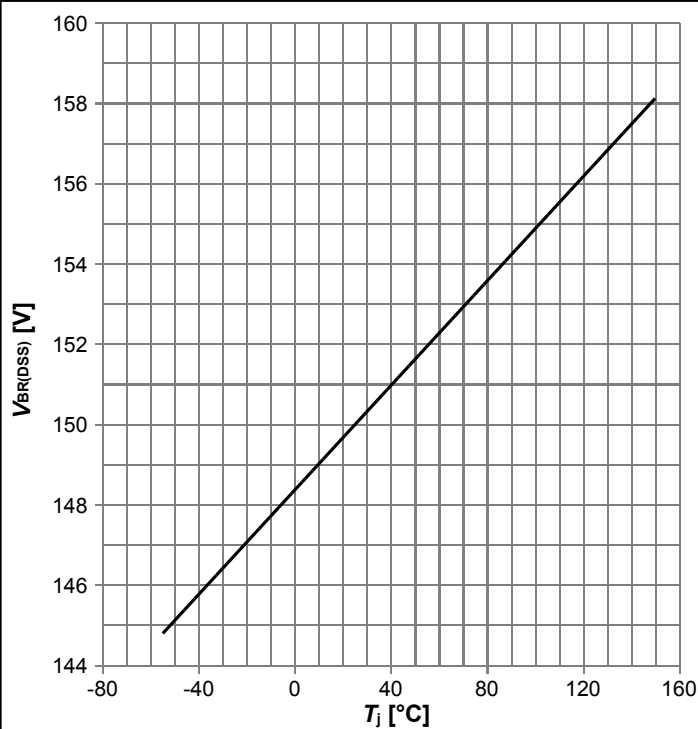
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$ ; parameter:  $T_{j,start}$

Diagram 14: Typ. gate charge



$V_{GS}=f(Q_{gate}); I_D=60 \text{ A}$  pulsed, resistive load; parameter:  $V_{DD}$

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



## 5 Package Outlines



Figure 1 Outline PG-TO 263-3, dimensions in mm/inches

## Revision History

IPB048N15N5LF

**Revision: 2017-03-29, Rev. 2.0**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2017-03-29	Release of final version

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