

REF 5BR3995CZ 16W1

About this document

Scope and purpose

This document is a reference design for a 16 W auxiliary power supply for single-phase electric meter with the latest fifth-generation Infineon fixed-frequency (FF) CoolSET™ ICE5BR3995CZ. The power supply is designed with ultra-wide input compatible with most geographic regions and three isolated outputs (12 V/1 A, 5 V/0.2 A, 5 V/0.2 A).

Highlights of the auxiliary power supply for smart metering are:

- Tightly regulated output voltages, high efficiency under light load and low standby power
- Comprehensive protection for a robust system
- 950 V rated MOSFET for ultra-wide input range
- Input line overvoltage protection (OVP)

Intended audience

This document is intended for power supply design engineers who are designing auxiliary power supplies for a single-phase electric meter or ultra-wide input range flyback converter.

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System introduction

1 System introduction

With the advancement of technology, the energy meter had also been undergoing continuous development to improve accuracy, power consumption, communication interfaces, measuring parameters, anti-tempering features, etc. These requirements are driving the demand for more innovative power supply designs to power electric meters. Infineon has introduced the latest fifth-generation FF CoolSET™ to address this need in an efficient and cost-effective manner.

An auxiliary SMPS is needed to power the various modules, which typically operate from a stable DC voltage source. The Infineon CoolSET[™] (as shown in **Figure 1**) forms the heart of the system, providing the necessary protection and AC-DC conversion from the mains to multiple regulated DC voltages to power the various blocks.

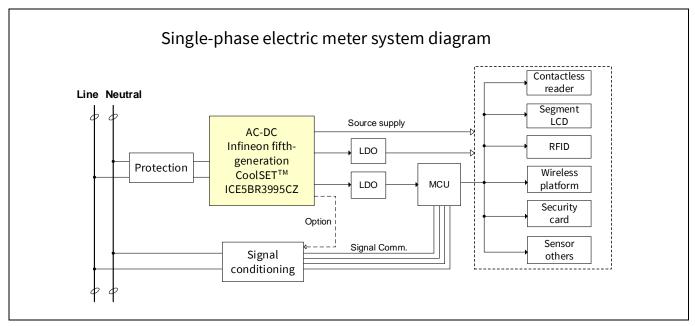


Figure 1 Simplified electric meter system diagram

Table 1 lists the system requirements for an auxiliary power supply for an electric meter, and the corresponding Infineon solution is shown in the right-hand column.

Table 1 System requirements and Infineon solutions

	System requirement for electric meter	Infineon solution – ICE5BR3995CZ
1	High efficiency under light load and low standby power	Digital frequency reduction and active burst mode (ABM)
2	Robust system and protection features	Comprehensive CoolSET™ protection feature in DIP-7 package
3	Line voltage fluctuation	950 V rated CoolMOS™ integrated for ultra-wide input voltage

1.1 High efficiency under light load and low standby power

Low power consumption of the meter is a key operating criterion. Smart meters in the field are consuming energy, which is a cost that must be paid by the end user. And in most cases, the system will reside in an idle state, in which the loading toward the auxiliary power supply is low. It is crucial that the auxiliary power supply operates as efficiently as possible, because it will be in this particular state for most of the time. Under light-



System introduction

load conditions, losses incurred with the power switch are usually dominated by the switching operation. The choice of switching scheme and frequency plays a crucial role in ensuring high conversion efficiency.

In this reference design, ICE5BR3995CZ was primarily chosen due to its frequency reduction switching scheme. Compared with a traditional FF flyback, the CoolSET™ reduces its switching frequency from medium to light load, thereby minimizing switching losses. Therefore, an efficiency of more than 80 percent is achievable under 25 percent loading conditions and nominal input voltages.

1.2 Simplified circuitry with good integration of power and protection features

To relieve the designer of the complexity of PCB layout and circuit design, CoolSET™ is a highly integrated device with both a controller and a 950 V MOSFET integrated into a single, space-saving DIP-7 package. These certainly help the designer to reduce component count as well as simplifying the layout into a simple PCB design for ease of manufacturing.

1.3 Auto-restart protection scheme to minimize interruption to enhance end-user experience

For a commercial electric meter unit, it would be annoying to both the end user and the manufacturer if the system were to halt and latch after protection. To minimize interruption, the CoolSET™ implements autorestart mode for all protections.



Reference board design

2 Reference board design

This document provides complete design details including specifications, schematics, bill of materials (BOM), PCB layout and transformer design. Performance results pertaining to line/load regulation, efficiency, transient load, thermal conditions, conducted EMI scans and so on are also included.

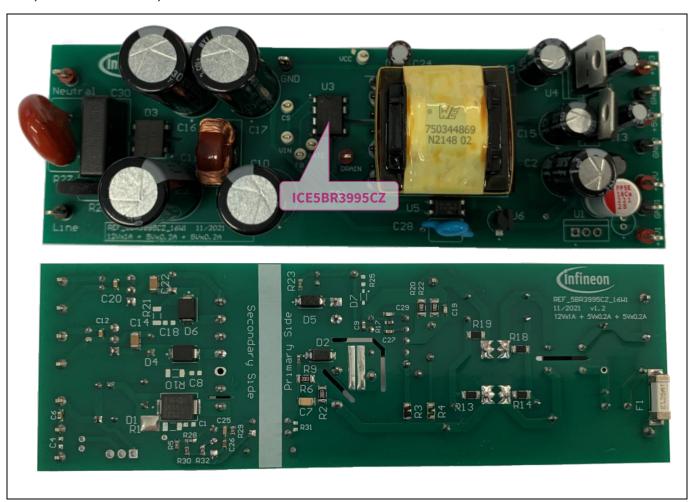


Figure 2 REF_5BR3995CZ_16W1



Power supply specifications

3 Power supply specifications

The table below shows the minimum acceptable performance of the design at 25°C ambient temperature. Actual performance is listed in the measurements section.

Table 2 Specifications of REF_5BR3995CZ_16W1

Description	Symbol	Min.	Тур.	Max.	Unit	Comments
Input						
Voltage	V _{IN}	85	_	460	V AC	2 wires (no P.E.)
Frequency	f _{LINE}	47	50/60	63	Hz	
Output						
Output voltage 1	V _{O1}	_	12	_	V	
Output current 1	I ₀₁	_	-	1.0	Α	
Output voltage ripple 1	$V_{RIPPLE1}$	_	-	120	mV	±1 percent
Output voltage 2	V _{O2}	_	5	-	V	
Output current 2	I _{O2}	_	_	0.2	Α	±1 percent, tapped from 8 V output via LDO
Output voltage ripple 2	$V_{RIPPLE2}$	-	-	50	mV	
Output voltage 3	V _{O3}	_	5		V	
Output current 3	I _{O3}	_	_	0.2	Α	±1 percent, tapped from 8 V output via LDO
Output voltage ripple 3	$V_{RIPPLE3}$	_	_	50	mV	
Output power	P_{OUT_Nom}		14	_	W	
Overcurrent protection (12 V)	I _{OCP}		1.2	_	Α	
Start-up time	t _{start_up}		-	350	ms	With full load on other outputs
Environmental						
Conducted EMI		10		dB	Margin, CISPR 22 class B	
ESD						EN 61000-4-2
Contact discharge			±6		kV	
Air discharge			±8		kV	
Surge immunity						EN 61000-4-5
Differential mode			±2		kV	
Common mode			±6		kV	
PCBA dimension		1	40 x 45 x 3	5	mm²	LxWxH



Circuit diagram

Circuit diagram 4

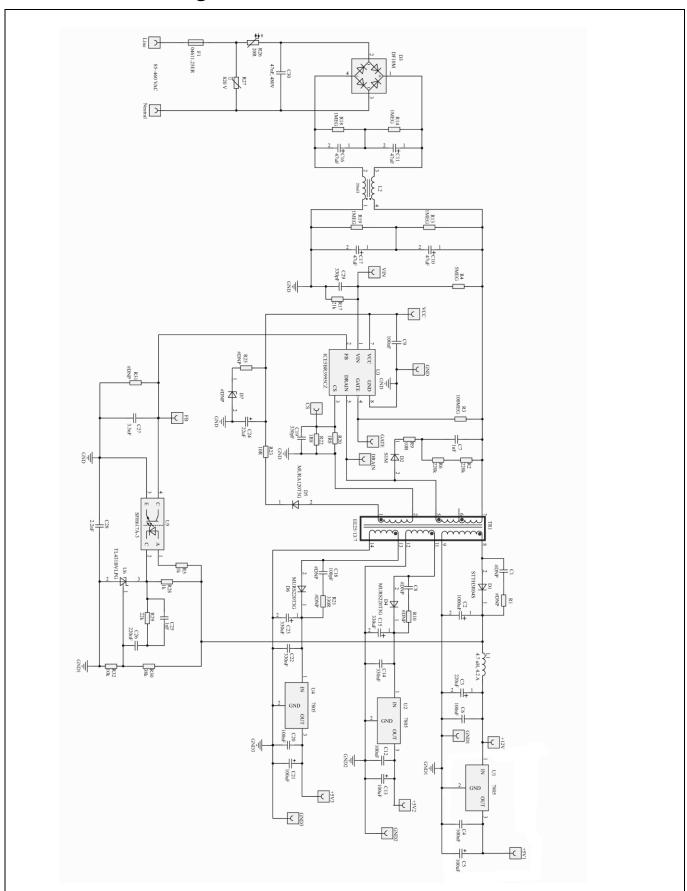


Figure 3 Schematic of REF_5BR3995CZ_16W1



Circuit description

5 Circuit description

In this section, the design circuit for the SMPS unit will be briefly described by the different functional blocks. For details of the design procedure and component selection for the flyback circuitry please refer to the IC design guide [2] and calculation tool [3].

5.1 EMI filtering and line rectification

The input of the power supply unit is in the range of 85 V AC ~ 460 V AC. The fuse F1 is directly connected to the input line to protect the system in case of excess current entering the system circuit due to any fault. Following is the varistor R27, which is connected across the input to absorb excess energy during line-surge transient. Thermistor R26 is placed to reduce inrush current during the turning-on period. The X-capacitor C30 reduces EMI noise. The bridge rectifier D3 rectifies the AC input into DC voltage, filtered by the Pi circuit, which reduces the EMI noise.

5.2 Flyback converter power stage

The flyback converter power stage consists of transformer TR1, CoolSET[™], secondary rectification diodes D1, D4 and D6, and secondary output capacitors C2, C15 and C23.

When the primary HV MOSFET turns on, energy is stored in the transformer. When it turns off, the stored energy is discharged to the output capacitors and into the output load.

For the output rectification, lower forward voltage and ultrafast recovery diodes can improve efficiency. There are two separate 5 V outputs from low dropout (LDO) regulator (U2, U4), and these outputs are not affected by cross-regulation. However, their inputs should be maintained within the operating range of the LDO.

5.3 Control of flyback converter through fifth-generation FF CoolSET™ ICE5BR3995CZ

5.3.1 Current sensing

The ICE5BR3995CZ is a current mode controller. The primary peak current is controlled cycle-by-cycle through the current sense (CS) resistors R20 and R22 in the CS pin (pin 3). Transformer saturation can be avoided through peak-current limitation (PCL); therefore, the system is more protected and reliable.

5.3.2 Feedback and compensation network

Resistor dividers R30 and R32 are used to sense the V_{OUT} and send the reference voltage to the feedback (FB) pin (pin 2) via error amplifier TL431(U6) and optocoupler (U5). A Type II compensation network (C25, C26 and R29) is implemented to stabilize the system.

The FB pin of ICE5BR3995CZ is a multifunction pin, which is used to select the entry burst power level (there are three levels available) through the resistor at the FB pin (R31) and also the burst-on/burst-off sense input during ABM. Here R31 is not placed for default ABM configuration.



Circuit description

5.4 Unique features of the fifth-generation FF CoolSET™ ICE5BR3995CZ

5.4.1 Fast self-start-up and sustaining of V_{cc}

The IC uses a cascode structure to fast-charge the V_{CC} capacitor. Pull-up resistor R3 connected to the GATE pin (pin 4) is used to initiate the start-up phase. At first, $I_{VCC_Charge1}$ is used to charge the V_{CC} capacitor from 0 V to V_{CC_SCP} . This is a protection which reduces the power dissipation of the power MOSFET during V_{CC} short-to-GND condition. Thereafter, a much higher charging current of $I_{VCC_Charge2}$ will charge the V_{CC} capacitor until the V_{CC_ON} is reached.

After start-up, the IC V_{CC} supply is usually sustained by the auxiliary winding of the transformer, which needs to support the V_{CC} to be above undervoltage lockout (UVLO) voltage (10 V typ.).

5.4.2 CCM, DCM operation with frequency reduction

ICE5BR3995CZ can be operated in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM) with frequency-reduction features. This reference board is designed to operate in DCM at operating input voltage and load conditions. When the system is operating at high output load, the controller will switch at 65 kHz FF. In order to achieve a better efficiency between light load and medium load, frequency reduction is implemented as a function of V_{FB} , as shown in **Figure 4**. Switching frequency will not reduce further once the minimum switching frequency of 28 kHz is reached.

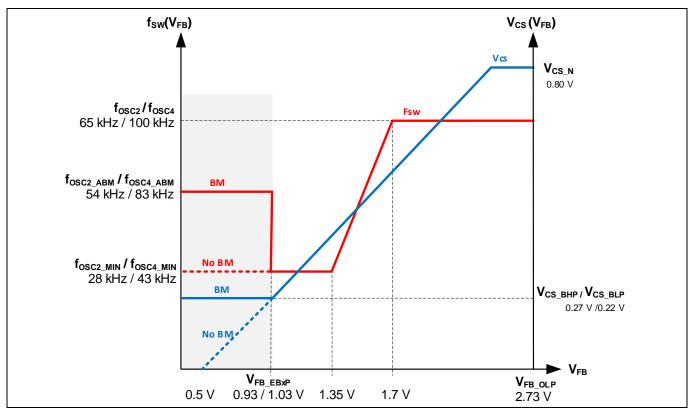


Figure 4 Frequency reduction curve

5.4.3 Frequency jittering with modulated gate drive

The ICE5BR3995CZ has a frequency jittering feature with modulated gate drive to reduce the EMI noise. The jitter frequency is internally set at 65 kHz (±4 percent), and the jitter period is 4 ms.



Circuit description

5.4.4 System robustness and reliability through protection features

Protection is one of the major factors in determining whether the system is safe and robust – therefore sufficient protection is necessary. ICE5BR3995CZ provides comprehensive protection to ensure the system is operating safely. This includes line overvoltage protection (LOVP), V_{cc} OV and undervoltage (UV), overload, overtemperature and V_{cc} short-to-GND. When those faults are found, the system will enter protection mode. Once the fault is removed, the system resumes normal operation. A list of protections and failure conditions is shown in the table below.

Table 3 Protection functions of ICE5BR3995CZ

Protection function	Failure condition	Protection mode		
V _{IN} LOVP	V _{VIN} greater than V _{VIN_LOVP}	Non-switch auto-restart		
V _{cc} OV	V_{VCC} greater than V_{VCC_OVP}	Odd-skip auto-restart		
V _{cc} UV	V_{VCC} less than V_{VCCoff}	Auto-restart		
Overload	V_{FB} greater than V_{FB_OLP} and lasts for $t_{FB_OLP_B}$	Odd-skip auto-restart		
Overtemperature	T _J greater than 140°C (40°C hysteresis)	Non-switch auto-restart		
V_{CC} short-to-GND ($V_{VCC} = 0 \text{ V}, R_{\text{start-up}} = 50 \text{ M}\Omega, V_{DRAIN} = 90 \text{ V}$)	V_{VCC} less than V_{CC_SCP} , $I_{VCC_Charge1} \approx -0.2$ mA	Cannot start up		

5.5 Clamper circuit

A clamper network (D2, C7, R2, R6, R9) is used to reduce the switching voltage spikes across the DRAIN pin of the integrated HV MOSFET of the CoolSET™, which are generated by the leakage inductance of the transformer TR1. This is a dissipative circuit; therefore, the value of clamper devices need to be fine-tuned depending on the voltage derating factor and efficiency requirement.

5.6 PCB design tips

For a good PCB design layout, there are several points to note.

• The switching power loop needs to be as small as possible (see **Figure 5**). There are four power loops in the reference design; one on the HV side and three on the output side. The HV side loop starts from the bulk capacitor (C10) positive terminal, primary transformer winding (pin 7 and pin 5 of TR1), CoolSET™, CS resistors and back to the C17 negative terminal. The first output side loop (12 V output) starts at the transformer winding (pin 8 of TR1), output diode D1, output capacitor C2 and back to pin 9 of TR1. The second output side loop (8 V output) starts at the transformer winding (pin 11 of TR1), output diode D4, output capacitor C15 and back to pin 12 of TR1. The third output side loop (8 V output) starts at the transformer winding (pin 13 of TR1), output diode D6, output capacitor C23 and back to pin 14 of TR1.



Circuit description

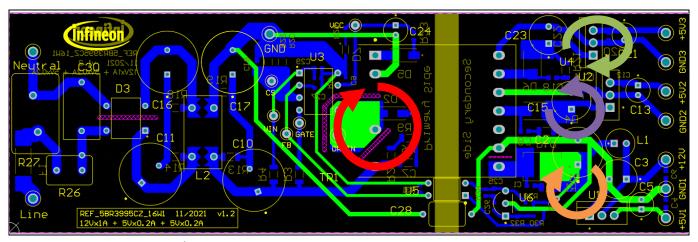


Figure 5 PCB layout tips

- Star-ground connection should be used to reduce high-frequency (HF) noise coupling that can affect the functional operation. The ground of the small-signal components should connect directly to the IC ground (pin 8 of U3).
- Separating the HV components and LV components, e.g., clamper circuit, main switching circuit can help to reduce spark-over chance of the high energy surge during a lightning surge test.
- Make the PCB copper pour on the DRAIN pin of the MOSFET act as a heatsink.

5.7 EMI reduction tips

EMI compliance is always a challenge for the power supply designer. There are several critical points to consider in order to achieve a satisfactory EMI performance.

- A proper transformer design can significantly reduce EMI. Low leakage inductance can incur a low switching spike and HF noise. Interlaced winding technique is the most common practice to reduce leakage inductance. Winding shield, core shield and whole transformer shield are also some of the techniques used to reduce EMI.
- Input CMC greatly reduces EMI, but this is costly and impractical especially for low-power applications.
- Short-switching power-loop design in the PCB (as described in section 5.6) can reduce radiated EMI due to the antenna effect.
- An output diode snubber circuit can reduce HF noise.
- Ferrite beads can reduce HF noise, especially on critical nodes such as the DRAIN pin, clamper diode and output diode terminals. There is no ferrite bead used in this design, as this can reduce the efficiency due to additional losses, especially on high-current terminals.



PCB layout

6 PCB layout

6.1 Top side

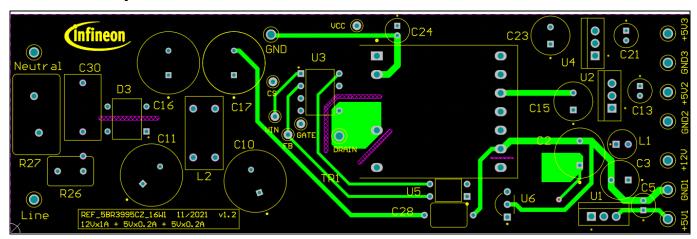


Figure 6 Top-side component legend

6.2 Bottom side

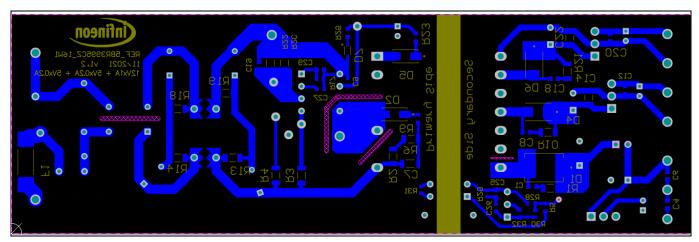


Figure 7 Bottom-side component legend



Bill of materials

7 Bill of materials

Table 4 BOM

No.	Designator	nator Description		Manufacturer	Quantity	
1	C19, C29	Ceramic capacitor 330 pF 50 V COG/NP0 0603			2	
2	C2	Aluminum capacitor 1000 μF 20% 25 V radial	· · · · · · · · · · · · · · · · · · ·		1	
3	СЗ	Aluminum capacitor 220 μF 20% 25 V radial	UHD1E221MPD1TD	Nichicon	1	
4	C13, C21	Capacitor 100 μF 20% 10 V	10YXF100MEFCT15X 11	Rubycon	2	
5	C7	Ceramic capacitor 1206 1 nF 500 V X7R 10%	12067C102KAT2A	AVX	1	
6	C4, C6, C9, C12, C20	Ceramic capacitor 100 nF 50 V X7R 0603			5	
7	C10, C11, C16, C17	Aluminum capacitor 47 μF 20% 400 V	EPAG401ELL470MK3 0S	United Chemi- Con	4	
8	C14, C22	Ceramic capacitor 1206 330 nF 50 V X7R			2	
9	C15, C23	Aluminum capacitor 330 μF 20% 16 V	16YXF330MEFC8X11. 5	Rubycon	2	
10	C24	Capacitor 22 μF 20% 35 V	UPW1H220MDD1TD	Nichicon	1	
11	C25	Ceramic capacitor 1000 pF 50 V X7R 0603			1	
12	C26	Ceramic capacitor 220 nF 50 V X7R 0603			1	
13	C27	Ceramic capacitor 3300 pF 50 V X7R 0603			1	
14	C28	Ceramic capacitor 2200 pF 440 V AC radial			1	
15	C30	Capacitor, SUP, X1, 0.047 μF, 480 V AC		Keya	1	
16	D1	Ultrafast diode 400 V 3 A SMC	afast diode 400 V 3 A SMC STTH3R04S STMic ics		1	
17	D2	General-purpose diode 1 kV 1 A DO214AC	. A S1M ON Semic		1	
18	D3	Bridge rectifier 1-phase 1 kV 1.5 A 4-DIP	' I DETOM I		1	
19	D4, D6	General-purpose diode 200 V 2 A SMB	MURS220T3G	ON Semiconductor	2	
20	D5	General-purpose diode 200 V 1 A SMA	MURA120T3G	ON Semiconductor	1	
21	F1	Surge-resistant TeleLink fuse	04611.25ER	Littelfuse	1	
22	L1	Fixed inductor 4.7μH 4.2 A 30 mΩ TH			1	
23	L2	CMC 20 mH 500 mA 2LN TH	744821120	Würth Elektronik	1	
24	R2, R6	SMD resistor 200 kΩ 1% 1/4 W 1206			2	
25	R3	SMD resistor 100 mΩ 1% 300 mW 1206	CRHA1206AF100MFK EF	Vishay	1	
26	R4	SMD resistor 5 mΩ 1% 300 mW 1206	SMD resistor 5 mΩ 1% 300 mW 1206 CRHV1206AF5M00FK FT Vishay		1	
27	R13, R14, R18, R19	SMD resistor 0.25 W 1 mΩ 1% 100 ppm	SMD resistor 0.25 W 1 mΩ 1% 100 ppm RCV12061M00FKEA Vishay		4	
28	R9, R23	SMD resistor 10 Ω 1% 1/10 W 0603	SMD resistor 10 Ω 1% 1/10 W 0603		2	
29	R17	SMD resistor 20.5 kΩ 1% 1/10 W 0603	SMD resistor 20.5 kΩ 1% 1/10 W 0603		1	
30	R20, R22	SMD resistor 1.8 Ω 1% 1/4 W 1206	SMD resistor 1.8 Ω 1% 1/4 W 1206		2	
31	R5, R28	SMD resistor 1 kΩ 1% 1/10 W 0603			2	
32	R29	SMD resistor 22 kΩ 1% 1/10 W 0603			1	
33	R30	SMD resistor 38 kΩ 1% 1/10 W 0603			1	
34	R32	SMD resistor 10 kΩ 1% 1/10 W 0603	<u> </u>		1	



Bill of materials

35	R26	ICL 25 Ω 20% 2.5 A 11.5 mm	B57236S0250M051	TDK	1
36	R27	Varistor 820 V 6.5 kA disk 14 mm	V14H510AUTO	Littelfuse	1
37	TR1	Transfomer EE25/13/7	750344869(rev.02)	Würth Elektronik	1
38	U2, U4	IC linear regulator 5 V 1.5 A TO-220AB	L7805ABV	STMicroelectron ics	2
39	U3	FF 950 V CoolSET™	ICE5BR3995CZ	Infineon	1
40	U5	Opto-isolator 5.3 kV transistor 4-DIP	SFH617A-3	Vishay	1
41	U6	IC V _{REF} shunt 36 V 0.4% TO92-3	TL431BVLPG	ON Semiconductor	1
42	+5 V1, +5 V2, +5 V3, +12 V, DRAIN, neutral	Test point THT, red	5010	Keystone	6
43	GND, GND1, line, GND2, GND3	Test point THT, black	5011	Keystone	5
44	CS, FB, GATE, V _{CC} , V _{IN}	Test point THT, white	5002	Keystone	5



Transformer specification

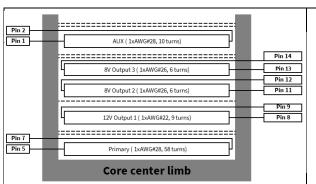
Transformer specification 8

Refer to Appendix A for transformer design.

Core name and material: EE25/13/7, TP4A (TDG)

Primary inductance: $L_p = 730 \mu H$ (±10 percent), measured between pin 5 and pin 7

Manufacturer and part number: Würth Elektronik Midcom (750344869) Rev. 02



Wire size requirement :									
Start	Stop	No. of turns	Wire size	Layer					
5	7	58	1 x AWG#28	Primary					
8	9	9	1 x AWG#22	O/P_1 Secondary					
11	12	6	1 x AWG#26	O/P_2 Secondary					
13	14	6	1 x AWG#26	O/P_3 Secondary					
1	2	11	1 x AWG#28	AUX					

Horizontal and vertical external shields are added and tied to pin 2

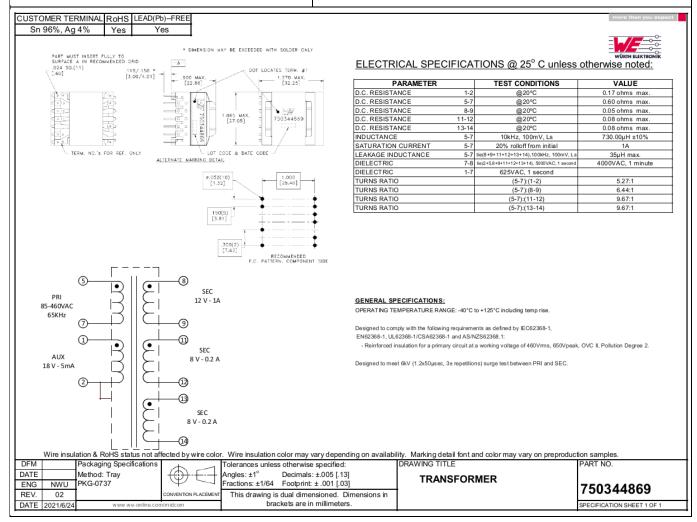


Figure 8 **Transformer structure**



Measurement data and graphs

Measurement data and graphs 9

Table 5 **Efficiency and standby performance**

Input (V AC/Hz)	P _{IN} (W)	V ₀₁ (V)	I ₀₁ (A)	V ₀₂ (V)	I ₀₂ (A)	V ₀₃ (V)	I ₀₃ (A)	Р _{оит} (W)	Efficiency (%)
05.1/4.0/60.11	0.226	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
85 V AC/60 Hz	19.490	12.000	0.996	4.985	0.198	4.968	0.198	13.918	71.41
115 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0.245	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
115 V AC/60 Hz	18.926	12.000	0.996	4.985	0.198	4.968	0.198	13.918	73.54
222 1/4 6/50 11	0.361	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
230 V AC/50 Hz	18.720	12.000	0.996	4.992	0.198	4.968	0.198	13.919	74.36
2647/46/5011-	0.455	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
264 V AC/50 Hz	18.689	12.000	0.996	4.992	0.198	4.968	0.198	13.919	74.48
200 \ / 4 C / 5 0 \ / 1	0.447	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
300 V AC/50 Hz	18.753	12.000	0.996	4.992	0.198	4.968	0.198	13.919	74.22
4C0 \/ AC /F0 \ I-	0.805	12.015	0.000	5.010	0.005	4.980	0.005	0.050	
460 V AC/50 Hz	19.650	12.000	0.996	4.992	0.198	4.968	0.198	13.919	70.84

Minimum-load condition: 12 V/0 mA, 5 V/5 mA, 5 V/5 mA;

Full-load condition: 12 V/1.0 A, 5 V/200 mA, 5 V/200 mA;

Minimum-load current for LDO regulation is 5 mA.

Efficiency and standby performance with a single-output configuration Table 6

Input (V AC/Hz)	P _{IN} (W)	V ₀₁ (V)	I ₀₁ (A)	P _{out} (W)	Efficiency
05.7/ 4.6/60.11-	0.052	12.078	0.000	0.000	
85 V AC/60 Hz	15.570	12.046	0.996	11.998	77.06%
115 \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \	0.067	11.984	0.000	0.000	
115 V AC/60 Hz	15.190	12.046	0.996	11.998	78.98%
220 V AC/F0 H-	0.164	12.078	0.000	0.000	
230 V AC/50 Hz	15.100	12.046	0.996	11.998	79.46%
2647/46/5011-	0.206	12.078	0.000	0.000	
264 V AC/50 Hz	15.150	12.046	0.996	11.998	79.19%
200 // 4.0 //50 //-	0.256	12.078	0.000	0.000	
300 V AC/50 Hz	15.220	12.046	0.996	11.998	78.83%
450 \ 46 50 1-	0.563	12.780	0.000	0.000	
460 V AC/50 Hz	16.070	12.046	0.996	11.998	74.66%

Note:

Single-output (+12 V) configuration efficiency measurement was done by removing two LDO outputs; the actual board comes with LDO circuits. The overall circuit is not optimized for singleoutput configuration; the above efficiency data is for illustration only.



Measurement data and graphs

9.1 Efficiency curve

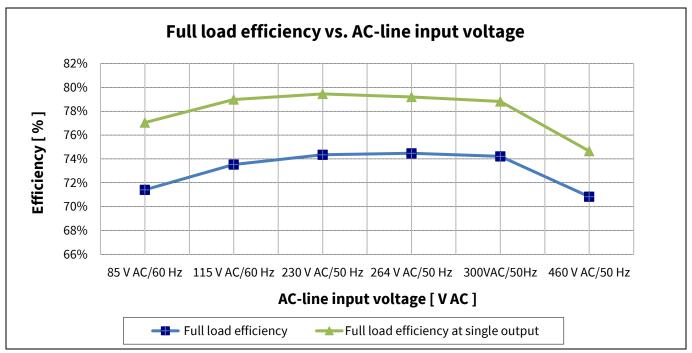


Figure 9 Efficiency vs. input line voltage

9.2 Standby power

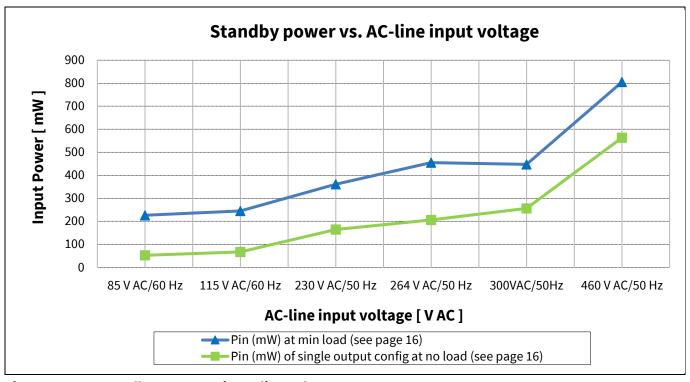


Figure 10 Standby power vs. input line voltage



Measurement data and graphs

9.3 Output voltage regulation

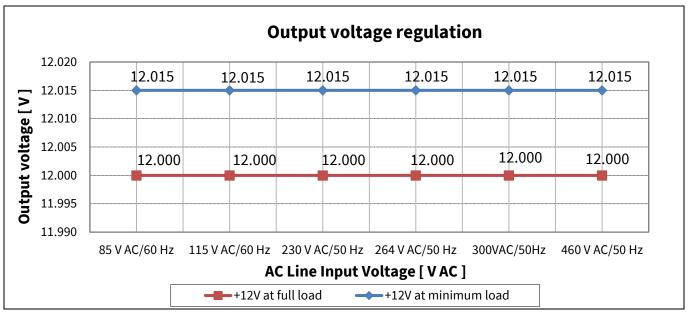


Figure 11 Output voltage regulation

9.4 ESD immunity (EN 61000-4-2)

This system was subjected to ESD testing according to EN 61000-4-2 for both contact and air discharge. A test failure was defined as non-recoverable.

• Air discharge: pass ±8 kV; contact discharge: pass ± 6 kV.

Table 7 System ESD test result

	ECD L I		Number of strike	es	
Description	ESD test	Level	V ₀₁	GND	Test result
115/2201/ 40	Contact	±6 kV	10	10	Pass
115/230 V AC	Air	±8 kV	10	10	Pass

9.5 Surge immunity (EN 61000-4-5)

The reference board was subjected to a surge immunity test (±2 kV DM and ±6 kV CM) according to EN 61000-4-5. It was tested at full load (resistive load). A test failure was defined as non-recoverable.

Table 8 System surge immunity test result

Description	Tost	Lovol	N	umbe	Test result		
Description	Test	Level	0°	90°	180°	270°	restresutt
115/230 V AC	DM	±2 kV	3	3	3	3	Pass
115/230 V AC	СМ	±6 kV	3	3	3	3	Pass



Measurement data and graphs

9.6 Conducted emissions (EN 55022 class B)

The conducted EMI was measured by Schaffner (SMR4503) and followed the test standard of EN 55022 (CISPR 22) class B. The reference board was tested at full load (resistive load) at an input voltage of 115 V AC and 230 V AC.

- 115 V AC: pass with greater than 10 dB margin for quasi-peak measurement
- 230 V AC: pass with greater than 10 dB margin for quasi-peak measurement

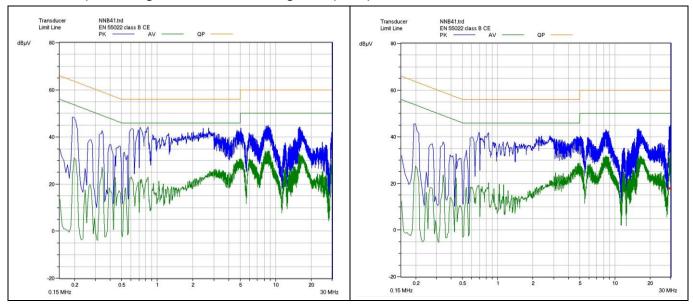


Figure 12 Conducted emissions at 115 V AC and full load on line (left) and neutral (right)

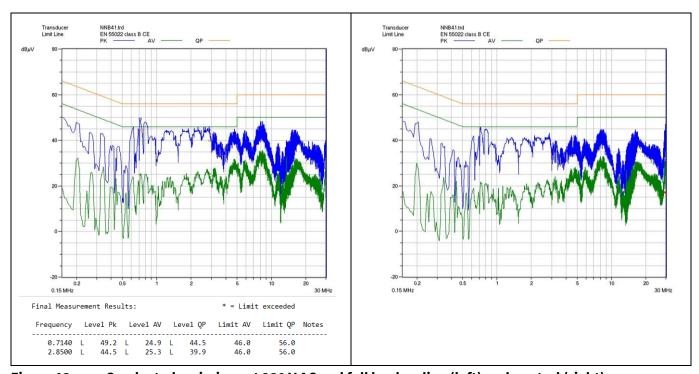


Figure 13 Conducted emissions at 230 V AC and full load on line (left) and neutral (right)



Measurement data and graphs

9.7 Thermal measurement

Thermal measurement was done using an infrared thermography camera (FLIR-T62101) at an ambient temperature of 25°C taken after one hour running at full load. The temperature of the components was taken in an open-frame set-up.

Table 9 Thermal measurement of components (open-frame)

No.	Components	Temperature at 85 V AC (°C)	Temperature at 460 V AC (°C)
1	U3 (ICE5BR3995CZ)	68.3	83.1
2	D3 (bridge diode)	55.5	37.4
3	TR1 (transformer)	56.6	65.5
4	D1 (output 1 diode)	97.2	97.8
5	D4 (output 2 diode)	68.6	69.8
6	D6 (output 3 diode)	64.7	65.6

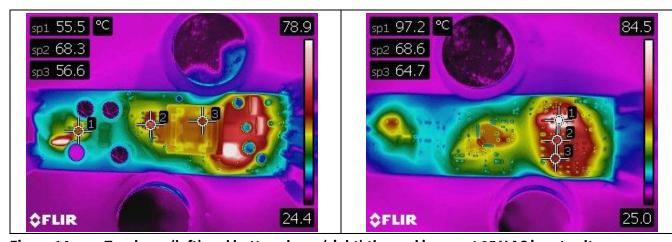


Figure 14 Top-layer (left) and bottom-layer (right) thermal image at 85 V AC input voltage

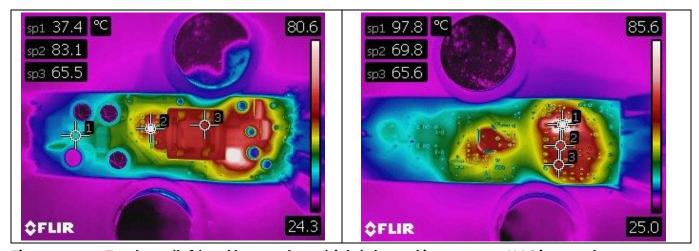


Figure 15 Top-layer (left) and bottom-layer (right) thermal image at 460 V AC input voltage



Waveforms and oscilloscope plots

10 Waveforms and oscilloscope plots

All waveforms and scope plots were recorded with a Teledyne LeCroy HDO4034 oscilloscope.

10.1 Start-up at full load

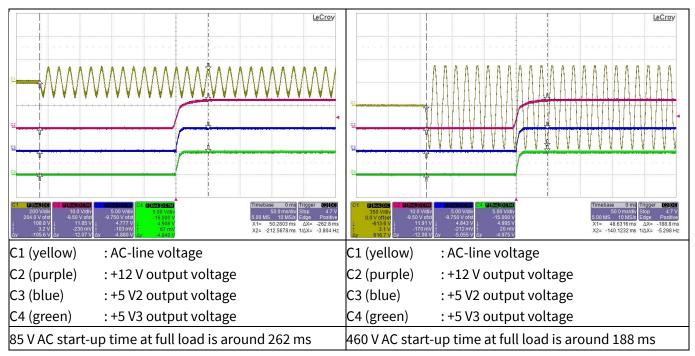


Figure 16 Start-up

10.2 Soft-start at full load

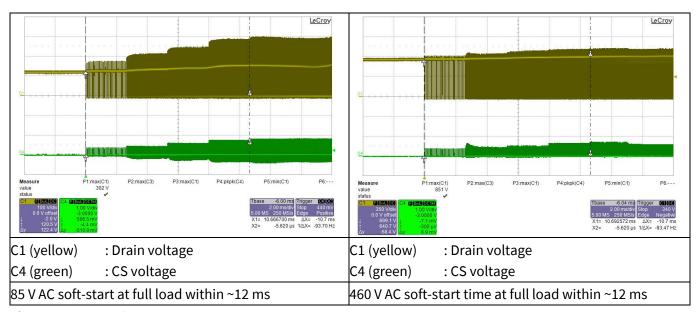


Figure 17 Soft-start



Waveforms and oscilloscope plots

10.3 Drain and CS voltage at full load

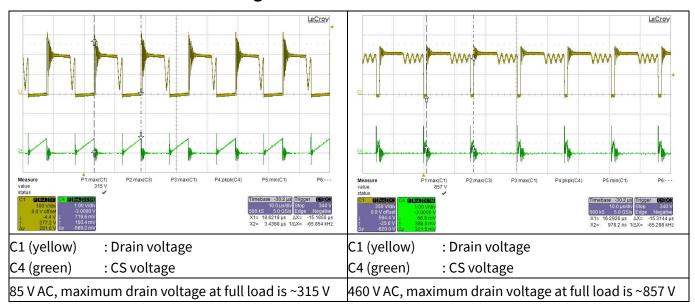


Figure 18 Drain and CS voltage

10.4 Frequency jittering and modulated gate drive

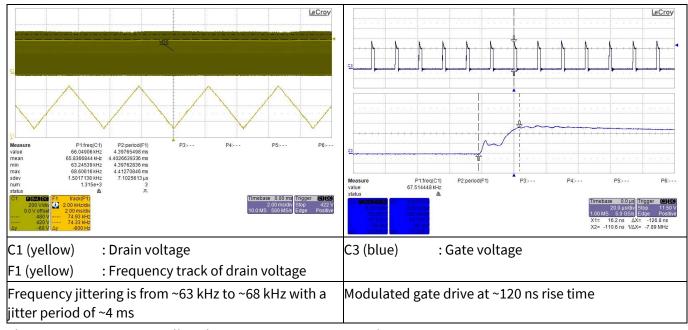


Figure 19 Frequency jittering and modulated gate drive



Waveforms and oscilloscope plots

10.5 Load-transient response

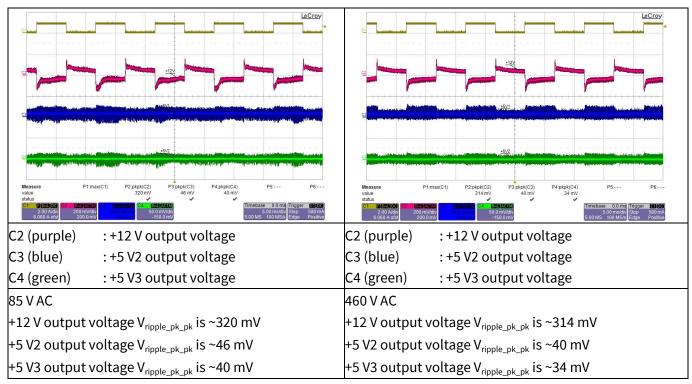


Figure 20 Load-transient response with +12 V output load change from 10 percent load to 100 percent load at 0.4 A/ μ s slew rate, 100 Hz. +5 V2 and +5 V3 output load are fixed at 0.2 A. Probe terminals are decoupled with 10 μ F electrolytic and 0.1 μ F ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz

10.6 Output ripple voltage at full load

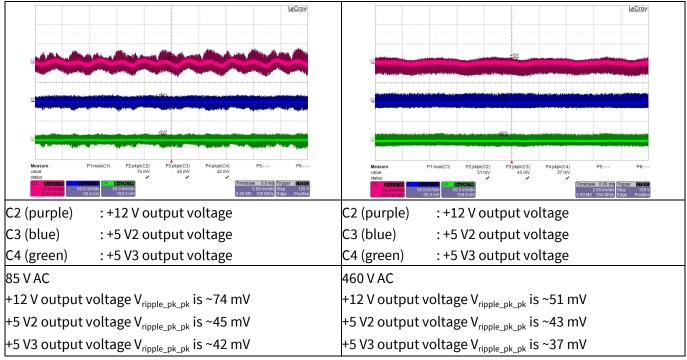


Figure 21 Output ripple voltage at full load. Probe terminals are decoupled with 10 μ F electrolytic and 0.1 μ F ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz



Waveforms and oscilloscope plots

10.7 Output ripple voltage at ABM

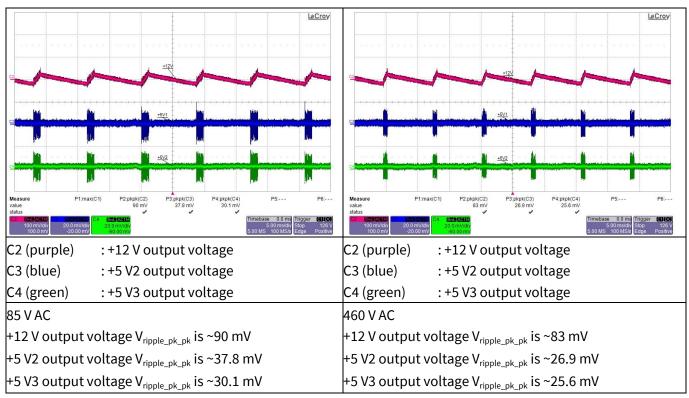


Figure 22 Output ripple voltage at minimum load. Probe terminals are decoupled with 10 μ F electrolytic and 0.1 μ F ceramic capacitors. Oscilloscope is bandwidth filter limited to 20 MHz

10.8 Entering ABM

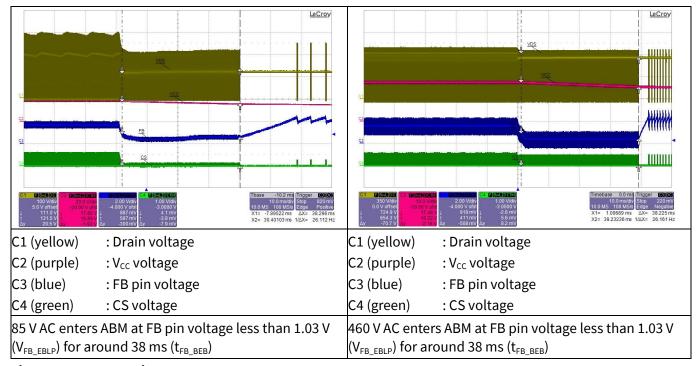


Figure 23 Entering ABM



Waveforms and oscilloscope plots

10.9 During ABM

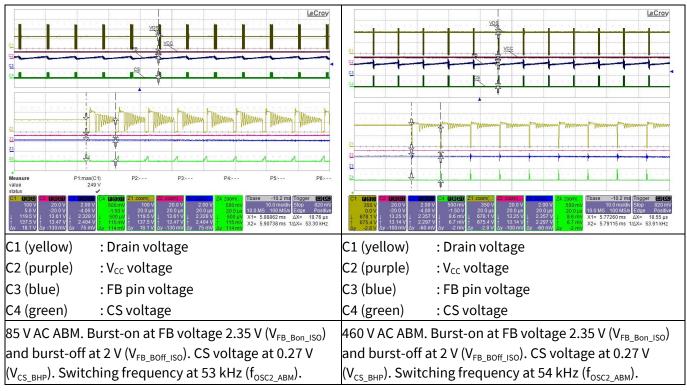


Figure 24 During ABM

10.10 Leaving ABM

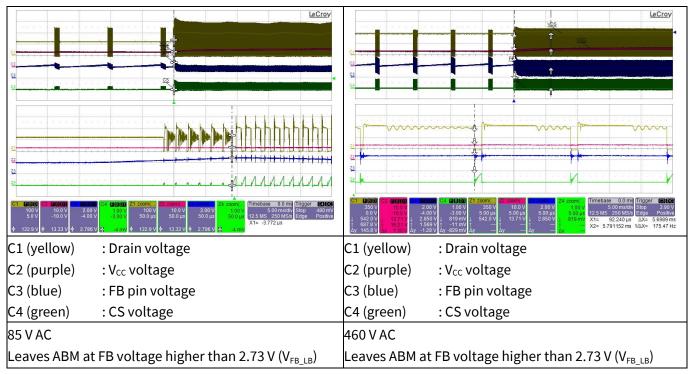


Figure 25 Leaving ABM



Waveforms and oscilloscope plots

10.11 V_{cc} OV/UV protection

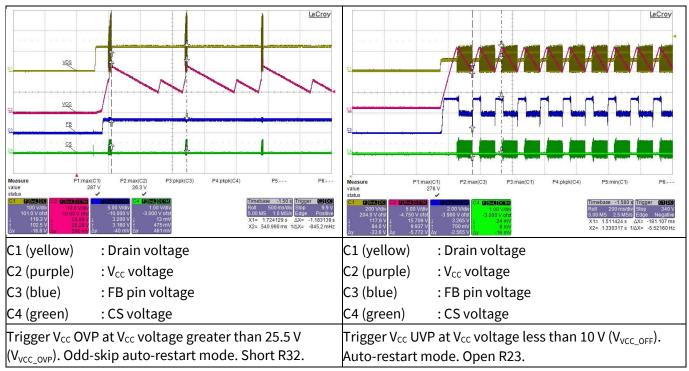


Figure 26 V_{cc} OV/UV protection

10.12 Overload protection

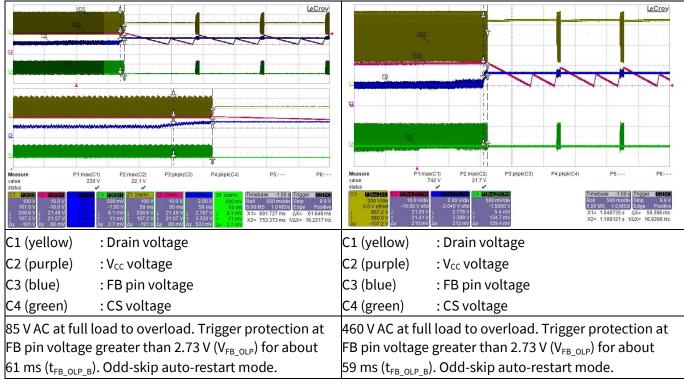
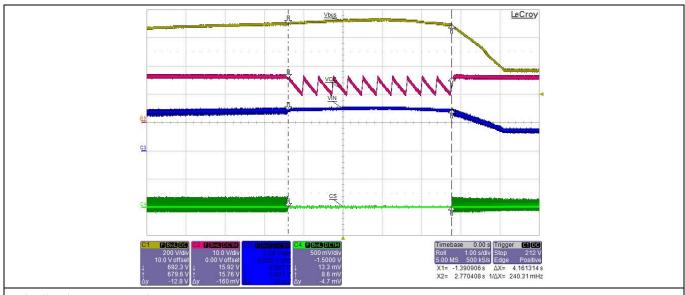


Figure 27 Overload protection



Waveforms and oscilloscope plots

10.13 Line overvoltage protection



C1 (yellow) : Bus voltage
C2 (purple) : V_{cc} voltage
C3 (blue) : VIN pin voltage
C4 (green) : CS voltage

Trigger LOVP at (692 V bus voltage/490 V AC), VIN pin voltage is greater than 2.85 V (V_{VIN LOVP}).

Non-switch auto-restart mode.

Resume switching when VIN pin voltage is lower than 2.85 V ($V_{VIN LOVP}$).

Figure 28 Line overvoltage protection



Appendix A: Transformer design and spreadsheet

11 Appendix A: Transformer design and spreadsheet

Calculation tool for FF flyback converter using fifth-generation CoolSET™ (Version 1.1)

Project:	REF_5BR3995CZ_16W1
Application:	Aux for metering
CoolSET™:	ICE5BR3995CZ
Date:	30 June 2021
Revision:	Version 1.1

Notes:

Enter design variables in orange-colored cells

Read design results in green-colored cells

Equation numbers are according to the design guide

Component designators refer to the calculation tool

 $Select\ component\ values\ based\ on\ standard\ values\ available$

Voltage/current rating does not include design margin, voltage spikes and transient currents

In "Output regulation", only fill in either isolated or non-isolated, whichever is applicable

Description	Eq. #	Parameter	Unit	Value
Input, output, CoolSET™ specs				
Line input				

Input	Minimum AC input voltage	V _{ACMin}	[V]	85
Input	Maximum AC input voltage	V _{ACMax}	[V]	460
Input	Line frequency	f _{AC}	[Hz]	60
Input	Bus capacitor DC ripple voltage	V _{DCRipple}	[V]	30

Output 1 specs

Input	Output voltage 1		V _{Out1}	[V]	12
Input	Output current 1		I _{Out1}	[A]	1
Input	Forward voltage of output diode 1		V _{FOut1}	[V]	0.6
Input	Output ripple voltage 1		V _{OutRipple1}	[V]	0.2
Result	Output power 1	Eq. 001	P _{Out1}	[W]	12
Result	Output load weight 1	Eq. 004	K _{L1}		0.79

Output 2 and 3 specs

Input	Output voltage 2		V _{Out2}	[V]	8
Input	Output current 2		I _{Out2}	[A]	0.2
Input	Forward voltage of output diode 2		V _{FOut2}	[V]	0.2
Input	Output ripple voltage 2		V _{OutRipple2}	[V]	0.2
Result	Output power 2	Eq. 002	P _{Out2}	[W]	1.6
Result	Output load weight 2	Eq. 005	K _{L2}		0.11
Input	Output voltage 3		V _{Out2}	[V]	8
Input	Output current 3		I _{Out2}	[A]	0.2
Input	Forward voltage of output diode 3		V _{FOut2}	[V]	0.2
Input	Output ripple voltage 3		V _{OutRipple2}	[V]	0.2
Result	Output power 3	Eq. 002	P _{Out2}	[W]	1.6
Result	Output load weight 3	Eq. 005	K _{L2}		0.11

Auxiliary

Input	V _{CC} voltage	V _{Vcc}	[V]	15
Input	Forward voltage of Vcc diode (D2)	V _{FVcc}	[V]	0.6

Power

Input	Efficiency		η		0.83
Result	Nominal output power	Eq. 003	P _{OutNom}	[W]	15.2



Appendix A: Transformer design and spreadsheet

Result Maximum input power for overload protection Eq. 006 P _{InMax} [W] 19.88 Input Minimum output power P _{OutMin} [W] 0.2	Input	Maximum output power for overload protection		P _{OutMax}	[W]	17
Input Minimum output power P _{OutMin} [W] 0.2	Result	Maximum input power for overload protection	Eq. 006	P _{InMax}	[W]	19.88
	Input	Minimum output power		P _{OutMin}	[W]	0.2

Controller/CoolSET™

	Controller/CoolSET™			ICE5BR3995CZ
Input	Switching frequency	fs	[Hz]	65000
Input	Targeted max. drain source voltage	V _{DSMax}	[V]	850
Input	Max. ambient temperature	T _{amax}	[°C]	50

Diode bridge and input capacitor

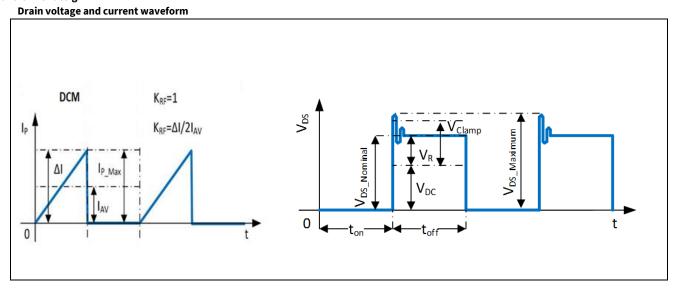
Diode bridge

Input	Power factor Power factor		cosφ		0.6
Result	Maximum AC input current	Eq. 007	I _{ACRMS}	[A]	0.39
Result	Peak voltage at V _{ACMax}	Eq. 008	$V_{DCMaxPk}$	[V]	650.54

Input capacitor

Result	Peak voltage at V _{ACMin}	Eq. 009	V _{DCMinPk}	[V]	120.21
Result	Selected minimum DC input voltage	Eq. 010	V _{DCMinSet}	[V]	90.21
Result	Discharging time at each half-line cycle	Eq. 011	T _D	[ms]	6.42
Result	Required energy at discharging time of input capacitor	Eq. 012	W _{In}	[Ws]	0.13
Result	Calculated input capacitor	Eq. 013	C _{INCal}	[μF]	40.42
Input	Select input capacitor (C1)		Cin	[μF]	47
Result	Calculated minimum DC input voltage	Eq. 015	V _{DCMin}	[V]	94.98

Transformer design



Primary inductance and winding currents

Primary in	ductance and winding currents				
Input	Reflection voltage		V _{RSET}	[V]	80
Result	Maximum duty cycle	Eq. 016	D _{Max}		0.46
Input	Select current ripple factor		K _{RF}		1
Result	Primary inductance	Eq. 017	L _P	[H]	7.30E-04
Result	Primary turn-on average current	Eq. 018	I _{AV}	[A]	0.46
Result	Primary peak-to-peak current	Eq. 019	ΔΙ	[A]	0.92
Result	Primary peak current	Eq. 020	I _{PMax}	[A]	0.92
Result	Primary valley current	Eq. 021	I _{Valley}	[A]	0.00
Result	Primary RMS current	Eq. 022	I _{PRMS}	[A]	0.357

Select core type

Input Select core type			2
------------------------	--	--	---



Appendix A: Transformer design and spreadsheet

Result	Core type			E25/13/7
Result	Core material			N87
Result	Maximum flux density	B _{Max}	[T]	0.3
Result	Cross-sectional area	Ae	[mm²]	52
Result	Bobbin width	BW	[mm]	15.6
Result	Winding cross-section	A _N	[mm ²]	61
Result	Average length of turn	l _N	[mm]	50

Winding calculation

Result	Calculated minimum number of primary turns	Eq. 023	N _{PCal}	Turns	42.82
Input	Select number of primary turns		N _P	Turns	58
Result	Calculated number of secondary 1 turns	Eq. 024	Eq. 024 N _{S1Cal}	Turns	9.14
Input	Select number of secondary 1 turns		N _{S1}	Turns	9
Result	Calculated number of secondary 2 turns	Eq. 025	N _{S2Cal}	Turns	5.95
Input	Select number of secondary 2 turns		N _{S2}	Turns	6
Result	Calculated number of auxiliary turns	Eq. 026	N _{VccCal}	Turns	11.14
Input	Select number of auxiliary turns		N _{Vcc}	Turns	10
Result	Calculated V _{CC} voltage	Eq. 027	V _{VccCal}	[V]	13.40

Post calculation

Result	Primary to secondary 1 turns ratio	Eq. 028	N _{PS1}		6.44
Result	Primary to secondary 2 turns ratio	Eq. 029	N _{PS2}		9.67
Result	Post-calculated reflected voltage	Eq. 030	V _{RPost}	[V]	81.20
Result	Post-calculated maximum duty cycle	Eq. 031	D _{MaxPost}		0.46
Result	Duty cycle prime	Eq. 032	D _{Max} '		0.53
Result	Actual flux density	Eq. 033	B _{MaxAct}	[T]	0.222
Result	Maximum DC input voltage for CCM operation	Eq. 034	V _{DCmaxCCM}	[V]	93.34

Transformer winding design

Input	Margin according to safety standard		М	[mm]	0
Input	Copper space factor		fcu		0.4
Result	Effective bobbin window	Eq. 035	BW _E	[mm]	15.6
Result	Effective winding cross-section	Eq. 036	A _{Ne}	[mm²]	61.0
Input	Primary winding area factor		AF _{NP}		0.45
Input	Secondary 1 winding area factor		AF _{NS1}		0.25
Input	Secondary 2 winding area factor		AF _{NS2}		0.20
Input	Auxiliary winding area factor		AF _{NVcc}		0.10

Primary winding

Result	Calculated copper wire cross-sectional area	Eq. 037	A _{PCal}	[mm²]	0.1893
Result	Calculated maximum wire size	Eq. 038	AWG _{PCal}		24
Input	Select wire size		AWG _P		28
Input	Select number of parallel wire		nw _P		1
Result	Copper wire diameter	Eq. 039	d₽	[mm]	0.32
Result	Copper wire cross-sectional area	Eq. 040	A _P	[mm²]	0.0821
Result	Wire current density	Eq. 041	S _P	[A/mm ²]	4.35
Input	Insulation thickness		INS _P	[mm]	0.01
Result	Turns per layer	Eq. 042	NL _P	Turns/layer	45
Result	Number of layers	Eq. 043	Ln _P	Layers	2

Secondary 1 winding

Result	Calculated copper wire cross-sectional area	Eq. 044	A _{NS1Cal}	[mm²]	0.6778
Result	Calculated maximum wire size	Eq. 045	AWG _{S1Cal}		19
Input	Select wire size		AWG _{S1}		22



Appendix A: Transformer design and spreadsheet

Input	Select number of parallel wires		nw _{S1}		1
Result	Copper wire diameter	Eq. 046	d _{S1}	[mm]	0.6465
Result	Copper wire cross-sectional area	Eq. 047	A _{S1}	[mm²]	0.3282
Result	Peak current	Eq. 048	I _{S1Max}	[A]	4.6537
Result	RMS current	Eq. 049	I _{S1RMS}	[A]	1.9648
Result	Wire current density	Eq. 050	S _{S1}	[A/mm ²]	5.99
Input	Insulation thickness		INS _{S1}	[mm]	0.02
Result	Turns per layer	Eq. 051	NL _{S1}	Turns/layer	9
Result	Number of layers	Eq. 052	Ln _{S1}	Layers	1

Secondary 2 winding

)				
Result	Calculated copper wire cross-sectional area	Eq. 053	A _{NS2Cal}	[mm²]	0.8133
Result	Calculated maximum wire size	Eq. 054	AWG _{S2Cal}		18
Input	Select wire size		AWG _{S2}		26
Input	Select number of parallel wires		nw _{S2}		1
Result	Copper wire diameter	Eq. 055	d _{S2}	[mm]	0.4073
Result	Copper wire cross-sectional area	Eq. 056	A _{S2}	[mm²]	0.1303
Result	Peak current	Eq. 057	I _{S2Max}	[A]	0.9307
Result	RMS current	Eq. 058	I _{S2RMS}	[A]	0.3930
Result	Wire current density	Eq. 059	S _{S2}	[A/mm ²]	3.02
Input	Insulation thickness		INS _{S2}	[mm]	0.02
Result	Turns per layer	Eq. 060	NL _{S2}	Turns/layer	34
Result	Number of layers	Eq. 061	Ln _{S2}	Layers	1

RCD clamper and CS resistor

RCD clamper circuit

Input	Leakage inductance percentage		L _{LK%}	[%]	1
Result	Leakage inductance	Eq. 062	L _{LK}	[H]	7.30E-06
Result	Clamping voltage	Eq. 063	V _{Clamp}	[V]	118.26
Result	Calculated clamping capacitor	Eq. 064	C _{ClampCal}	[nF]	0.26
Input	Select clamping capacitor value (C2)		C _{clamp}	[nF]	1
Result	Calculated clamping resistor	Eq. 065	R _{clampCal}	[kΩ]	167.0
Input	Select clamping resistor value (R4)		R _{clamp}	[k Ω]	400

CS resistor

Input	CS threshold value from datasheet		V _{CS_N}	[V]	0.8
Result	Calculated current sense resistor (R8A, R8B)	Eq. 066	R _{sense}	[Ω]	0.87

Output rectifier

Secondary 1 output rectifier

Result	Diode reverse voltage	Eq. 067	V _{RDiode1}	[V]	112.95
Result	Diode RMS current		I _{S 1RMS}	[A]	1.96
Input	Max. voltage undershoot at output capacitor		Δ V _{Out1}	[V]	0.3
Input	Number of clock periods		n _{cp1}		20
Result	Output capacitor ripple current	Eq. 068	I _{Ripple1}	[A]	1.69
Result	Calculated minimum output capacitor	Eq. 069	C _{Out1Cal}	[μF]	1026
Input	Select output capacitor value (C152)		C _{Out1}	[μF]	1000
Input	ESR (Z _{max}) value from datasheet at 100 kHz		R _{ESR1}	[Ω]	0.032
Input	Number of parallel capacitors		nc _{COut1}		1
Result	Zero frequency of output capacitor	Eq. 070	f _{ZCOut1}	[kHz]	4.97
Result	First-stage ripple voltage	Eq. 071	V _{Ripple1}	[V]	0.148919
Input	Select LC filter inductor value (L151)		L _{out1}	[μH]	4.7
Result	Calculated LC filter capacitor	Eq. 072	C _{LCCal1}	[μF]	217.9
Input	Select LC filter capacitor value (C153)		C _{LC1}	[μF]	220



Appendix A: Transformer design and spreadsheet

Result	LC filter frequency	Eq. 073	f _{LC1}	[kHz]	4.95
Result	Second-stage ripple voltage	Eq. 074	V _{2ndRipple1}	[mV]	0.86
		•			
	ry 2 output rectifier	F., 075	W	Da	75.20
Result	Diode reverse voltage	Eq. 075	V _{RDiode2}	[V]	75.30
Result	Diode RMS current May yeltars undersheet at output capacitar		I _{S2RMS}	[A]	0.39
Input	Max. voltage undershoot at output capacitor		Δ V _{Out1}	[V]	0.15
Input Result	Number of clock periods Output capacitor ripple current	Eq. 076	n _{cp2}	[A]	0.34
Result	Calculated minimum output capacitor	Eq. 077	I _{Ripple2}	[A] [μF]	410
Input	Select output capacitor value (C152)	Eq. 011	Cout2Cal	[μF]	330
ode and o	apacitor		Cours	[6,1]	
	and capacitor		· ·	5.0	
Result	Auxiliary diode reverse voltage (D2)	Eq. 083	V _{RDiodeVCC}	[V]	125.56
Input	Soft-start time from datasheet		t _{ss}	[ms]	12
Input	lvcc,charge3 from datasheet		lvcc_charge3	[mA]	2
Input	V _{cc} on-threshold		V _{VCC_ON}	[V]	16
Input	V _{cc} off-threshold		V _{VCC_OFF}	[V]	10
Result	Calculated V _{CC} capacitor	Eq. 084	Cvcccal	[μF]	22.00
Input	Select V _{CC} capacitor (C3)		Cvcc	[μF]	22
Input	V _{CC} short threshold from datasheet		V _{VCC_SCP}	[V]	1.1
Input Result	lvcc_charge1 from datasheet Start-up time	Eq. 085	lvcc_charge1	[mA]	284.90
Result	Diode bridge power loss	Eq. 086	P _{DIN}	[W]	0.78
Transfor	mer copper				
Result	Primary winding copper resistance	Eq. 087	R _{PCu}	$[m\Omega]$	607.52
Result	Secondary 1 winding copper resistance	Eq. 088	R _{S1Cu}	[m Ω]	23.58
Result	Secondary 2 winding copper resistance	Eq. 089	R _{S2Cu}	[m Ω]	23.36
Result	Primary winding copper loss		_		
Result	Secondary 1 winding copper loss	Eq. 090	P _{PCu}	[mW]	
		Eq. 091	P _{S1Cu}		39.60 77.62 91.04
Result	Secondary 2 winding copper loss	Eq. 091 Eq. 092	P _{S1Cu}	[mW] [mW]	39.60 77.62
Result Result		Eq. 091	PsiCu	[mW]	39.60 77.62 91.04 6.12
Result Output re	Secondary 2 winding copper loss Total transformer copper loss ectifier diode	Eq. 091 Eq. 092 Eq. 093	Ps1cu Ps2cu Pcu	[mW] [mW] [mW] [W]	39.60 77.62 91.04 6.12 0.1748
Result Output re	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss	Eq. 091 Eq. 092 Eq. 093	Ps1cu Ps2cu Pcu Pbiode1	[mW] [mW] [mW] [W]	39.60 77.62 91.04 6.12 0.1748
Result Output r	Secondary 2 winding copper loss Total transformer copper loss ectifier diode	Eq. 091 Eq. 092 Eq. 093	Ps1cu Ps2cu Pcu	[mW] [mW] [mW] [W]	39.60 77.62 91.04 6.12 0.1748
Output re Result Result RCD clan	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss per circuit	Eq. 091 Eq. 092 Eq. 093 Eq. 094 Eq. 095	Psicu Pszcu Pcu Pbiodei Pbiode2	[mW] [mW] [mW] [W]	39.60 77.62 91.04 6.12 0.1748 1.18 0.08
Output re Result Result RCD clan Result	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss per circuit RCD clamper loss	Eq. 091 Eq. 092 Eq. 093	Ps1cu Ps2cu Pcu Pbiode1	[mW] [mW] [mW] [W]	39.60 77.62 91.04 6.12 0.1748
Output re Result Result RCD clan Result Current s	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss per circuit RCD clamper loss sense resistor	Eq. 091 Eq. 092 Eq. 093 Eq. 094 Eq. 095	Ps1Cu Ps2Cu Pcu Pbiode1 Pbiode2 Pclamper	[mW] [mW] [mW] [W] [W] [W]	39.60 77.62 91.04 6.12 0.1748 1.18 0.08
Output re Result Result RCD clan Result Current se	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss per circuit RCD clamper loss	Eq. 091 Eq. 092 Eq. 093 Eq. 094 Eq. 095	Psicu Pszcu Pcu Pbiodei Pbiode2	[mW] [mW] [mW] [W]	39.60 77.62 91.04 6.12 0.1748 1.18 0.08
Result Result RCD clan Result Currents Result MOSFET	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss sense resistor CS resistor loss	Eq. 091 Eq. 092 Eq. 093 Eq. 094 Eq. 095	PS1Cu PS2Cu PCu PDiode1 PDiode2 PClamper PCS	[mW] [mW] [mW] [w] [w] [w] [w]	39.60 77.62 91.04 6.12 0.1748 1.18 0.08
Result Result RCD clan Result Currents Result MOSFET	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss nper circuit RCD clamper loss sense resistor CS resistor loss RDS(on) from datasheet	Eq. 091 Eq. 092 Eq. 093 Eq. 094 Eq. 095	Psicu Psicu Psicu Prodei Poiodei Pbiodei Pclamper Pcs Ros(on) at Ta = 125°C	[mW] [mW] [mW] [w] [w] [w] [w] [w]	39.60 77.62 91.04 6.12 0.1748 1.18 0.08 0.34
Result Result RCD clan Result Current s Result MOSFET Input Input	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss per circuit RCD clamper loss sense resistor CS resistor loss RDS(on) from datasheet Co(er) from datasheet	Eq. 091 Eq. 092 Eq. 093 Eq. 094 Eq. 095	Psicu Pszcu Pcu Pbiode1 Pbiode2 Pclamper Pcs Rbs(on) at TA = 125°C Co(er)	[mW] [mW] [mW] [w] [w] [w] [w] [w] [pF]	39.60 77.62 91.04 6.12 0.1748 1.18 0.08 0.34 0.11
Result Result RCD clan Result Currents Result MOSFET	Secondary 2 winding copper loss Total transformer copper loss ectifier diode Secondary 1 diode loss Secondary 2 diode loss nper circuit RCD clamper loss sense resistor CS resistor loss RDS(on) from datasheet	Eq. 091 Eq. 092 Eq. 093 Eq. 094 Eq. 095	Psicu Psicu Psicu Prodei Poiodei Pbiodei Pclamper Pcs Ros(on) at Ta = 125°C	[mW] [mW] [mW] [w] [w] [w] [w] [w]	39.60 77.62 91.04 6.12 0.1748 1.18 0.08

Eq. 099

 $P_{condMinAC} \\$

[W]

0.9825

Result

Conduction loss at minimum AC input voltage



Appendix A: Transformer design and spreadsheet

Result	Total MOSFET loss at minimum AC input voltage	Eq. 100	P _{MOSMinAC}	[W]	1.0127
Result	Switch-on loss at maximum AC input voltage	Eq. 101	P _{SONMaxAC}	[W]	0.5221
Result	Conduction loss at maximum AC input voltage	Eq. 102	$P_{condMaxAC}$	[W]	0.1434
Result	Total MOSFET loss at maximum AC input voltage	Eq. 103	P _{MOSMaxAC}	[W]	0.6655
Result	Total MOSFET loss (from minimum or maximum AC)		P _{MOS}	[W]	1.0127

Controller

Input	Controller current consumption		I _{VCC_Normal2}	[mA]	2
Result	Controller loss	Eq. 104	P _{Ctrl}	[W]	0.027

Efficiency after losses

Result	Total power loss	Eq. 105	P _{Losses}	[W]	3.70
Result	Post calculated efficiency	Eq. 106	η _{Post}	%	81.68%

CoolSET™/MOSFET temperature

CoolSET™/MOSFET temperature

Input	Enter thermal resistance junction-ambient (include copper pour)		R _{thJA_As}	[°K/W]	80
Result	Temperature rise	Eq. 107	ΔΤ	[°K]	81.1
Result	Junction temperature at T _{amax}	Eq. 108	Tjmax	°C	131.1

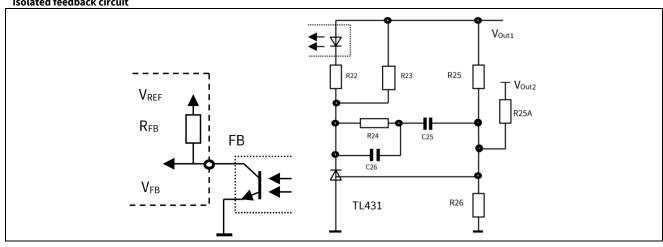
Line OVP

Line OVP

Input	Select AC input LOVP		V _{OVP_AC}	[V AC]	500
Input	High-side DC input voltage divider/resistor (R3A, R3B, R3C)		R _{I1}	[ΜΩ]	5
Input	Controller LOVP threshold		V _{VIN_LOVP}	[V]	2.85
Result	Low-side DC input voltage divider/resistor	Eq. 109	R _{I2Cal}	[kΩ]	20.23
Input	Select low-side DC input voltage divider/resistor (R7)		R ₁₂	[k Ω]	20.5
Result	Post-calculated LOVP	Eq. 110	V _{OVP_ACPost}	[V AC]	493.54

Output regulation (isolated using TL431 and optocoupler)

Isolated feedback circuit



Output regulation

	,				
Input	TL431 reference voltage		V _{REF_TL}	[V]	2.5
Input	Weighted regulation factor of V _{Out1}		W ₁		1
Input	Current for voltage divider/resistor R26		I _{R26}	[mA]	0.25
Result	Calculated voltage divider/resistor	Eq. 111	R26 _{Cal}	[k Ω]	10
Input	Select voltage divider/resistor value		R26	$[k\Omega]$	10
Result	Calculated voltage divider/resistor	Eq. 112	R25 _{Cal}	[k Ω]	38.00
Input	Select voltage divider/resistor value		R25	[k Ω]	38.0

Optocoupler and TL431 bias

Input Current transfer ratio (CTR)	Gc	[Percent]	200%
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Appendix A: Transformer design and spreadsheet

Input	Optocoupler diode forward voltage		V _{FOpto}	[V]	1.25
Input	Maximum current for optocoupler diode		I _{Fmax}	[mA]	50
Input	Minimum current for TL431		I _{KAmin}	[mA]	1
Result	Calculated minimum optocoupler bias resistance	Eq. 114	R22 _{Cal}	[k Ω]	0.1650
Input	Select optocoupler bias resistor		R22	[k Ω]	1
Input	FB pull-up reference voltage V _{REF} from datasheet		V _{REF}	[V]	3.3
Input	V _{FB_OLP} from datasheet		V _{FB_OLP}	[V]	2.75
Input	R _{FB} from datasheet		R _{FB}	[kΩ]	15
Result	Calculated maximum TL431 bias resistance	Eq. 115	R23 _{Cal}	[kΩ]	1.27
Input	Selected TL431 bias resistor		R23	[kΩ]	1

Regulation loop

Regulati	on toop				
Result	FB transfer characteristic	Eq. 116	K _{FB}		30.00
Result	Gain of FB transfer characteristic	Eq. 117	G _{FB}	[db]	29.54
Result	Voltage divider transfer characteristic	Eq. 118	K _{VD}		0.208333
Result	Gain of voltage divider transfer characteristic	Eq. 119	G _{VD}	[db]	-13.62
Result	Resistance at maximum load pole	Eq. 120	R _{LH}	[Ω]	8.73
Result	Resistance at minimum load pole	Eq. 121	R _{LL}	[Ω]	48.00
Result	Poles of power stage at maximum load pole	Eq. 122	fон	[Hz]	36.47
Result	Poles of power stage at minimum load pole	Eq. 123	foL	[Hz]	6.63
Result	Zero frequency of the compensation network	Eq. 124	fом	[Hz]	15.55
Input	Zero dB crossover frequency		fg	[kHz]	5
Input	PWM-OP gain from datasheet		A _V		2.03
Result	Transient impedance	Eq. 117	Z _{PWM}	[V/A]	2.2
Result	Power stage at crossover frequency	Eq. 118	F _{PWR} (fg)		0.043
Result	Gain of power stage at crossover frequency	Eq. 119	G _{PWR} (fg)	[db]	-27.31
Result	Gain of the regulation loop at fg	Eq. 120	Gs(ω)	[db]	-11.389
Result	Separated components of the regulator	Eq. 121	Gr(ω)	[db]	11.389
Result	Calculated resistance value of compensation network	Eq. 122	R24 _{Cal}	[k Ω]	29.38
Input	Select resistor value of compensation network		R24	[k Ω]	22
Result	Calculated capacitance value of compensation network	Eq. 123	C26 _{Cal}	[nF]	1.447
Input	Select capacitor value of compensation network		C26	[nF]	1
Result	Calculated capacitance value of compensation network	Eq. 124	C25 _{Cal}	[nF]	464.17
Input	Select capacitor value of compensation network		C25	[nF]	220

Final design

Electrical

Minimum AC voltage	[V]	85
Maximum AC voltage	[V]	460
Maximum input current	[A]	0.23
Minimum DC voltage	[V]	95
Maximum DC voltage	[V]	651
Maximum output power	[W]	16.5
Output voltage 1	[V]	12.0
Output ripple voltage 1	[mV]	0.9
Output voltage 1	[V]	8.0
Output ripple voltage 1	[mV]	0.0
Transformer peak current	[A]	0.92
Maximum duty cycle		0.46
Reflected voltage	[V]	81
Copper losses	[W]	0.17
MOSFET losses	[W]	1.01
Sum losses	[W]	3.70
Efficiency	[Percent]	81.68%

Transformer_

Core type	Core type			E25/13/7
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Appendix A: Transformer design and spreadsheet

Core material			N87
Effective core area		[mm²]	52
Maximum flux density		[mT]	222
Inductance		[μH]	730
Margin		[mm]	0
Primary turns		Turns	58
Primary copper wire size		AWG	28
Number of primary copper wires in parallel			1
Primary layers		Layer	2
Secondary 1 turns (N _{S1})		Turns	9
Secondary 1 copper wire size		AWG	22
Number of secondary 1 copper wires in parallel			1
Secondary 1 layers		Layer	1
Secondary 2 turns (N _{S2})		Turns	6
Secondary 2 copper wire size		AWG	26
Number of secondary 2 copper wires in parallel			1
Secondary 2 layers		Layer	1
Auxiliary turns		Turns	10
Leakage inductance		[μH]	7.3

Components

Input capacitor (C1)	[μF]	47.0
Secondary 1 output capacitor (C152)	[μF]	1000.0
Secondary 1 output capacitor in parallel		1.0
Secondary 1 LC filter inductor (L151)	[μH]	4.7
Secondary 1 LC filter capacitor (C153)	[μF]	220.0
Secondary 2 output capacitor (C102)	[μF]	330.0
Secondary 2 output capacitor in parallel		1.0
V _{CC} capacitor (C3)	[μF]	22.0
Sense resistor (R8A, R8B)	[Ω]	0.87
Clamping resistor (R4)	[k Ω]	400.0
Clamping capacitor (C2)	[nF]	1
High-side DC input voltage divider/resistor (R3A, R3B, R3C)	[MΩ]	5000.0
Low-side DC input voltage divider/resistor (R7)	[kΩ]	20.5

Regulation components (isolated using TL431 and optocoupler)

Voltage divider	R26	[k Ω]	10.0
Voltage divider (V _{out1} sense)	R25	[kΩ]	38.0
Optocoupler bias resistor	R22	[kΩ]	1.00
TL431 bias resistor	R23	[kΩ]	1.0
Compensation network resistor	R24	[kΩ]	22.0
Compensation network capacitor	C26	[nF]	1.00
Compensation network capacitor	C25	[nF]	220.0



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12 References

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Revision history

Revision history

Document version	Date of release	Description of changes
V 1.0	2022-06-15	First release

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