

MOSFET

OptiMOS™5 Power-Transistor, 100 V

Features

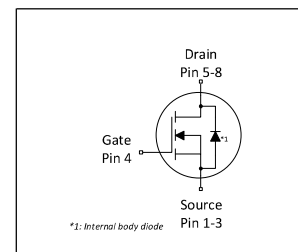
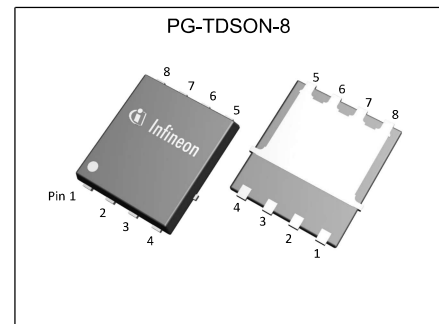
- Ideal for high-frequency switching
- Optimized for chargers
- 100% avalanche tested
- Superior thermal resistance
- N-channel, logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	100	V
$R_{DS(on),max}$	7.8	m Ω
I_D	71	A
Q_{oss}	34	nC
$Q_G(0V..4.5V)$	13	nC



Type / Ordering Code	Package	Marking	Related Links
ISC0805NLS	PG-TDSON-8	0805NL	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	71 54 13	A	$V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^2)$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	284	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	58	mJ	$I_D=30\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	74 2.5	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}^2)$
Operating and storage temperature	T_j , T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case, bottom	R_{thJC}	-	1.0	1.7	°C/W	-
Thermal resistance, junction - case, top	R_{thJC}	-	-	20	°C/W	-
Device on PCB, 6 cm ² cooling area ²⁾	R_{thJA}	-	-	50	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	1.1	1.6	2.3	V	$V_{DS}=V_{GS}$, $I_D=40\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	μA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	10	100	nA	$V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	7.2 9.2	7.8 10.7	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=4.5\text{ V}$, $I_D=25\text{ A}$
Gate resistance	R_G	-	1.1	-	Ω	-
Transconductance	g_{fs}	-	73	-	S	$ V_{DS} \geq 2 I_D /R_{DS(on)max}$, $I_D=50\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	1700	2200	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	280	360	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	13	23	pF	$V_{GS}=0\text{ V}$, $V_{DS}=50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	6.7	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Rise time	t_r	-	21	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$
Fall time	t_f	-	3.8	-	ns	$V_{DD}=50\text{ V}$, $V_{GS}=4.5\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=3\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	6.0	-	nC	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	2.9	-	nC	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate to drain charge	Q_{gd}	-	4.7	-	nC	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Switching charge	Q_{sw}	-	7.8	-	nC	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	13	16	nC	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	3.4	-	V	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	25	33	nC	$V_{DD}=50\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$
Gate charge total, sync. FET	$Q_{g(sync)}$	-	22	-	nC	$V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$
Output charge	Q_{oss}	-	34	-	nC	$V_{DS}=50\text{ V}$, $V_{GS}=0\text{ V}$

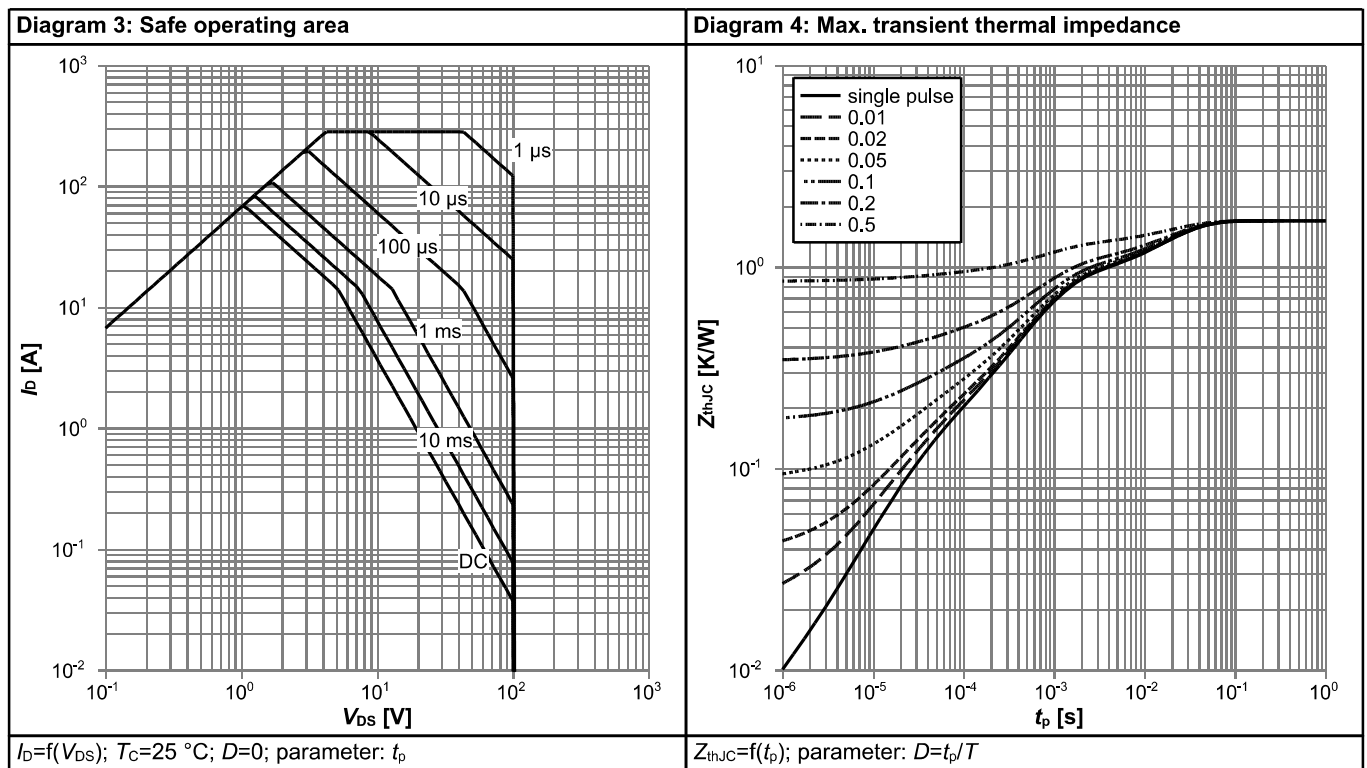
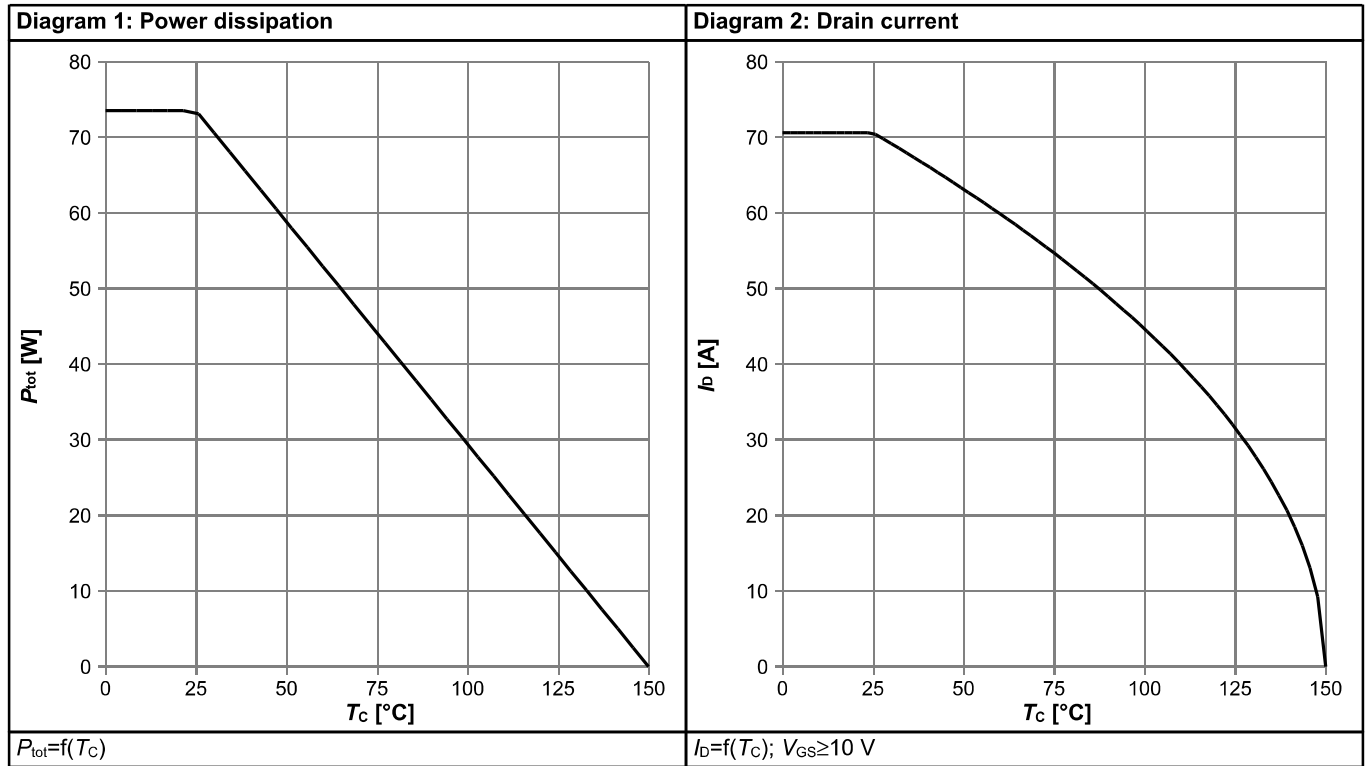
¹⁾ Defined by design. Not subject to production test.

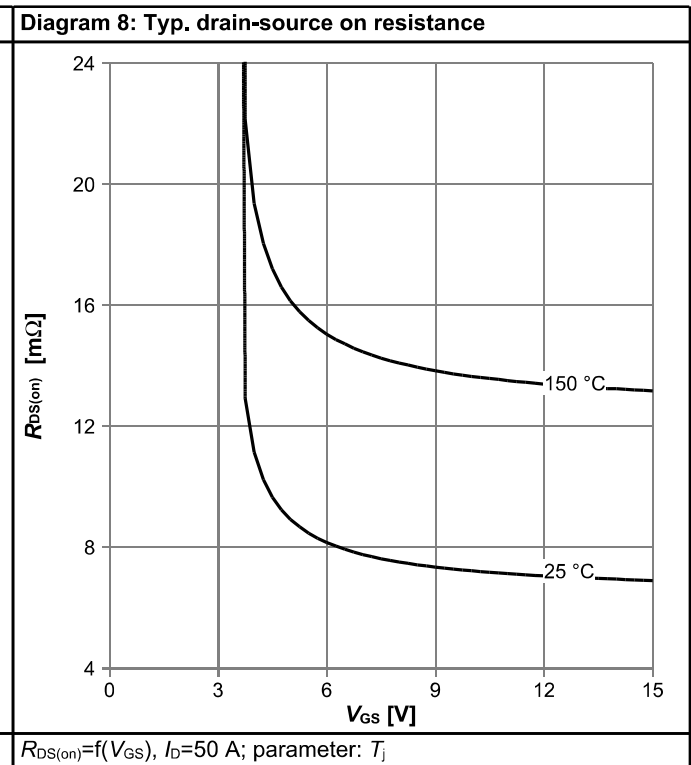
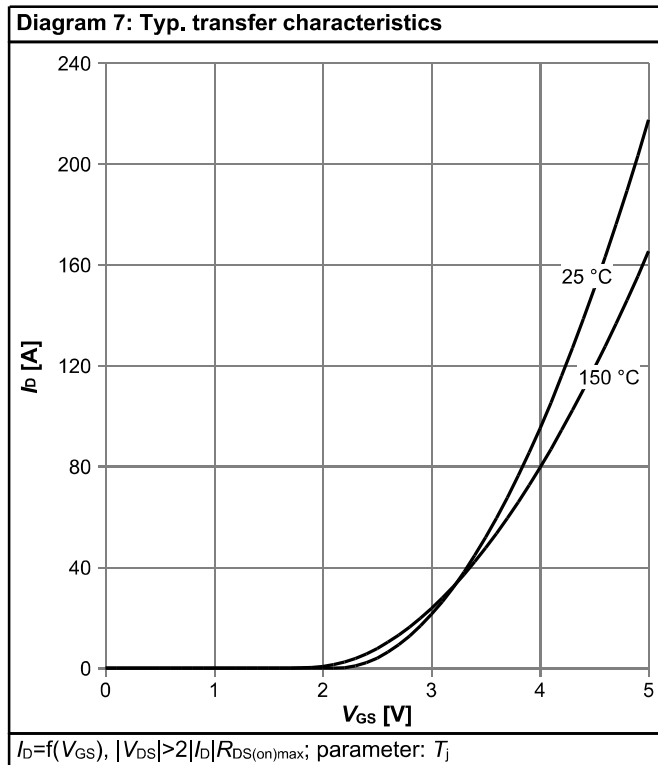
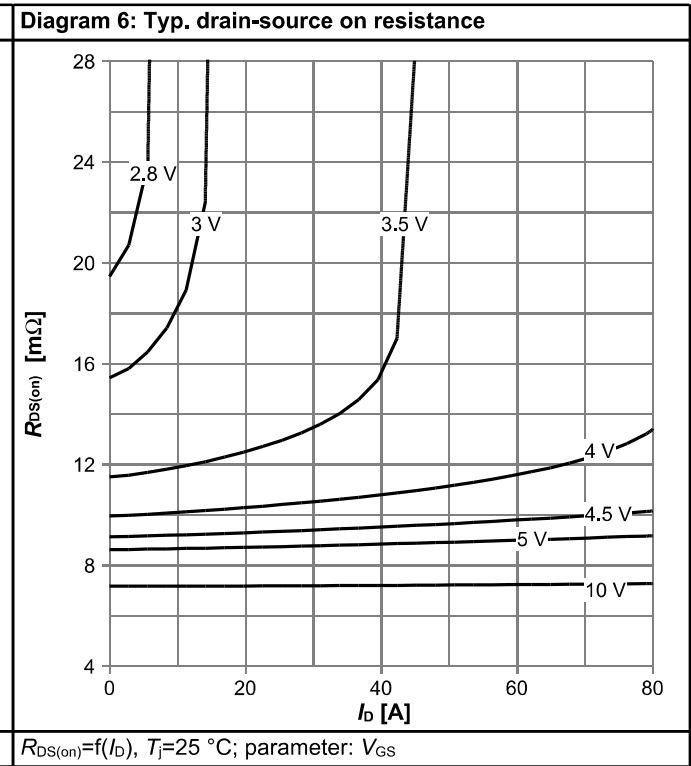
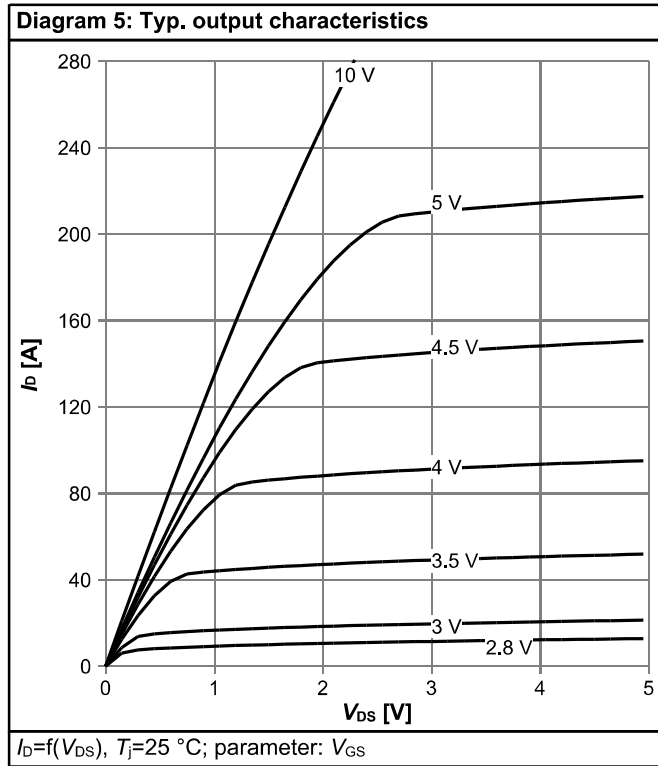
²⁾ See "Gate charge waveforms" for parameter definition

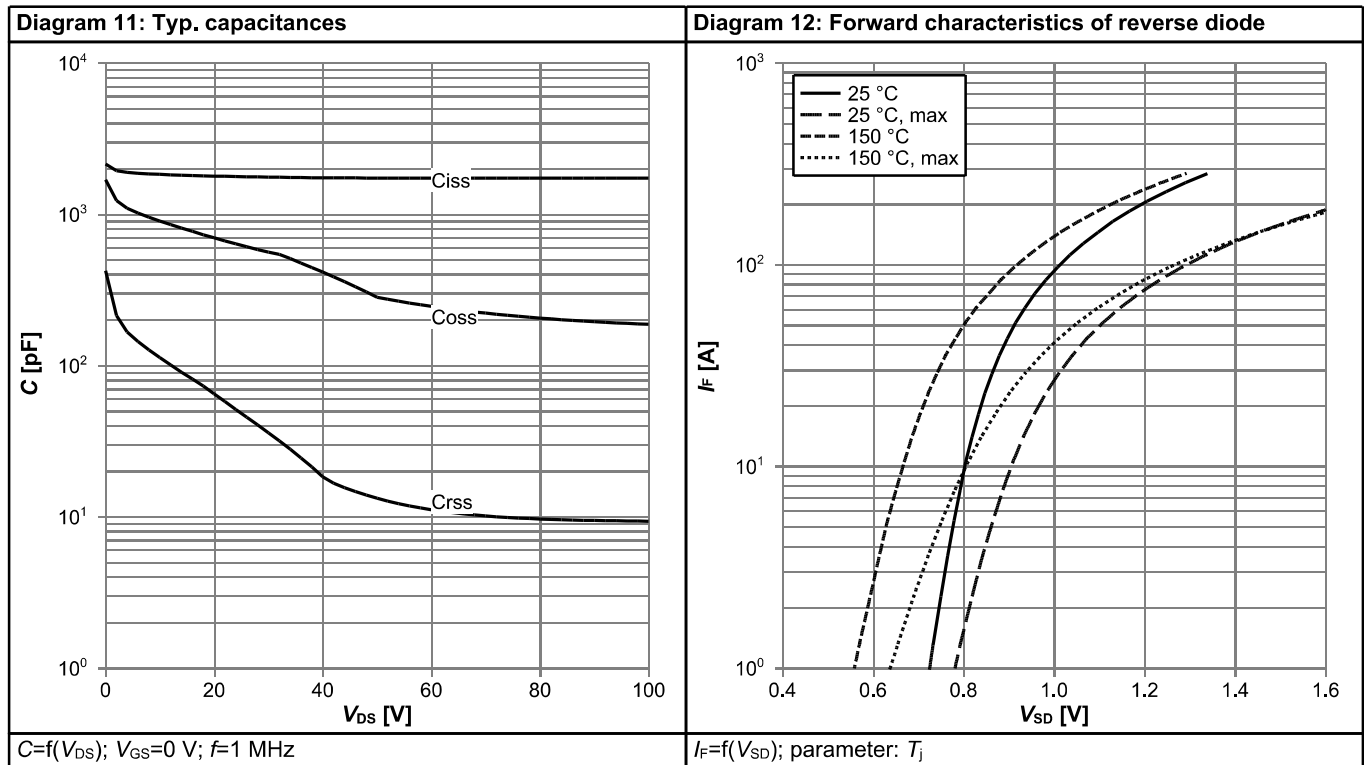
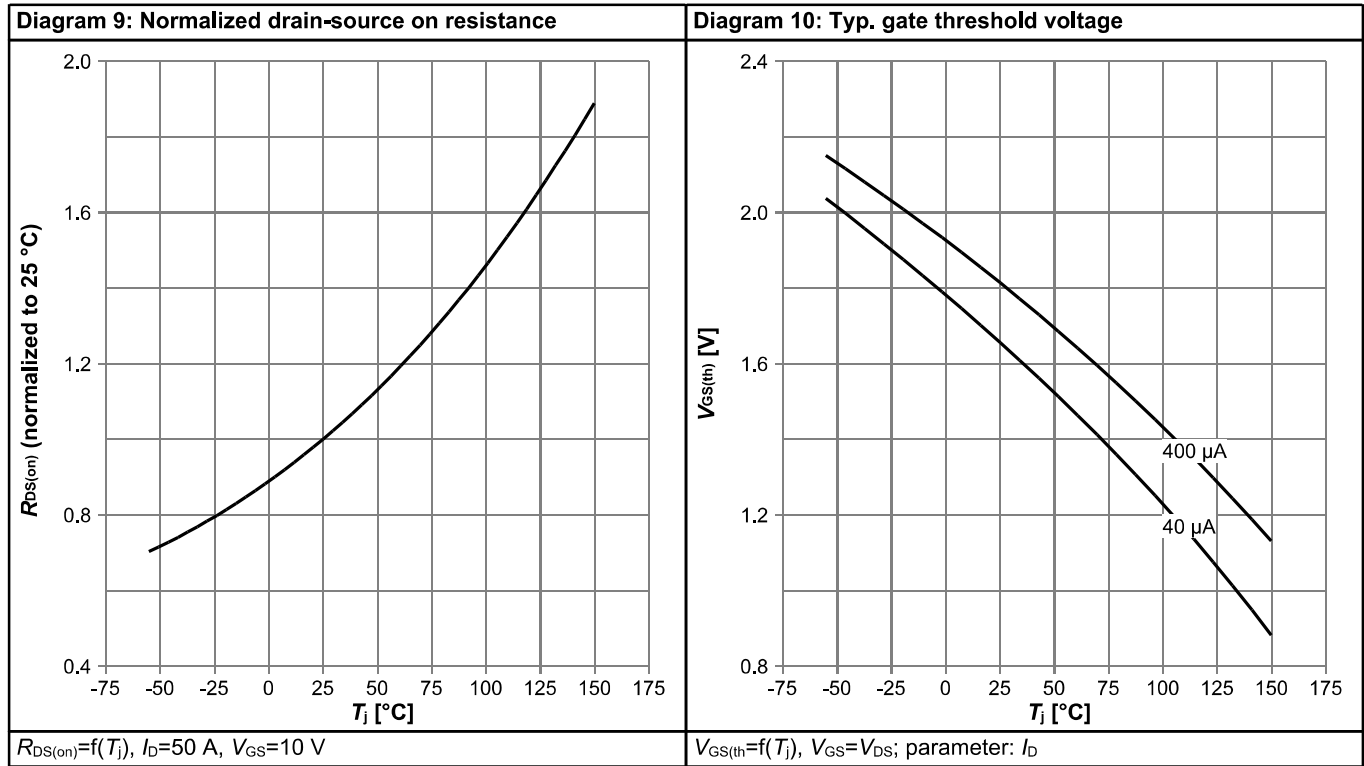
Table 7 Reverse diode

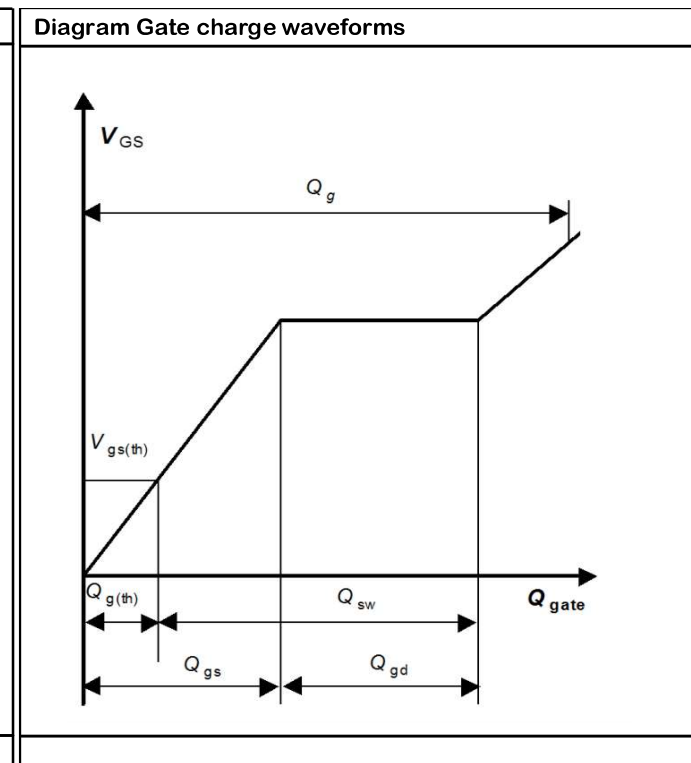
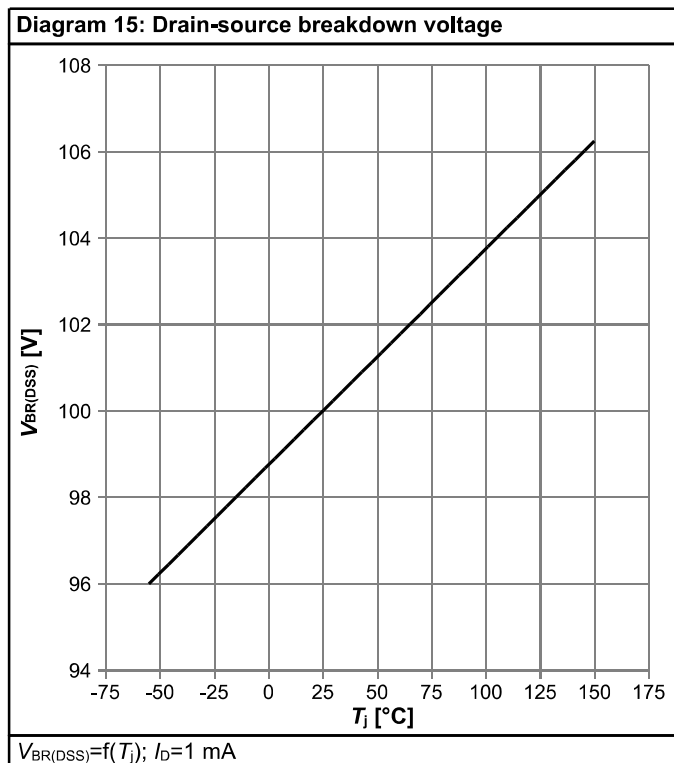
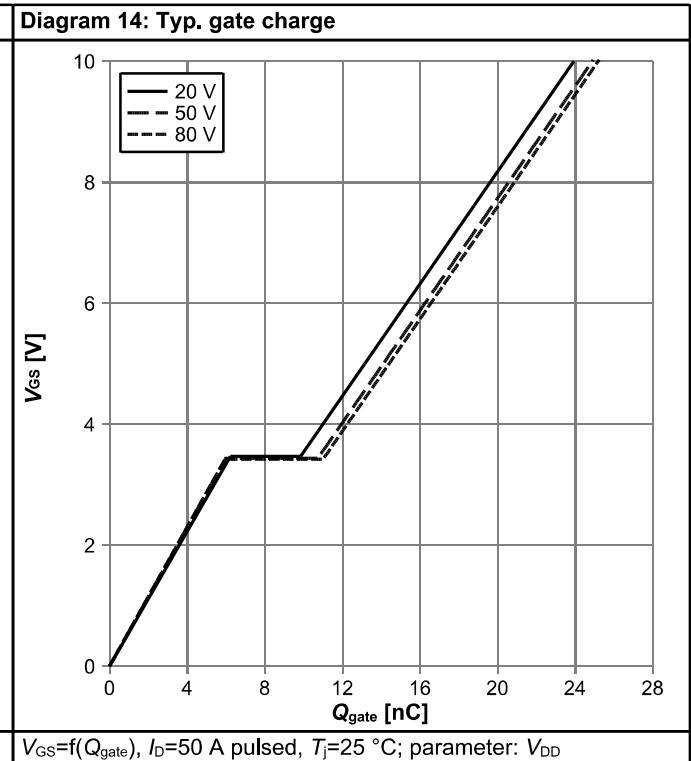
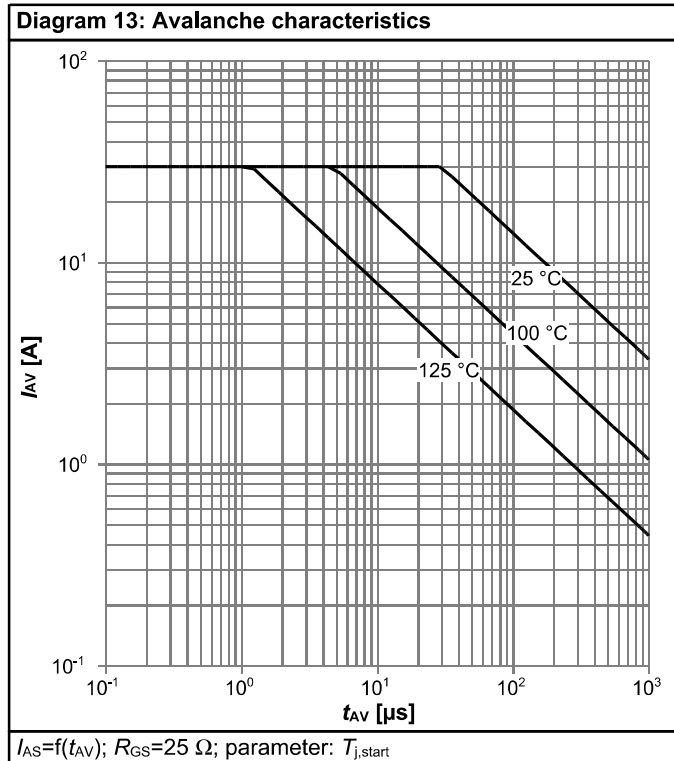
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	66	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	284	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	0.92	1.1	V	$V_{GS}=0\text{ V}, I_F=50\text{ A}, T_j=25\text{ °C}$
Reverse recovery time	t_{rr}	-	33	-	ns	$V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$
Reverse recovery charge	Q_{rr}	-	28	-	nC	$V_R=50\text{ V}, I_F=50\text{ A}, di_F/dt=100\text{ A}/\mu\text{s}$

4 Electrical characteristics diagrams

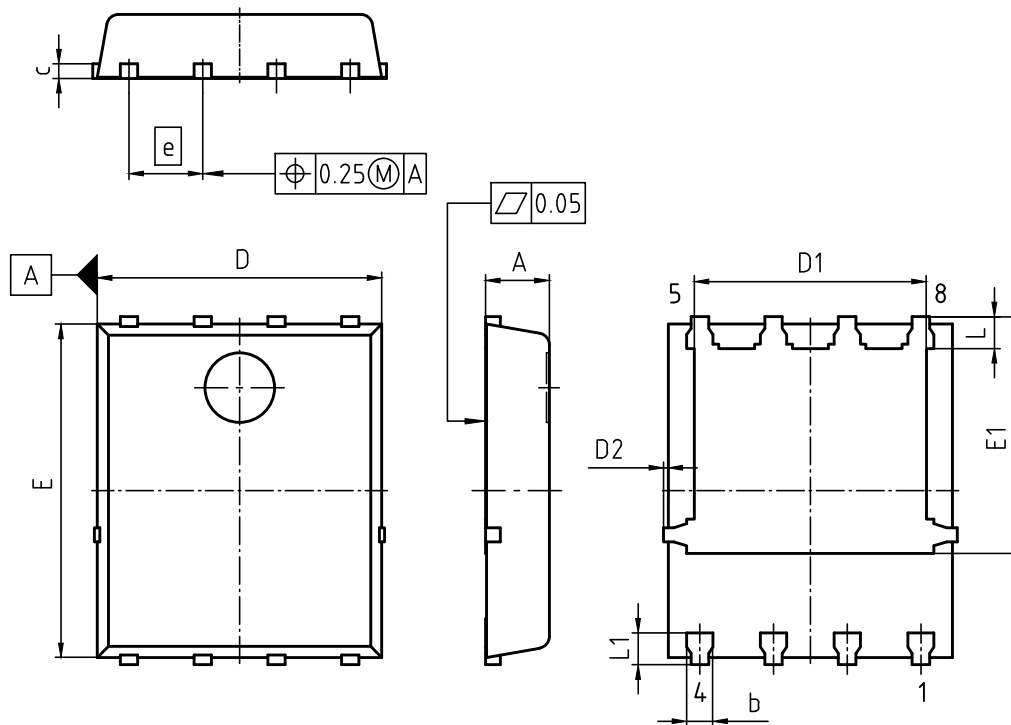








5 Package Outlines



PACKAGE - GROUP NUMBER:		PG-TDSON-8-U08	
REVISION: 01		DATE: 12.02.2021	
DIMENSIONS	MILLIMETERS		
	MIN.	MAX.	
A	0.90	1.20	
b	0.34	0.54	
c	0.15	0.35	
D	4.80	5.35	
D1	3.90	4.40	
D2	0.00	0.22	
E	5.70	6.10	
E1	4.05	4.25	
e	1.27		
L	0.45	0.65	
L1	0.45	0.65	

- 1) EXCLUDING MOLD FLASH
- 2) REMOVAL ON MOLD GATE INTRUSION 0.1 MM PROTRUSION 0.1 MM
- 3) ALL METAL SURFACES ARE PLATED, EXCEPT AREA OF CUT

Figure 1 Outline PG-TDSON-8, dimensions in mm

Revision History

ISC0805NLS

Revision: 2022-01-31, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-03-15	Release of final version
2.1	2021-04-01	Update of features list
2.2	2022-01-31	Update avalanche energy and footnotes

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