

# TLE42764

Low Dropout Linear Voltage Regulator

TLE42764GV50  
TLE42764DV50  
TLE42764EV50  
TLE42764GV  
TLE42764DV

## Data Sheet

Rev. 1.3, 2013-07-30

# Automotive Power



## 1 Overview

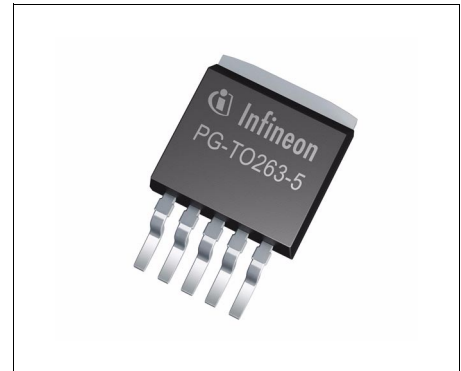
### Features

- Very Low Current Consumption
- Adjustable and 5 V Fixed Output Voltage  $\pm 2\%$
- Output Current up to 400 mA
- Enable Input
- Very Low Dropout Voltage
- Output Current Limitation
- Overtemperature Shutdown
- Reverse Polarity Protection
- Wide Temperature Range From  $-40\text{ }^{\circ}\text{C}$  up to  $150\text{ }^{\circ}\text{C}$
- Green Product (RoHS compliant)
- AEC Qualified

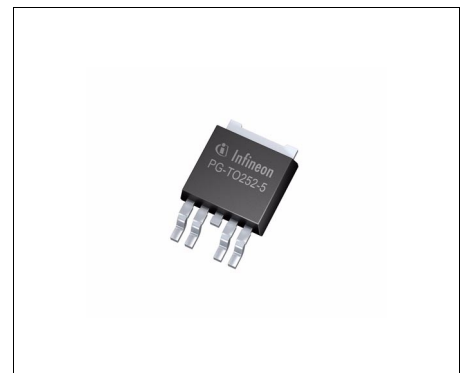
### Description

The TLE42764 is a monolithic integrated low dropout voltage regulator for load currents up to 400 mA. An input voltage up to 40 V is regulated to an adjustable or 5 V fixed voltage with a precision of  $\pm 2\%$ . The device is designed for the harsh environment of automotive applications. Therefore it is protected against overload, short circuit and overtemperature conditions by the implemented output current limitation and the overtemperature shutdown circuit. The TLE42764 can be also used in all other applications requiring a stabilized voltage between 2.5 V and 20 V.

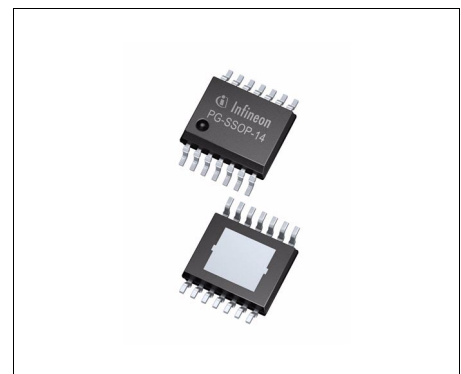
Due to its very low quiescent current the TLE42764 is dedicated for use in applications permanently connected to  $V_{\text{BAT}}$ . In addition the device can be switched off via the Enable input reducing the current consumption to less than  $10\text{ }\mu\text{A}$ .



PG-TO263-5



PG-TO252-5



PG-SSOP-14 exposed pad

| Type         | Package                | Marking |
|--------------|------------------------|---------|
| TLE42764GV50 | PG-TO263-5             | 42764V5 |
| TLE42764DV50 | PG-TO252-5             | 42764V5 |
| TLE42764GV   | PG-TO263-5             | 42764V  |
| TLE42764DV   | PG-TO252-5             | 42764V  |
| TLE42764EV50 | PG-SSOP-14 exposed pad | 42764V5 |

## 2 Block Diagram

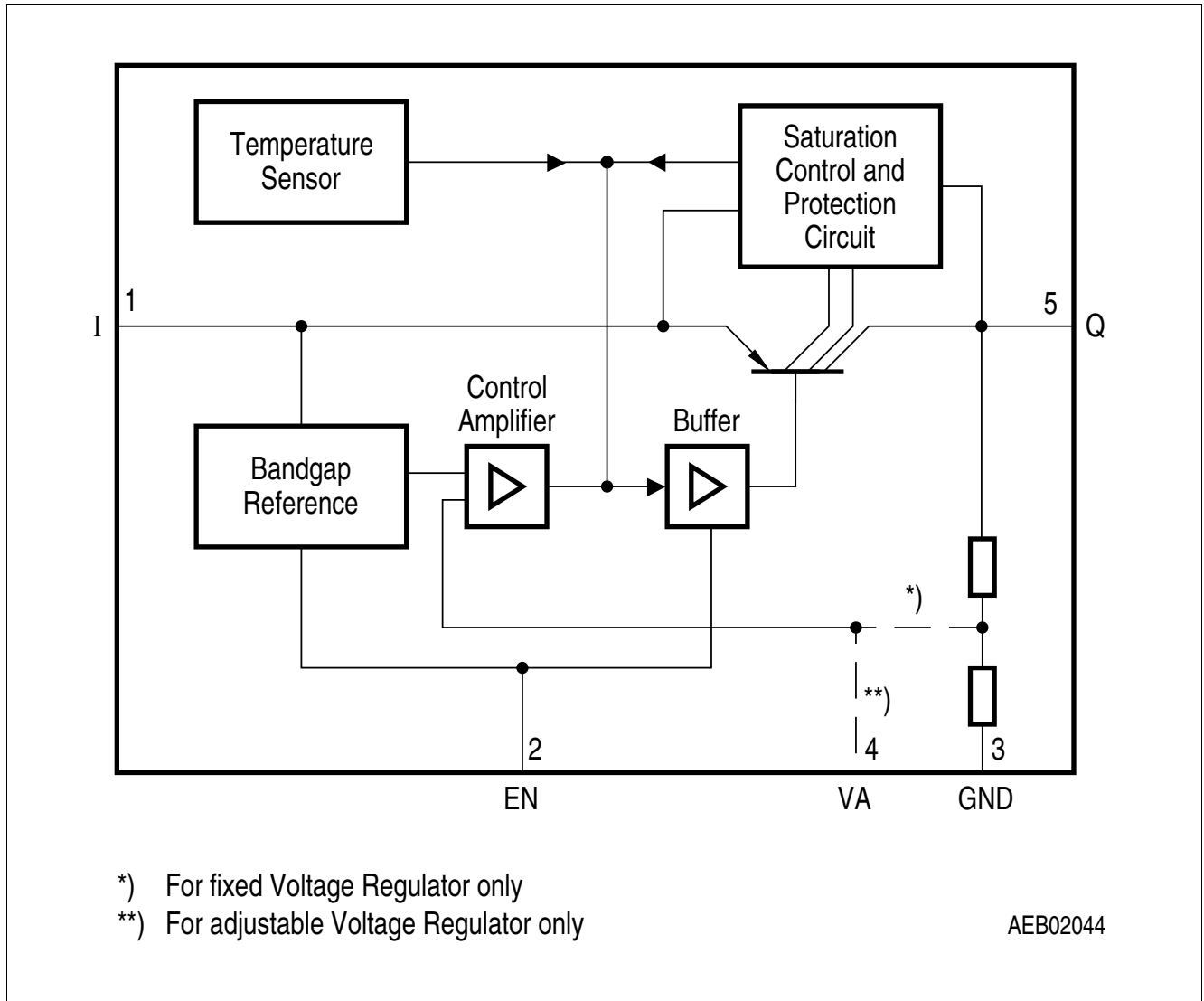


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment PG-TO263-5, PG-TO252-5

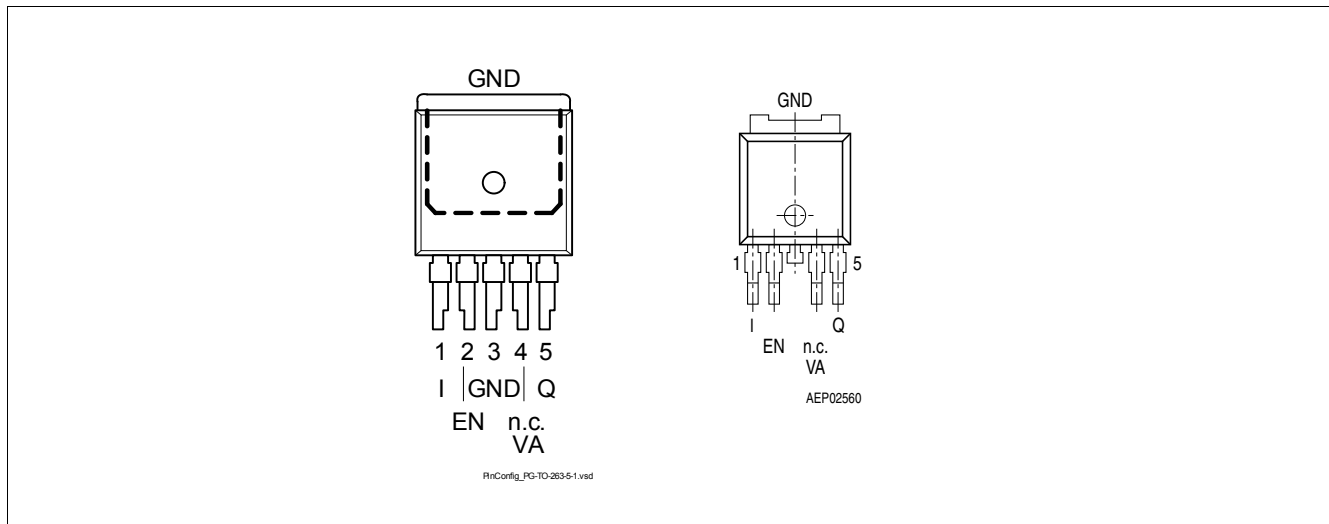


Figure 2 Pin Configuration (top view)

#### 3.2 Pin Definitions and Functions PG-TO263-5, PG-TO252-5

| Pin No.   | Symbol     | Function   |
|-----------|------------|--|
| 1         | I          | <b>Input</b><br>block to ground directly at the IC with a ceramic capacitor  |
| 2         | EN         | <b>Enable Input</b><br>high level input signal enables the IC;<br>low level input signal disables the IC;<br>integrated pull-down resistor   |
| 3         | GND        | <b>Ground</b><br>internally connected to heat slug   |
| 4         | n.c.<br>VA | <b>not connected</b> for TLE42764GV50, TLE42764DV50<br>can be open or connected to GND<br><b>Voltage Adjust Input</b> for TLE42764GV, TLE42764DV<br>connect external voltage divider to configure the output voltage |
| 5         | Q          | <b>Output</b><br>block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in <b>“Functional Range” on Page 7</b>  |
| Heat Slug | –          | <b>Heat Slug</b><br>internally connected to GND;<br>connect to GND and heatsink area   |

### 3.3 Pin Assignment PG-SSOP-14 exposed pad

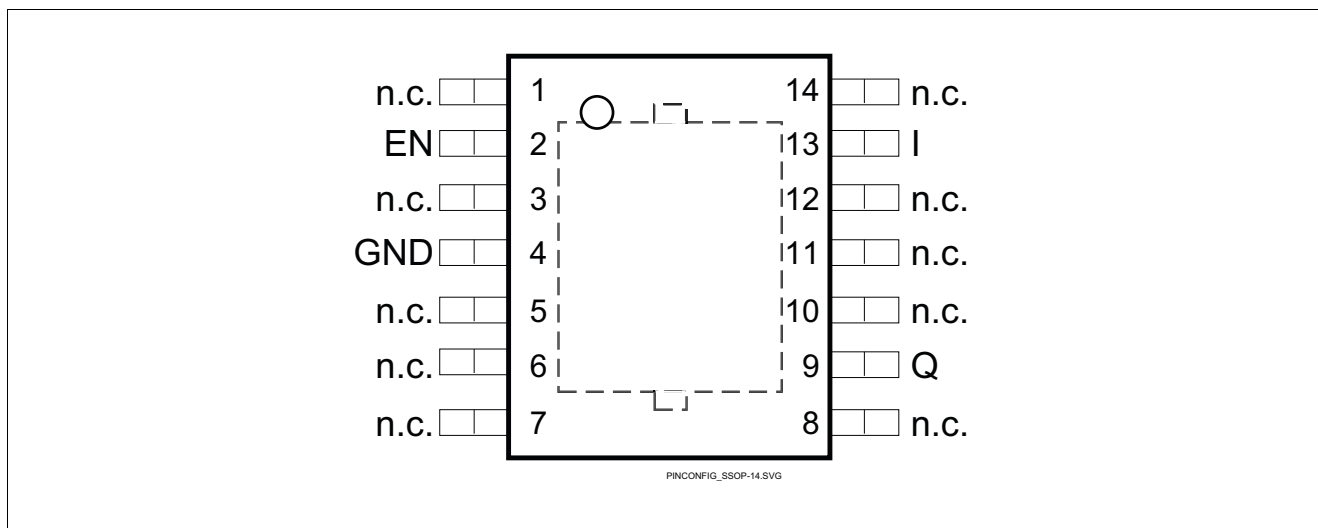


Figure 3 Pin Configuration (top view)

### 3.4 Pin Definitions and Functions PG-SSOP-14 exposed pad

| Pin No.      | Symbol | Function  |
|--------------|--------|---|
| 1, 3, 5-7    | n.c.   | <b>non connected</b><br>can be open or connected to GND   |
| 2            | EN     | <b>Enable Input</b><br>high level input signal enables the IC;<br>low level input signal disables the IC;<br>integrated pull-down resistor                                  |
| 4            | GND    | <b>Ground</b>   |
| 8, 10-12, 14 | n.c.   | <b>non connected</b><br>can be open or connected to GND   |
| 9            | Q      | <b>Output</b><br>block to ground with a capacitor close to the IC terminals, respecting the values given for its capacitance and ESR in <b>“Functional Range” on Page 7</b> |
| 13           | I      | <b>Input</b><br>block to ground directly at the IC with a ceramic capacitor   |
| Exposed Pad  | –      | <b>Exposed Pad</b><br>connect to GND and heatsink area  |

## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

**Table 1 Absolute Maximum Ratings<sup>1)</sup>**
 $T_j = -40\text{ °C to }150\text{ °C}$ ; all voltages with respect to ground, (unless otherwise specified)

| Pos.                           | Parameter            | Symbol        | Limit Values |      | Unit | Test Condition                                      |
|--------------------------------|----------------------|---------------|--------------|------|------|---|
|                                |                      |               | Min.         | Max. |      |   |
| <b>Input I, Enable EN</b>      |                      |               |              |      |      |   |
| 4.1.1                          | Voltage              | $V_I$         | -42          | 45   | V    | –   |
| <b>Voltage Adjust Input VA</b> |                      |               |              |      |      |   |
| 4.1.2                          | Voltage              | $V_{VA}$      | -0.3         | 10   | V    | –   |
| <b>Output Q</b>                |                      |               |              |      |      |   |
| 4.1.3                          | Voltage              | $V_Q$         | -1           | 40   | V    | –   |
| <b>Temperature</b>             |                      |               |              |      |      |   |
| 4.1.4                          | Junction temperature | $T_j$         | -40          | 150  | °C   | –   |
| 4.1.5                          | Storage temperature  | $T_{stg}$     | -50          | 150  | °C   | –   |
| <b>ESD Susceptibility</b>      |                      |               |              |      |      |   |
| 4.1.6                          | ESD Absorption       | $V_{ESD,HBM}$ | -3           | 3    | kV   | Human Body Model (HBM) <sup>2)</sup>                |
| 4.1.7                          |                      | $V_{ESD,CDM}$ | -1000        | 1000 | V    | Charge Device Model (CDM) <sup>3)</sup> at all pins |

1) not subject to production test, specified by design

2) ESD susceptibility Human Body Model “HBM” according to AEC-Q100-002 - JESD22-A114

3) ESD susceptibility Charged Device Model “CDM” according to ESDA STM5.3.1

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

## 4.2 Functional Range

**Table 2 Functional Range**

| Pos.  | Parameter                  | Symbol     | Limit Values |      | Unit               | Remarks  |
|-------|----------------------------|------------|--------------|------|--------------------|--|
|       |                            |            | Min.         | Max. |                    |  |
| 4.2.1 | Input voltage              | $V_I$      | 5.5          | 40   | V                  | TLE42764GV50,<br>TLE42764DV50,<br>TLE42764EV50   |
| 4.2.2 | Input voltage              | $V_I$      | $V_Q + 0.5$  | 40   | V                  | TLE42764GV,<br>TLE42764DV;<br>$V_Q > 4\text{ V}$ |
| 4.2.3 | Input voltage              | $V_I$      | 4.5          | 40   | V                  | TLE42764GV,<br>TLE42764DV;<br>$V_Q < 4\text{ V}$ |
| 4.2.4 | Output Capacitor's         | $C_Q$      | 22           | –    | $\mu\text{F}$      | <sup>1)</sup>                                    |
| 4.2.5 | Requirements for Stability | $ESR(C_Q)$ | –            | 3    | $\Omega$           | <sup>2)</sup>                                    |
| 4.2.6 | Junction temperature       | $T_j$      | -40          | 150  | $^{\circ}\text{C}$ | –  |

1) The minimum output capacitance requirement is applicable for a worst case capacitance tolerance of 30%

2) Relevant ESR value at  $f = 10\text{ kHz}$

*Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.*



### 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

**Table 3 Thermal Resistance**

| Pos.   | Parameter                         | Symbol     | Limit Values |      |      | Unit | Conditions   |
|--|-----------------------------------|------------|--------------|------|------|------|--|
|  |                                   |            | Min.         | Typ. | Max. |      |  |
| <b>TLE42764GV, TLE42764GV50 (PG-TO263-5)</b> |                                   |            |              |      |      |      |  |
| 4.3.1  | Junction to Case <sup>1)</sup>    | $R_{thJC}$ | –            | 3.6  | –    | K/W  | measured to heat slug                                  |
| 4.3.2  | Junction to Ambient <sup>1)</sup> | $R_{thJA}$ | –            | 22   | –    | K/W  | <sup>2)</sup>  |
| 4.3.3  |                                   |            | –            | 74   | –    | K/W  | footprint only <sup>3)</sup>                           |
| 4.3.4  |                                   |            | –            | 42   | –    | K/W  | 300 mm <sup>2</sup> heatsink area <sup>3)</sup>        |
| 4.3.5  |                                   |            | –            | 34   | –    | K/W  | 600 mm <sup>2</sup> heatsink area <sup>3)</sup>        |
| <b>TLE42764DV, TLE42764DV50 (PG-TO252-5)</b> |                                   |            |              |      |      |      |  |
| 4.3.6  | Junction to Case <sup>1)</sup>    | $R_{thJC}$ | –            | 3.6  | –    | K/W  | measured to heat slug                                  |
| 4.3.7  | Junction to Ambient <sup>1)</sup> | $R_{thJA}$ | –            | 27   | –    | K/W  | <sup>2)</sup>  |
| 4.3.8  |                                   |            | –            | 115  | –    | K/W  | footprint only <sup>3)</sup>                           |
| 4.3.9  |                                   |            | –            | 52   | –    | K/W  | 300 mm <sup>2</sup> heatsink area <sup>3)</sup>        |
| 4.3.10                                       |                                   |            | –            | 40   | –    | K/W  | 600 mm <sup>2</sup> heatsink area <sup>3)</sup>        |
| <b>TLE42764EV50 (PG-SSOP-14 exposed pad)</b> |                                   |            |              |      |      |      |  |
| 4.3.11                                       | Junction to Case <sup>1)</sup>    | $R_{thJC}$ | –            | 7    | –    | K/W  | –  |
| 4.3.12                                       | Junction to Ambient <sup>1)</sup> | $R_{thJA}$ | –            | 41   | –    | K/W  | <sup>2)</sup>  |
| 4.3.13                                       |                                   |            | –            | 130  | –    | K/W  | footprint only <sup>3)</sup>                           |
| 4.3.14                                       |                                   |            | –            | 60   | –    | K/W  | 300 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> |
| 4.3.15                                       |                                   |            | –            | 50   | –    | K/W  | 600 mm <sup>2</sup> heatsink area on PCB <sup>3)</sup> |

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

3) Specified  $R_{thJA}$  value is according to Jedec JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm<sup>3</sup> board with 1 copper layer (1 x 70µm Cu).



## 5 Electrical Characteristics

### 5.1 Electrical Characteristics Voltage Regulator

**Table 4** Electrical Characteristics

$V_I=13.5\text{ V}$ ;  $T_j = -40\text{ }^\circ\text{C}$  to  $150\text{ }^\circ\text{C}$ ; all voltages with respect to ground (unless otherwise specified)

| Pos.            | Parameter                                     | Symbol                   | Limit Values |      |      | Unit | Measuring Condition  |
|-----------------|---|--------------------------|--------------|------|------|------|--|
|                 |   |                          | Min.         | Typ. | Max. |      |  |
| <b>Output Q</b> |   |                          |              |      |      |      |  |
| 5.1.1           | Output Voltage                                | $V_Q$                    | 4.9          | 5.0  | 5.1  | V    | TLE42764GV50,<br>TLE42764DV50,<br>TLE42764EV50<br>$5\text{ mA} < I_Q < 400\text{ mA}$<br>$6\text{ V} < V_I < 28\text{ V}$  |
| 5.1.2           | Output Voltage                                | $V_Q$                    | 4.9          | 5.0  | 5.1  | V    | TLE42764GV50,<br>TLE42764DV50,<br>TLE42764EV50<br>$5\text{ mA} < I_Q < 200\text{ mA}$<br>$6\text{ V} < V_I < 40\text{ V}$  |
| 5.1.3           | Output Voltage <sup>1)</sup>                  | $\Delta V_Q$             | -2           | –    | 2    | %    | TLE42764GV,<br>TLE42764DV;<br>$R_2 < 50\text{ k}\Omega$ ;<br>$V_Q + 1\text{ V} < V_I < 28\text{ V}$ ;<br>$V_I > 4.5\text{ V}$ ;<br>$5\text{ mA} \leq I_Q \leq 400\text{ mA}$ |
|                 |   | $\Delta V_Q$             | -2           | –    | 2    | %    | TLE42764GV,<br>TLE42764DV;<br>$R_2 < 50\text{ k}\Omega$ ;<br>$V_Q + 1\text{ V} < V_I < 40\text{ V}$ ;<br>$V_I > 4.5\text{ V}$ ;<br>$5\text{ mA} \leq I_Q \leq 200\text{ mA}$ |
| 5.1.4           | Output Voltage Adjustable Range <sup>3)</sup> | $V_{Q,\text{range}}$     | 2.5          | –    | 20   | V    | TLE42764GV,<br>TLE42764DV;<br>see <a href="#">Page 14</a>  |
| 5.1.5           | Dropout Voltage                               | $V_{\text{dr}}$          | –            | 250  | 500  | mV   | TLE42764GV50,<br>TLE42764DV50,<br>TLE42764EV50;<br>$I_Q = 250\text{ mA}$<br>$V_{\text{dr}} = V_I - V_Q$ <sup>2)</sup>  |
| 5.1.6           | Dropout Voltage                               | $V_{\text{dr}}$          | –            | 250  | 500  | mV   | TLE42764GV,<br>TLE42764DV;<br>$I_Q = 250\text{ mA}$ ; $V_I > 4.5\text{ V}$ ;<br>$V_{\text{dr}} = V_I - V_Q$ <sup>2)</sup>  |
| 5.1.7           | Load Regulation                               | $\Delta V_{Q,\text{lo}}$ | –            | 5    | 35   | mV   | $I_Q = 5\text{ mA}$ to $400\text{ mA}$ ;<br>$V_I = 6\text{ V}$ TLE42764GV50,<br>TLE42764DV50,<br>TLE42764EV50;<br>$V_I = 4.5\text{ V}$ TLE42764GV,<br>TLE42764DV             |

**Table 4 Electrical Characteristics**

$V_I=13.5\text{ V}$ ;  $T_j = -40\text{ °C}$  to  $150\text{ °C}$ ; all voltages with respect to ground (unless otherwise specified)

| Pos.   | Parameter                                      | Symbol             | Limit Values |      |      | Unit | Measuring Condition   |
|--------|--|--------------------|--------------|------|------|------|---|
|        |  |                    | Min.         | Typ. | Max. |      |   |
| 5.1.8  | Line Regulation                                | $\Delta V_{Q, li}$ | –            | 15   | 25   | mV   | $V_I = 12\text{ V}$ to $32\text{ V}$<br>$I_Q = 5\text{ mA}$ |
| 5.1.9  | Output Current Limitation                      | $I_Q$              | 400          | 600  | 1100 | mA   | <sup>2)</sup>   |
| 5.1.10 | Power Supply Ripple Rejection <sup>3)</sup>    | $PSRR$             | –            | 54   | –    | dB   | $f_r = 100\text{ Hz}$ ; $V_r = 0.5\text{ Vpp}$              |
| 5.1.11 | Temperature Output Voltage Drift <sup>3)</sup> | $\frac{dV_Q}{dT}$  | –            | 0.5  | –    | mV/K | –   |

**Current Consumption**

|        |  |       |   |     |     |               |   |
|--------|--|-------|---|-----|-----|---------------|---|
| 5.1.12 | Current Consumption, Regulator Disabled  | $I_q$ | – | –   | 10  | $\mu\text{A}$ | $V_{EN} = 0\text{ V}$<br>$T_j \leq 100\text{ °C}$ |
| 5.1.13 | Quiescent Current<br>$I_q = I_I - I_Q$   | $I_q$ | – | 100 | 220 | $\mu\text{A}$ | $I_Q = 1\text{ mA}$ ; $V_{EN} = 5\text{ V}$       |
| 5.1.14 | Current Consumption<br>$I_q = I_I - I_Q$ | $I_q$ | – | 5   | 10  | mA            | $I_Q = 250\text{ mA}$ ; $V_{EN} = 5\text{ V}$     |
| 5.1.15 | Current Consumption<br>$I_q = I_I - I_Q$ | $I_q$ | – | 15  | 25  | mA            | $I_Q = 400\text{ mA}$ ; $V_{EN} = 5\text{ V}$     |

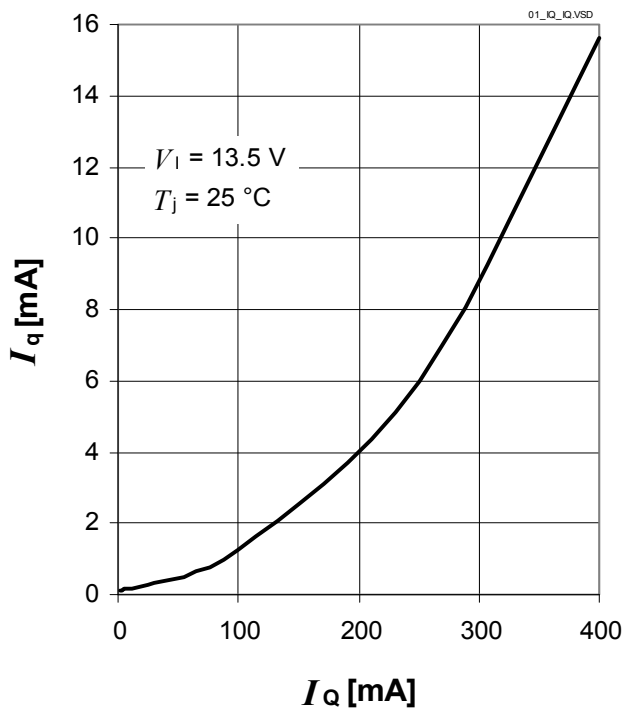
1) influence of resistor divider on precision neglected

2) Measured when the output voltage  $V_Q$  has dropped 100 mV from the nominal value obtained at  $V_I = 13.5\text{ V}$ .

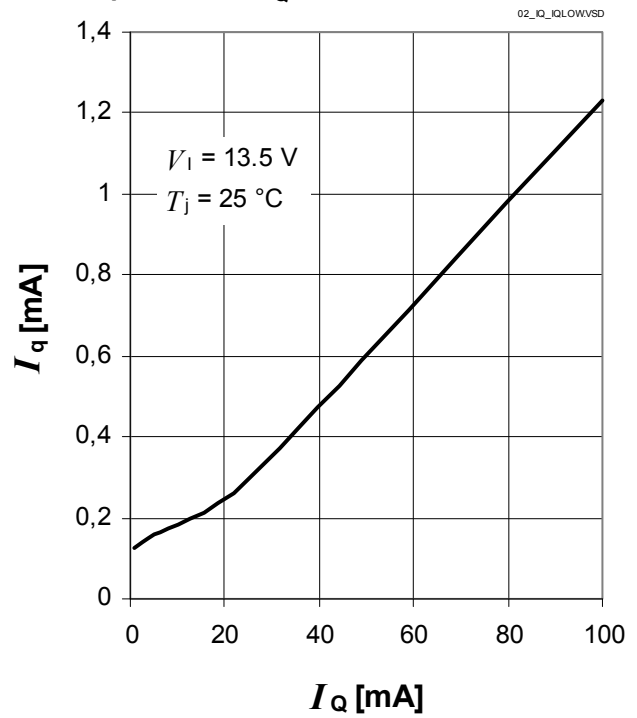
3) not subject to production test, specified by design

## 5.2 Typical Performance Characteristics Voltage Regulator

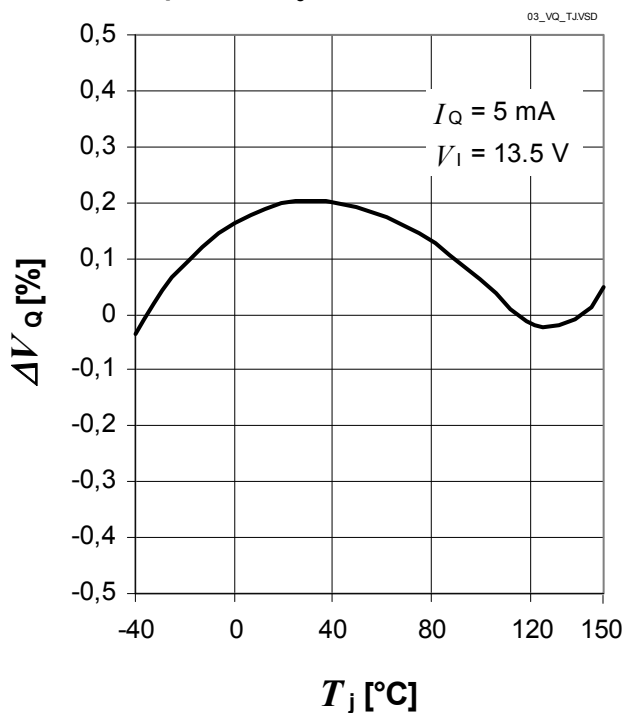
Current Consumption  $I_q$  versus Output Current  $I_Q$



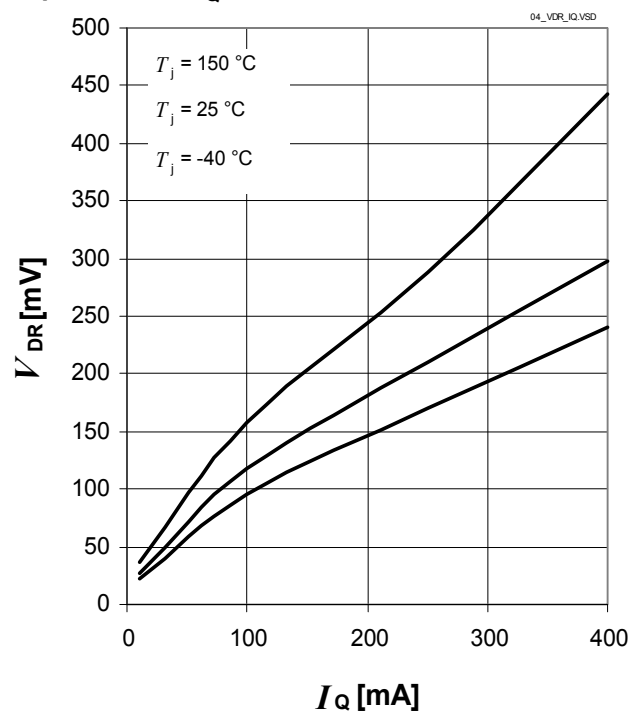
Current Consumption  $I_q$  versus Low Output Current  $I_Q$



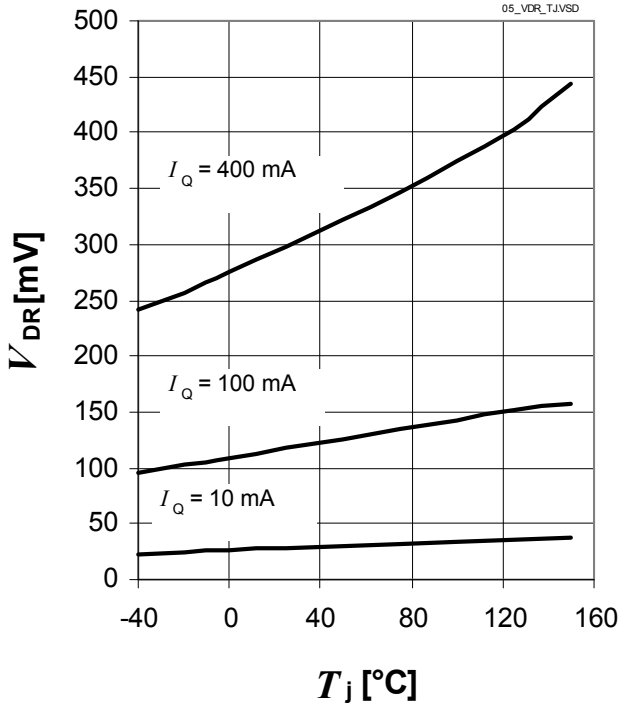
Output Voltage  $V_Q$  versus Junction Temperature  $T_j$



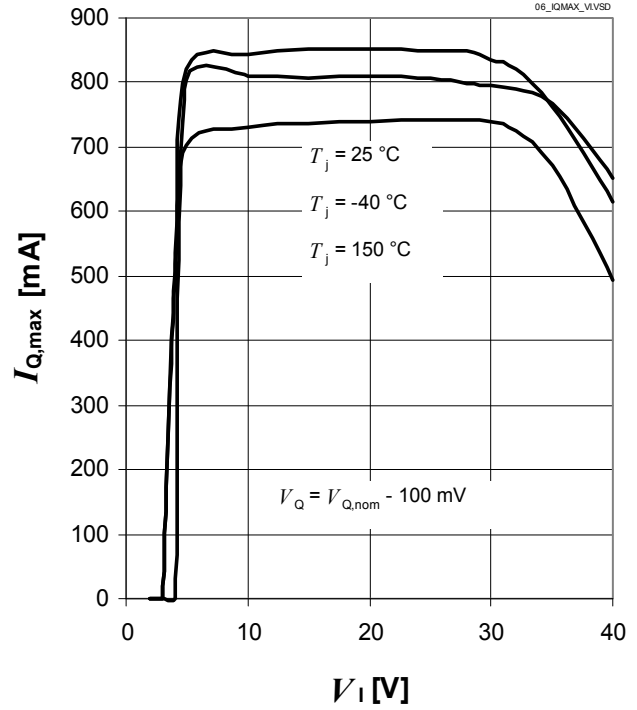
Dropout Voltage  $V_{dr}$  versus Output Current  $I_Q$



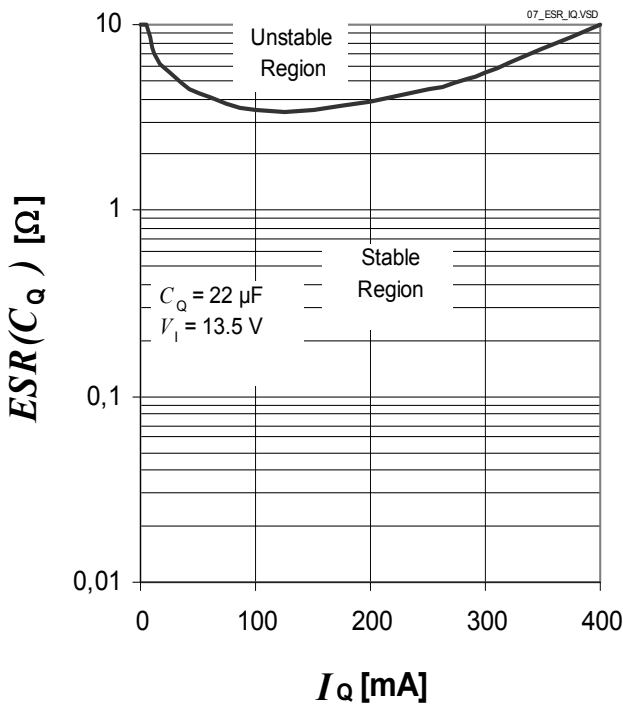
**Dropout Voltage  $V_{dr}$  versus Junction Temperature**



**Maximum Output Current  $I_Q$  versus Input Voltage  $V_I$**



**Region Of Stability: Output Capacitor's ESR  $ESR(C_Q)$  versus Output Current  $I_Q$**



### 5.3 Electrical Characteristics Enable Function

The Enable Function allows disabling/enabling the regulator via the input pin EN. The regulator is turned on in case the pin EN is connected to a voltage higher than  $V_{EN,H}$ . This can be e.g. the battery voltage, whereby no additional pull-up resistor is needed. The regulator can be turned off by connecting the pin EN to a voltage less than  $V_{EN,L}$ , e.g. GND.

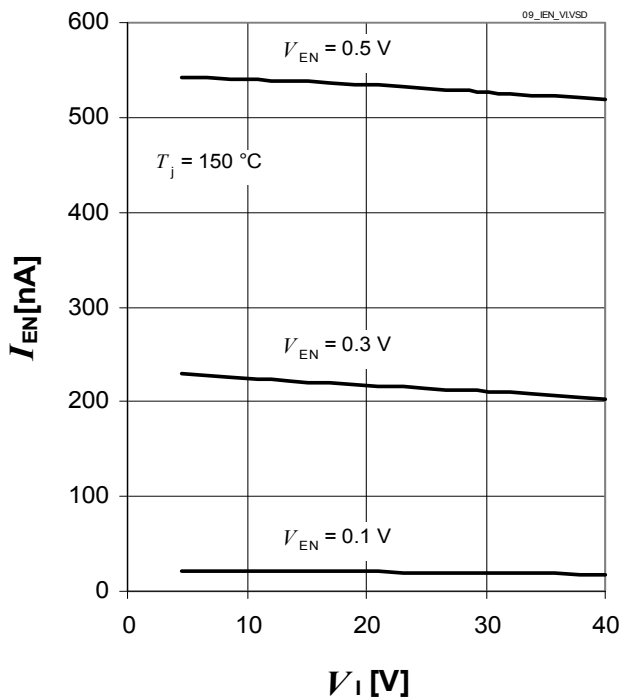
**Table 5 Electrical Characteristics Enable**

$V_I=13.5\text{ V}$ ;  $T_j = -40\text{ °C}$  to  $150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

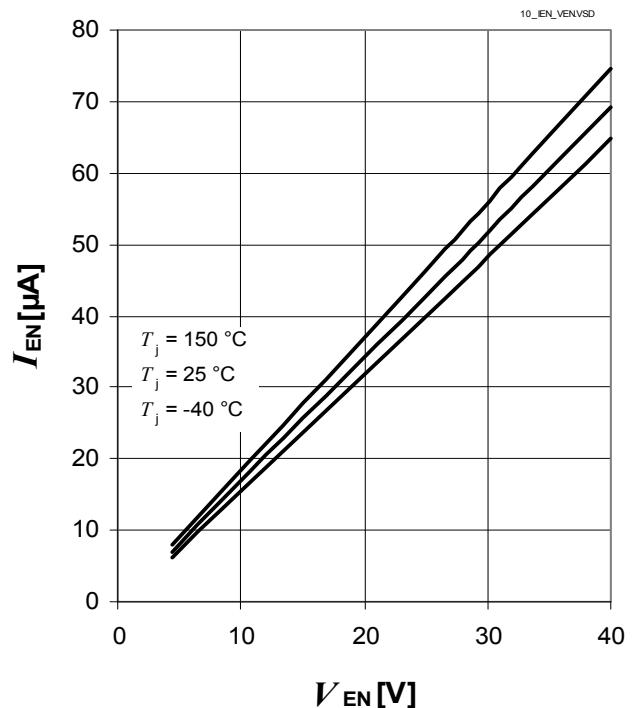
| Pos.   | Parameter                | Symbol     | Limit Values |      |      | Unit          | Measuring Condition     |
|--------|--------------------------|------------|--------------|------|------|---------------|-------------------------|
|        |                          |            | Min.         | Typ. | Max. |               |                         |
| 5.3.16 | High Level Input Voltage | $V_{EN,H}$ | 3.5          | –    | –    | V             | $V_Q \geq 4.9\text{ V}$ |
| 5.3.17 | Low Level Input Voltage  | $V_{EN,L}$ | –            | –    | 0.5  | V             | $V_Q \leq 0.1\text{ V}$ |
| 5.3.18 | High Level Input Current | $I_{EN,H}$ | 5            | 10   | 20   | $\mu\text{A}$ | $V_{EN} = 5\text{ V}$   |

### 5.4 Typical Performance Characteristics Enable Function

Enabled Input Current  $I_{EN}$  versus Input Voltage  $V_I$ , EN=Off



Enabled Input Current  $I_{EN}$  versus Enabled Input Voltage  $V_{EN}$



## 6 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

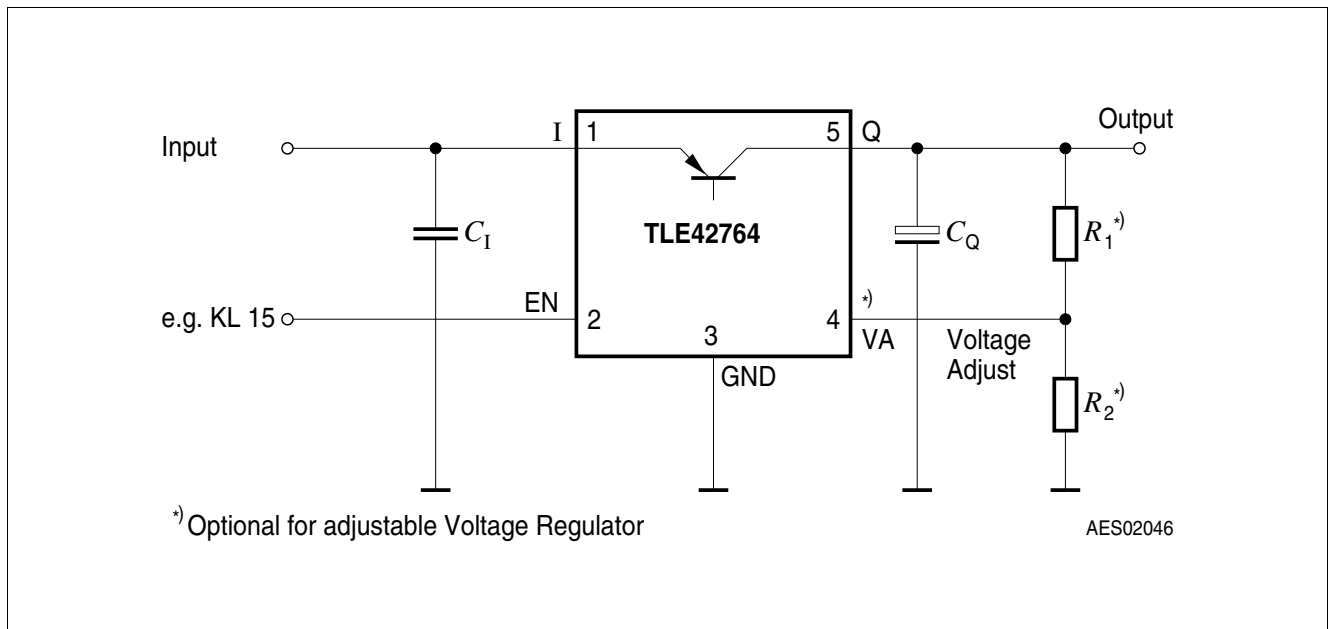


Figure 4 Application Diagram

A typical application circuit of the TLE42764 is shown in [Figure 4](#). It shows a generic configuration of the voltage regulator, with the recommendable minimum number of components one should use. Theoretically, if there is no risk of high frequency noise at all, even the small input filter capacitor can be omitted. For a normal operation mode of the device the only required device is the output capacitor, for the TLE42764GV and the TLE42764DV additionally the resistor divider. However, depending on the application's environment, additional components like an input buffer capacitor or a reverse polarity protection diode can be considered as well.

### Input Filter Capacitor

A small ceramic capacitor (e.g. 100nF in [Figure 4](#)) at the device's input helps filtering high frequency noise. To reach the best filter effect, this capacitor should be placed as close as possible to the device's input pin. The input filter capacitor does not have an influence on the stability of the device's regulation loop.

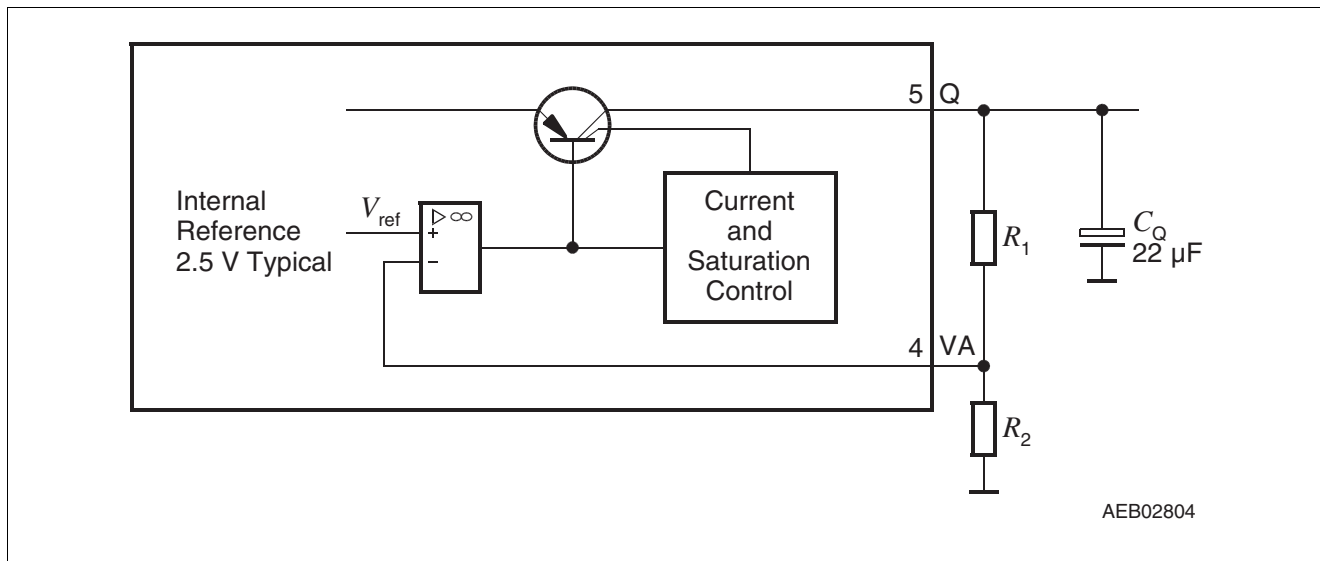
### Output Capacitor $C_Q$

The output capacitor is the only external component that is required in any case as it is a part of the device's regulating loop. To maintain stability of this loop, the TLE42764 requires an output capacitor respecting the values given in "[Functional Range](#)" on [Page 7](#).

### Adjusting the Output Voltage of Variable Output Regulators TLE42764GV, TLE42764DV

The output voltage of the TLE42764GV and the TLE42764DV can be adjusted between 2.5 V and 20 V by an external resistor divider, connected to the voltage adjust pin VA.

The pin VA is connected to the error amplifier comparing the voltage at this pin with the internal reference voltage of typically 2.5 V.



**Figure 5 External Components at Output for Variable Voltage Regulator**

The output voltage can be easily calculated, neglecting the current flowing into the VA pin:

$$V_Q = \frac{R_1 + R_2}{R_2} \times V_{ref}$$

where

$R_2 < 50 \text{ k}\Omega$  to neglect the current flowing into the VA pin,

with:

- $V_{ref}$ : internal reference voltage, typically 2.5V
- $R_1$ : resistor between regulator output Q and voltage adjust pin VA
- $R_2$ : resistor between voltage adjust pin VA and GND

For a 2.5 V output voltage the output pin Q has to be directly connected to the adjust pin VA.

Take into consideration, that the accuracy of the resistors  $R_1$  and  $R_2$  adds an additional error to the output voltage tolerance.



## 7 Package Outlines

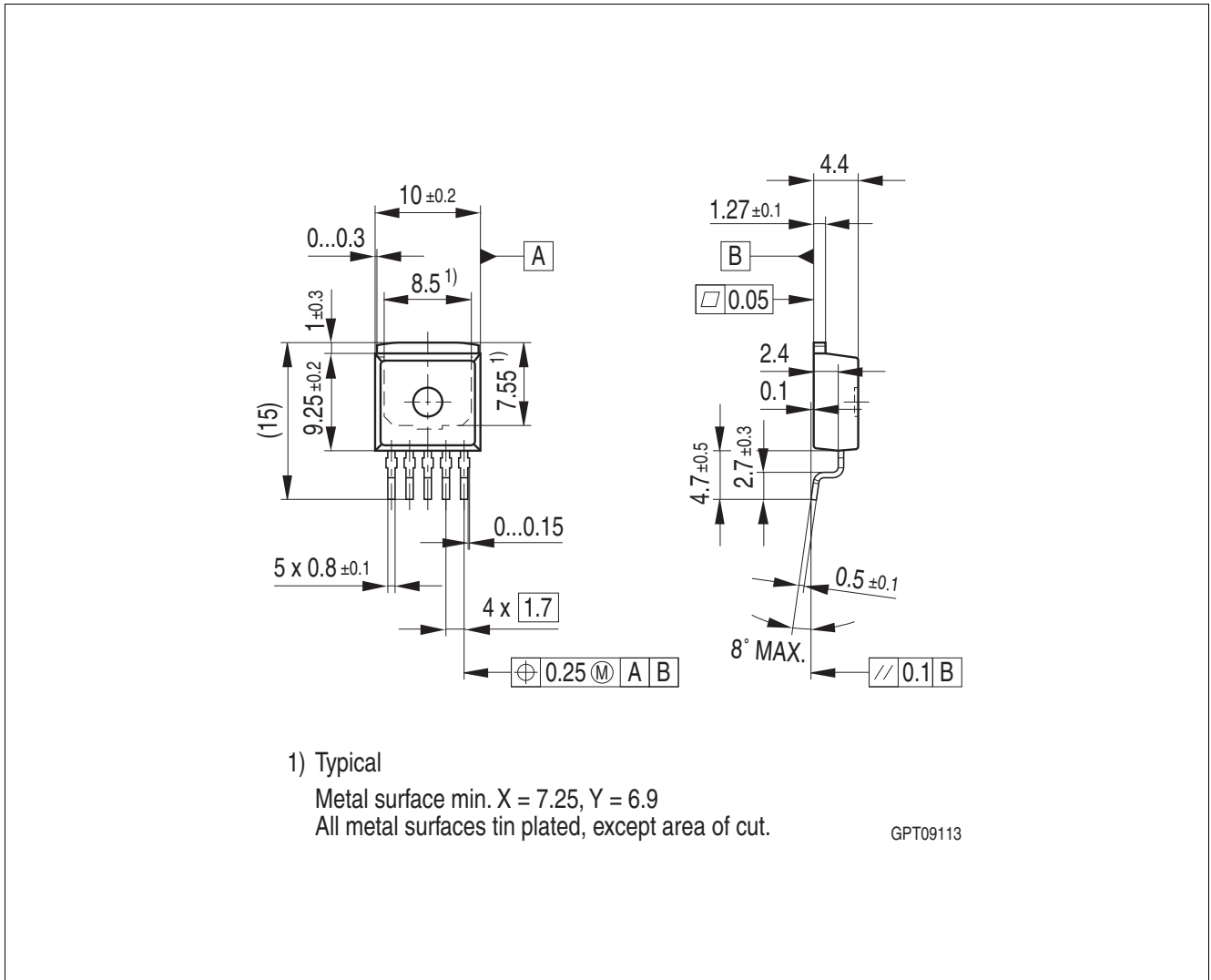


Figure 6 PG-TO263-5

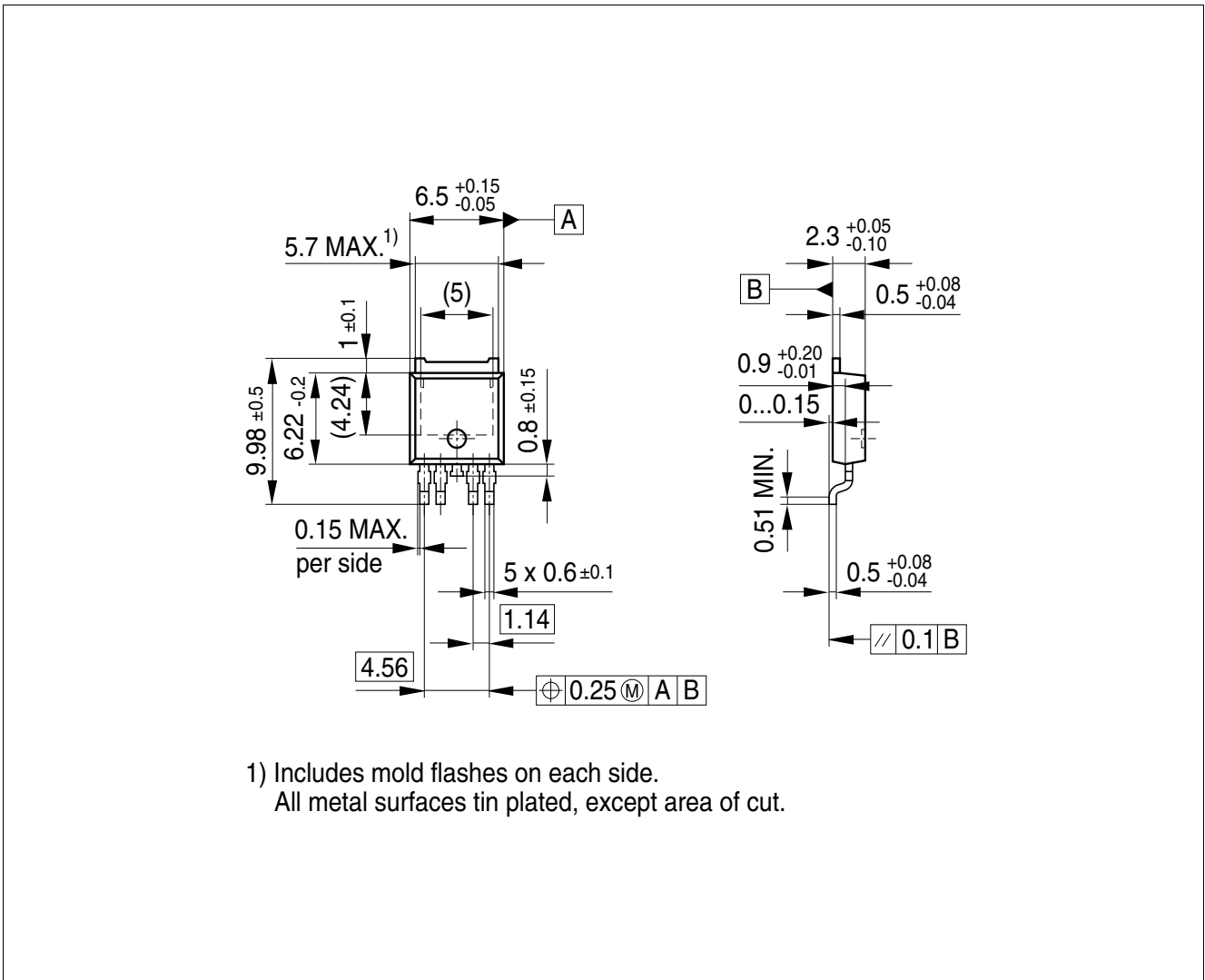


Figure 7 PG-TO252-5

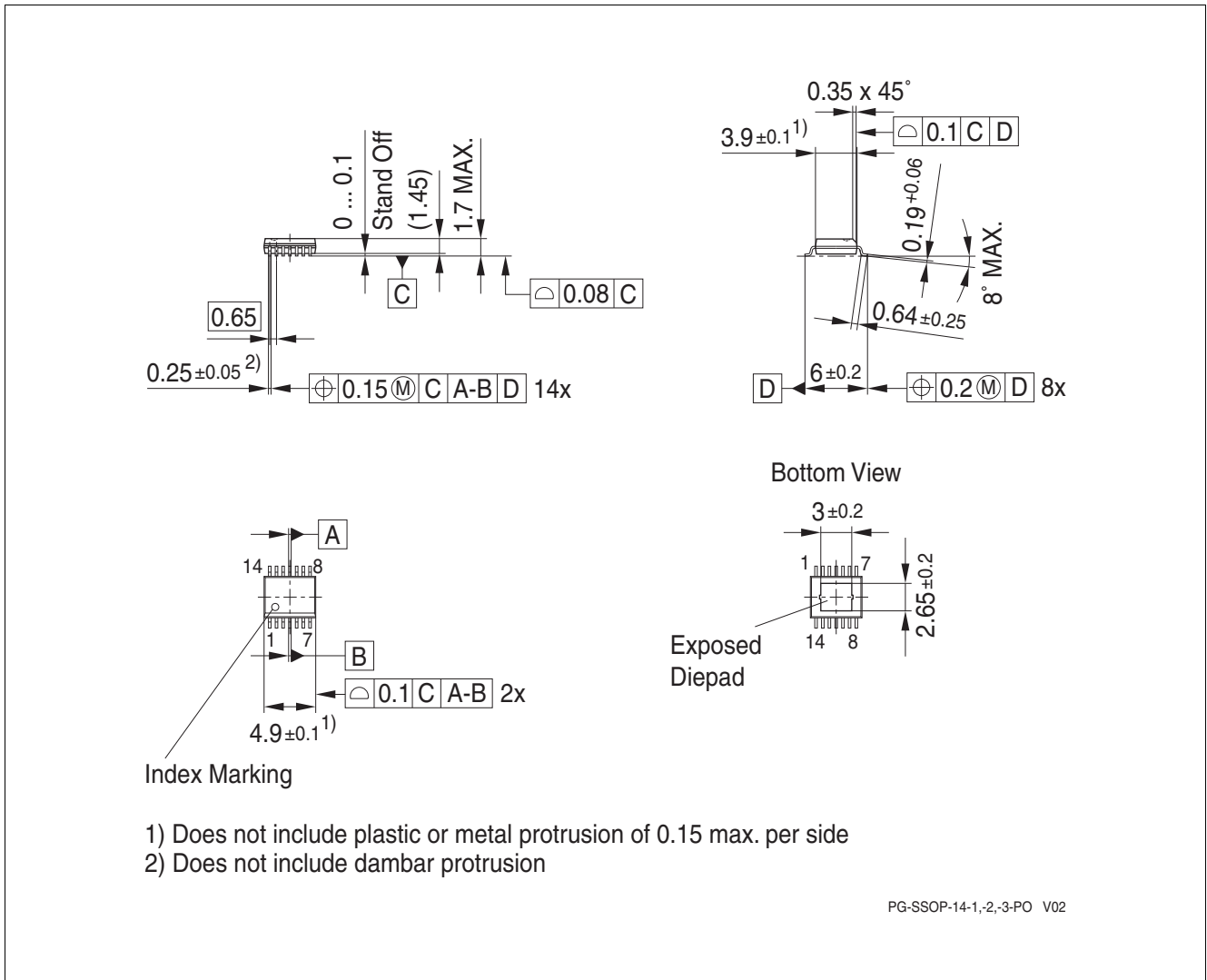


Figure 8 PG-SSOP-14 exposed pad

**Green Product (RoHS compliant)**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on alternative packages, please visit our website:  
<http://www.infineon.com/packages>.

Dimensions in mm

## 8 Revision History

| Revision | Date       | Changes  |
|----------|------------|--|
| 1.3      | 2013-07-30 | Split of the Accuracy Specification for the adjustable variants TLE42764GV and TLE42764DV ( <b>5.1.3</b> ) into two different conditions.<br>For high input voltages up to 40V and output current up to 200mA the accuracy is specified with +-2%.<br>For input voltages up to 28V, the output current is allowed to go up to 400mA to achieve an accuracy of +-2% according to the specification. |
| 1.2      | 2011-02-15 | Updated Version final Data Sheet: 5V Version TLE42764EV50 in PG-SSOP-14 exposed pad package and all related description added  |
| 1.1      | 2009-10-09 | Updated Version final Data Sheet: 5V Versions in PG-TO252-5 and PG-TO263-5 package and all related description added   |
|          |            | In <b>“Features” on Page 2</b> in text “and 5 V Fixed “added   |
|          |            | In <b>“Description” on Page 2</b> “or 5 V fixed “added   |
|          |            | In table on bottom of page <b>“Overview” on Page 2</b> 2 product versions including package and marking added  |
|          |            | In <b>“Functional Range” on Page 7 Item 4.2.1</b> added  |
|          |            | In <b>“Electrical Characteristics Voltage Regulator” on Page 9 Item 5.1.1, Item 5.1.2 and Item 5.1.5</b> added; In Conditions of <b>Item 5.1.7</b> “ $V_1 = 6\text{ V}$ TLE42764GV50, TLE42764DV50;” added   |
| 1.0      | 2008-01-14 | Initial Version final Data Sheet   |

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