XDPL8210 Digital Flyback Controller IC

XDP™ Digital Power

Datasheet
Revision 1.1

Features

- Single stage flyback controller with ***Power Factor Correction (PFC)***
- Primary side regulated ***Constant Current (CC)*** output with high precision
- Supports universal AC input (90 V_{rms} to 305 V_{rms})
- Supports wide LED load voltage range (up to 4 times of the minimum LED load voltage)
- Excellent line and load regulation (typical within +/- 2%)
- High power quality (Typical ***Power Factor (PF)*** up to 0.99 and ***Total Harmonic Distortion (THD)*** < 10%)
- High efficiency with ***Quasi-Resonant Mode, switching in first valley (QRM1)*** at high output power and frequency controlled ***Discontinuous Conduction Mode (DCM)*** at medium output power
- Dim-to-off operation (with typical standby power as low as 60 mW)
- Dedicated PWM input pin for dimming control by either a micro-controller or a transformer-less IEC60929-compliant isolated 0 - 10 V dimming circuit (based on CDM10VD)
- Dimming down to 1%
- ***Limited Power (LP)*** mode
- Input overvoltage and undervoltage (Brown-in/Brown-out) protection with configurable threshold for output on/off
- Brown-out maximum power reduction, to better protect primary components from overheating and saturation
- Adaptive output overvoltage protection to meet UL1310 standard (Class 2) for the 54 V LED driver design.
- Output and *VCC* undervoltage protection
- Configurable dimming parameters, e.g. dimming curve (linear/quadratic), minimum current, dim-to-off option (enabled/disabled)

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Potential applications

- Electronic control gear for LED luminaires

Potential applications

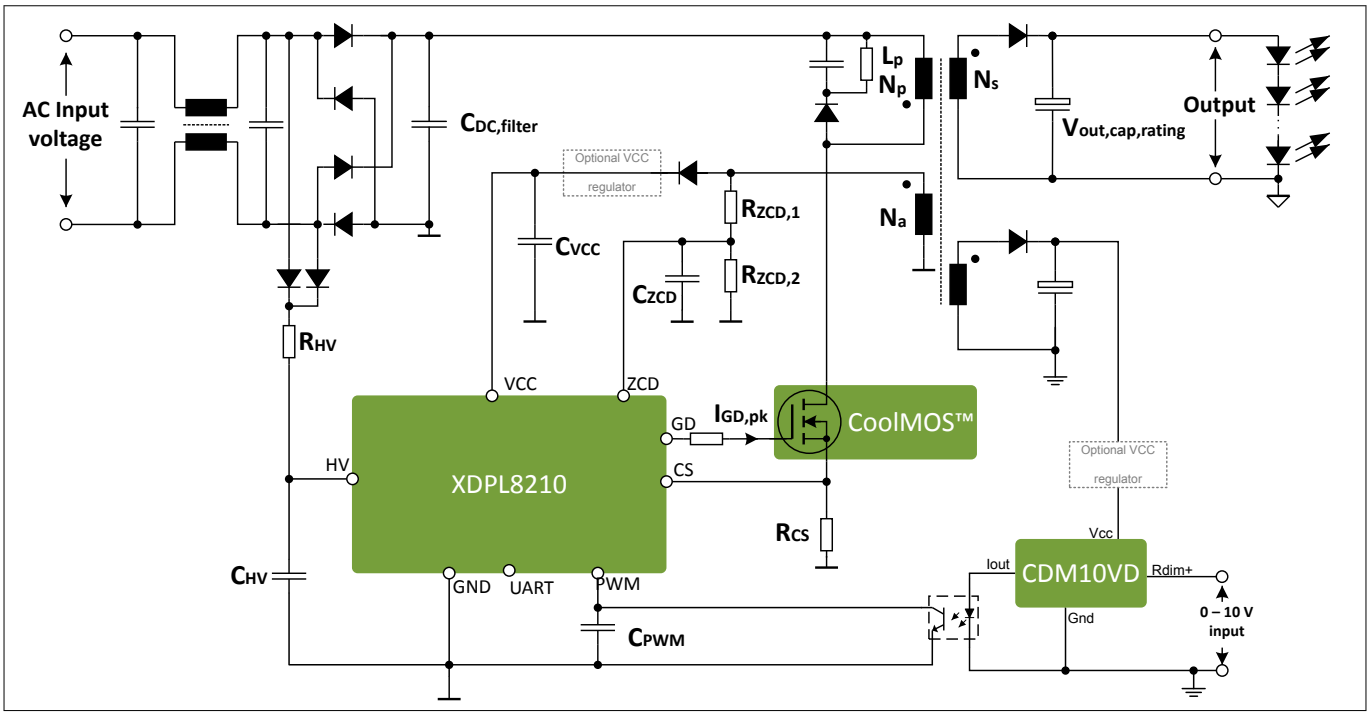

Figure 1 Potential application 1 for XDPL8210

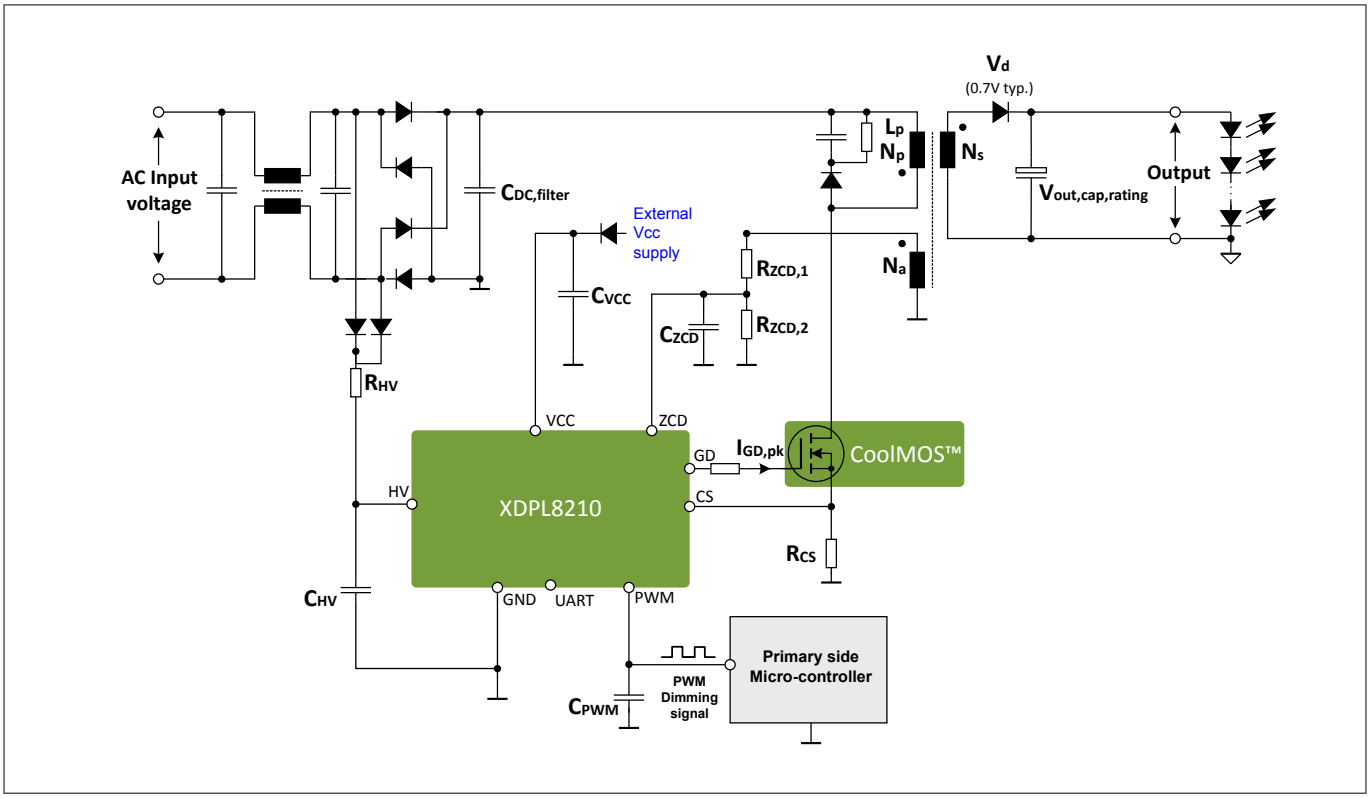

Figure 2 Potential application 2 for XDPL8210

Product type	Package	Marking	Firmware version	Ordering code
XDPL8210	PG-DSO-8	XDPL8210	4.2.0.0	SP001643692

Description

The XDPL8210 is a high performance configurable single-stage flyback controller with high power factor, primary side regulated constant current output and ***LP*** mode.

The primary side control saves external components especially an opto coupler, thus reducing cost and effort and increasing reliability. With its integrated functionality, XDPL8210 enables an increase set of features without external parts.

The digital core of the XDPL8210 and its advanced control algorithms provide multiple operation modes such as ***QRM1***, ***DCM*** or ***Active Burst Mode (ABM)***. In addition, XDPL8210 includes an enhanced ***PFC*** function which can partially compensate the effect of the input capacitance on power factor and harmonic distortion. With this functionality and smooth transition between the operation modes, the controller delivers high efficiency, high power factor and low harmonic distortion over wide load range. The active burst mode control scheme significantly extends the dimming range and is synchronized with the line frequency avoiding effects like flicker while reducing audible noise.

Operation parameters such as the output current, dimming curve and the protection features are digitally configurable. Infineon offers a user friendly ***Graphic User Interface*** for ***Personal Computer***s, allowing rapid engineering changes without the need for complex component design iterations. Functionality can be defined at the end of the production line. Multiple different ***Light Emitting Diode (LED)*** drivers can be built with the same hardware using different XDPL8210 parameter sets.

For instance, the dimming curve shape is configurable to linear or quadratic (eye-adaptive) and can optionally be inverted. Additionally, dim-to-off can be enabled or disabled.

Note: By default, the configurable parameters of a new XDPL8210 chip from Infineon are empty, so it is necessary to configure them before any application testing.

The system performance and efficiency can be optimized using Infineon *CoolMOS P7 power MOSFETs*.

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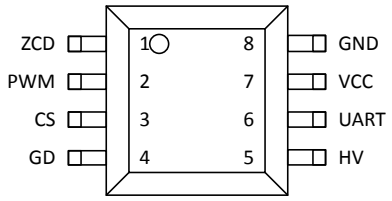
1 Pin configuration

Pin assignments and basic pin description information are shown below.



PG-DSO-8 (150mil)

Figure 3 Pinning of XDPL8210

Table 1 Pin definitions and functions

Name	Pin	Type	Function
ZCD	1	I	Zero-crossing detection: The *ZCD* pin is connected to the auxiliary winding via external resistors divider. It is used for zero-crossing detection, primary-side output voltage sensing and input voltage sensing.
PWM	2	I	***Pulse Width Modulation (PWM)*** dimming: The *PWM* pin is used as a dimming input. The PWM frequency should be fixed in the range from 500 Hz to 2 kHz.
CS	3	I	Current sensing: The *CS* pin is used for Flyback MOSFET current sensing via external shunt resistor.
GD	4	O	Gate driver: The *GD* pin is used for Flyback MOSFET gate drive control via external series resistor.
HV	5	I	High voltage: The *HV* pin is connected to the rectified input voltage via external series resistor. The *HV* pin is used to charge *VCC* pin voltage during startup and protection, via an internal 600 V startup cell. In addition, it is also used for line synchronization.
UART	6	I/O	***Universal Asynchronous Receiver Transmitter*** configuration: The *UART* pin is used as the digital interface for parameter configuration.
VCC	7	I	Operating voltage supply and sensing
GND	8	-	***Integrated Circuit (IC)*** grounding

2 Functional block diagram

The functional block diagram shows the basic data flow from input pins via signal processing to the output pins.

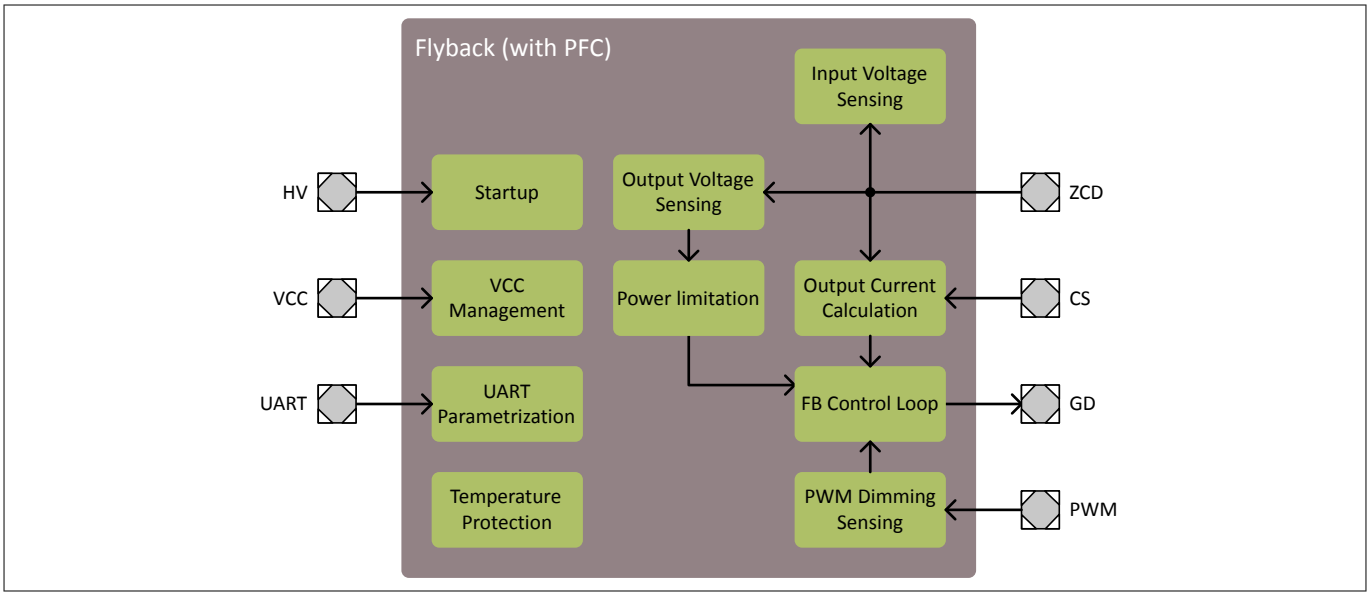


Figure 4 XDPL8210 functional block diagram

3 Functional description

The functional description provides an overview about the integrated functions and features as well as their relationship. The mentioned parameters and equations are based on typical values at T_A = 25°C. The corresponding min. and max. values are shown in the electrical characteristics.

3.1 Regulated mode

The XDPL8210 regulated mode provides a primary side control of the output current. The secondary side feedback components are not necessary for the output current control as the primary side regulation control loop is fully integrated.

3.1.1 Constant current and limited power set-point

Under non-dimming condition, the regulated mode ***CC*** output current set-point is based on the maximum output current set-point $I_{out,full}$. Under dimming condition, the regulated mode CC output current set-point is selected between $I_{out,full}$ and minimum output current set-point $I_{out,min}$, depending on the dimming level. Both $I_{out,min}$ and $I_{out,full}$ parameters are configurable.

If the output power produced by the regulated mode CC output current set-point and the connected LED voltage V_{LED} exceeds the configurable maximum output power limit set-point $P_{out,set}$, the regulated mode ***LP*** set point based on $P_{out,set}$ parameter would take over and reduce the output current set-point to $P_{out,set}$ / V_{LED}.

To achieve a full CC output dimming range between $I_{out,min}$ and $I_{out,full}$, the connected LED voltage V_{LED} should not exceed $P_{out,set}$ / $I_{out,full}$, as shown in ***Figure 5***.

If only the CC regulation is desired, the LP regulation can be disabled by configuring $P_{out,set}$ = 0.

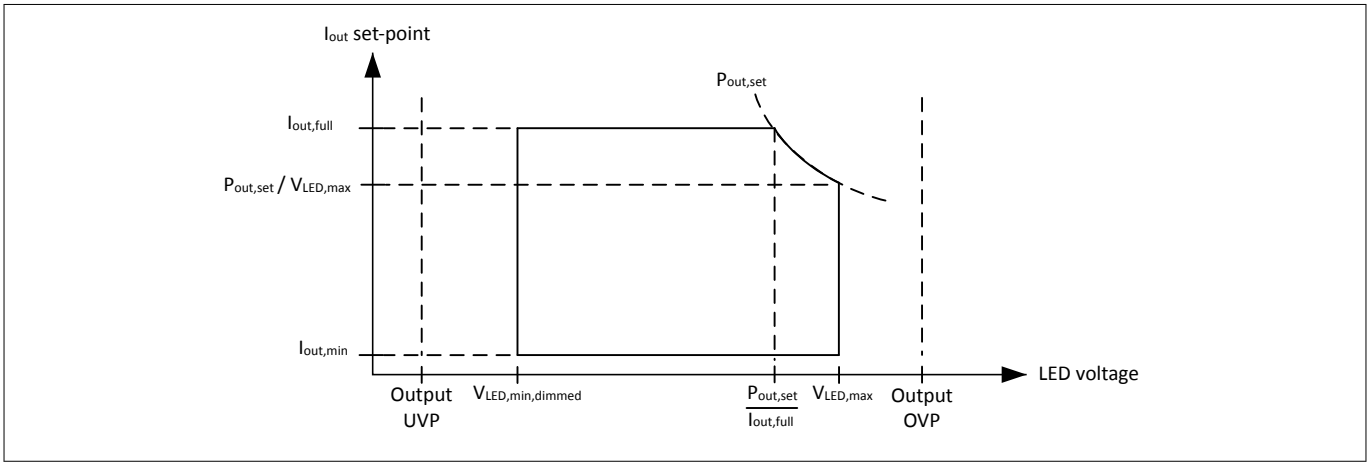


Figure 5 Operating window with constant current and limited power regulation

Note: $V_{LED,max}$ refers to the desired maximum operating LED voltage when output current is $I_{out,full}$. $V_{LED,max}$ should be designed well below the output overvoltage protection level.

Note: $V_{LED,min,dimmed}$ refers to the desired minimum operating LED voltage when output current is $I_{out,min}$. $V_{LED,min,dimmed}$ should be designed well above the output undervoltage protection level.

3.1.2 Multimode operation

In regulated mode, there are three different switching modes (***QRM1***, ***DCM*** and ***ABM***). The integrated primary side control loop selects the switching mode depending on the operating condition.

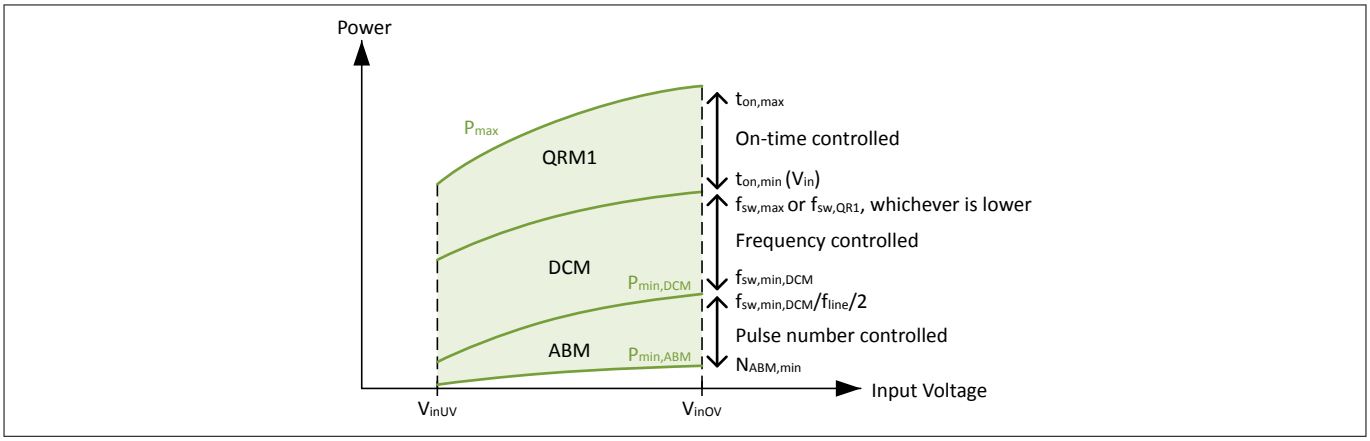


Figure 6 Multimode operation scheme

- QRM1: This mode minimizes the switching loss by switching on the MOSFET at the quasi-resonant 1st valley of the primary auxiliary winding voltage V_{AUX} signal, to maximize the efficiency. The power is controlled by regulating the on-time of the MOSFET.

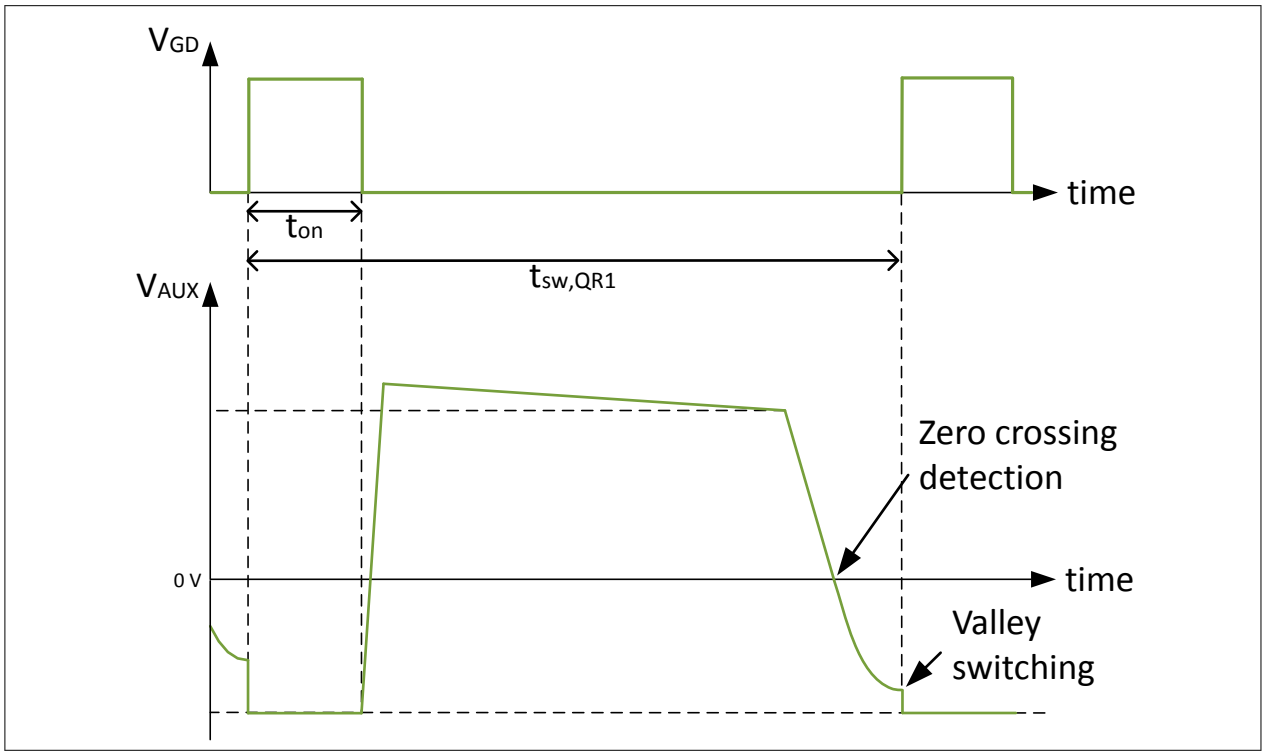


Figure 7 Switching waveforms in QRM1

Note: If the quasi-resonant 1st valley switching period $t_{sw,QR1}$ is lower than the minimum switching period of $1/f_{sw,max}$, the MOSFET can only be switched on after the quasi-resonant 1st valley.

- DCM: This mode minimizes the switching loss by reducing the switching frequency when the output power is reduced. The on-time is kept at the minimum value, while the power is controlled by regulating the switching frequency. The minimum power transfer in DCM $P_{min,DCM}$ happens when the minimum switching frequency $f_{sw,min}$ is reached.

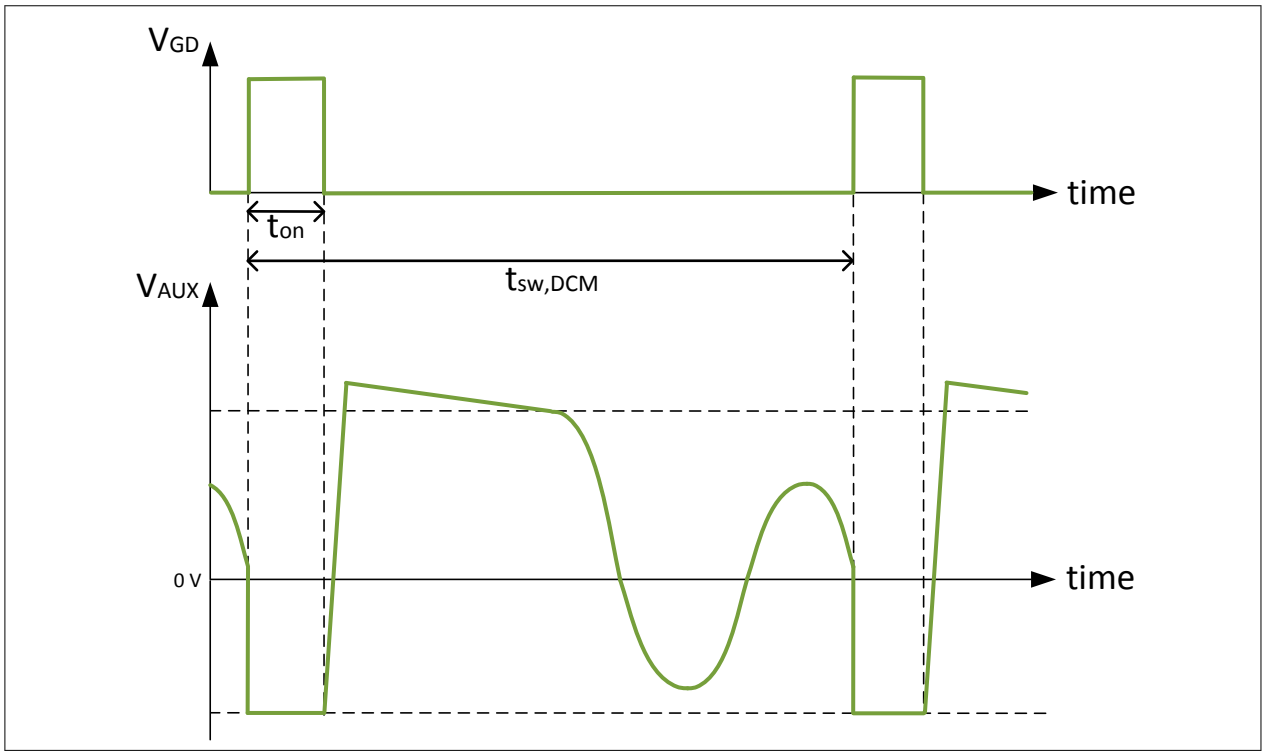


Figure 8 Switching waveforms in DCM

- ABM: This mode can be enabled with EN_{ABM} parameter to deliver a lower output power than in ***DCM***, for a lower minimum output current. The on-time and switching frequency are kept at the minimum value, while the power is controlled by regulating the switching pulse number of each burst period. The burst frequency in this mode is synchronized to the rectified AC input frequency, to ensure good light quality and low audible noise. The minimum power transfer in ***ABM*** $P_{min,ABM}$ happens when the minimum switching pulse number $N_{ABM,min}$ is reached.

Minimum on-time adaptation based on estimated input voltage

In all switching modes, $t_{on,min,V,out,sense}(V_{in})$ variable is scaled to allow a desired minimum transformer demagnetization time based on $t_{min,demag}$ parameter at the peak of input voltage $V_{in,peak}$, for output voltage sensing.

$$t_{\text{on, min, }V\text{, out, sense}}(V_{\text{in}}) = t_{\text{min, demag}} \cdot \frac{N_p}{N_s} \cdot \frac{V_{\text{out}}}{V_{\text{in, peak}}}$$

Equation 1

The minimum on-time of $t_{on,min}(V_{in})$ is based on $t_{on,min}$ parameter or $t_{on,min,V,out,sense}(V_{in})$ variable, whichever is higher.

$$t_{\text{on}} > t_{\text{on, min}}(V_{\text{in}}) = \max\left[t_{\text{on, min, }V\text{, out, sense}}(V_{\text{in}}),\ t_{\text{on, min}}\right]$$

Equation 2

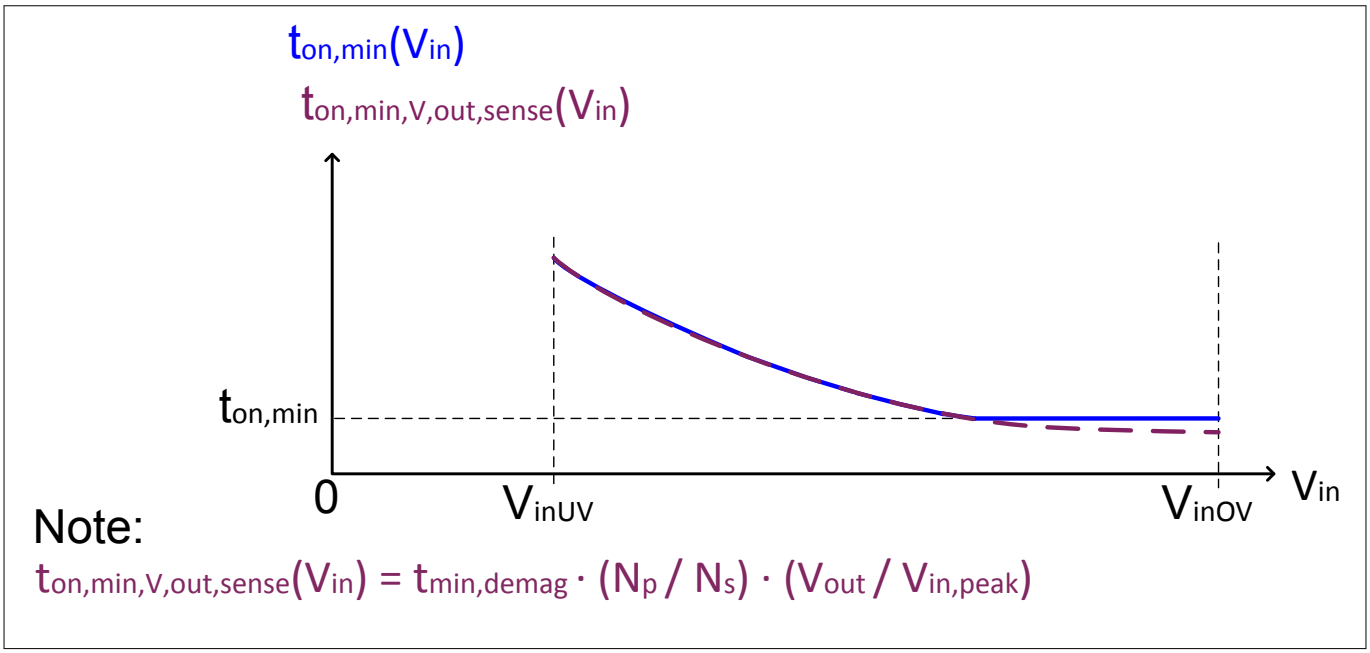


Figure 9 Minimum on-time depending on the estimated input voltage

3.1.3 Control loop initialization

When the regulated mode is entered initially after the startup phase, the control loop initialization is necessary. To ensure a fast and smooth startup with minimal output current overshoot, XDPL8210 features an adaptive control loop switching parameter initialization depending on the EN_{ABM} parameter and estimated input voltage V_{in}:

- If ***ABM*** is enabled with EN_{ABM} parameter, ABM is selected as the initial switching mode for the control loop. The initial controlled ABM switching pulse number $N_{ABM,init}$ is scaled between $N_{ABM,min}$ and $N_{ABM,init,VinUV}$ parameters, depending on V_{in}.
- If ABM is disabled with EN_{ABM} parameter, ***DCM*** is selected as the initial switching mode for the control loop. The initial controlled DCM switching frequency number $f_{DCM,init}$ is scaled between $f_{sw,min,DCM}$ parameter and $f_{DCM,init,VinUV}$ (20 kHz typ.), depending on V_{in}.

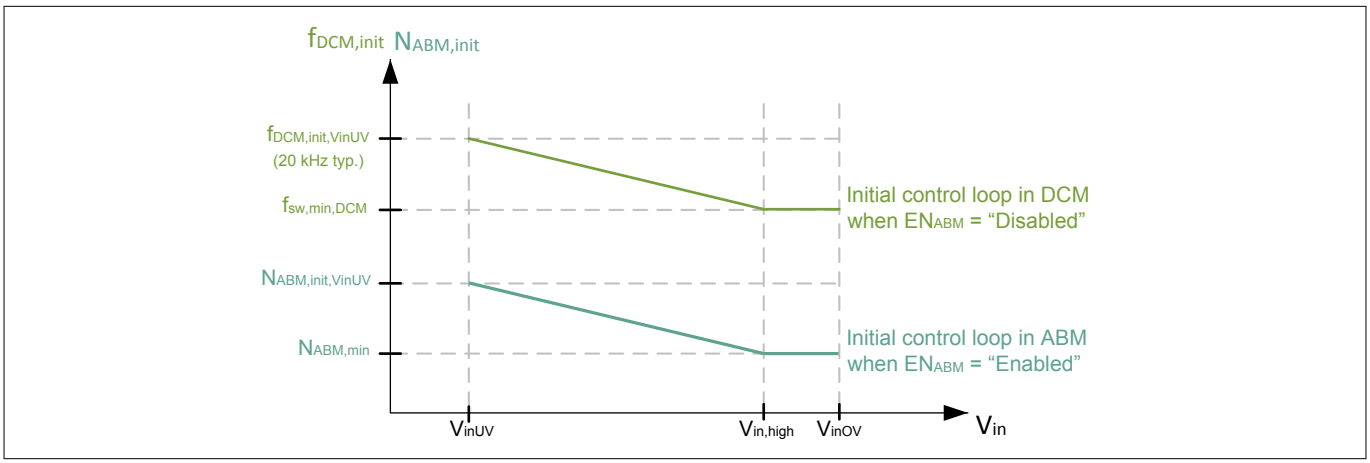


Figure 10 Adaptive control loop parameter initialization

Note: V_{inUV} and V_{inOV} refer to the input undervoltage protection level and input overvoltage level parameter respectively.

Note: *$V_{in,high}$ refers to the high input voltage parameter. If the estimated input voltage V_{in} is $V_{in,high}$ or more, $N_{ABM,init} = N_{ABM,min}$ or $f_{DCM,init} = f_{sw,min,DCM}$ is applied.*

3.2 Configurable gate voltage rising slope at GD pin

The gate drive peak voltage $V_{GD,pk}$ is 12 V with sufficient Vcc voltage supply. To achieve a good balance of switching loss and ***Electro-Magnetic Interference (EMI)***, the gate voltage rising slope which determines the MOSFET switching on speed can be controlled, by configuring the gate driver peak source current $I_{GD,pk}$ parameter (Configurable range: 30 mA to 118 mA). This saves two components (see $D_{fastoff}$, R_{slowon} in ***Figure 11***), which are conventionally added for the same purpose.

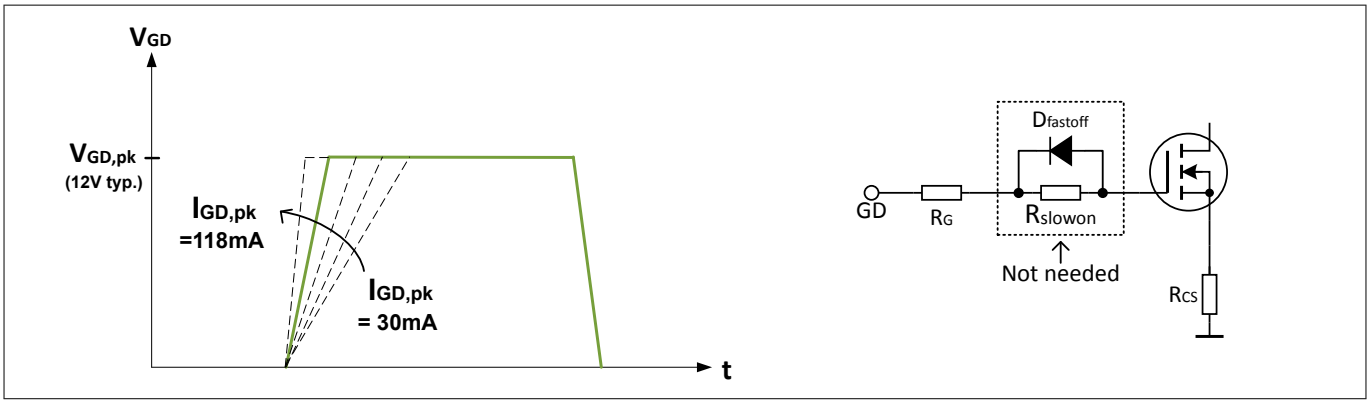


Figure 11 Configurable gate voltage rising slope and component saving

3.3 Startup

The startup phase is entered upon checking the startup conditions (e.g. input voltage, ***IC*** temperature) are within limits.

To estimate the input voltage level before startup, *ZCD* pin signal is measured during a single pulse generated on *GD* pin. This single pulse has an on-time based on the pre-start *CS* pin maximum voltage limit of $V_{OCP1,init}$ or 8 times of the leading edge blanking time $t_{CS,LEB}$ (e.g. 8 * 480 ns = 3.84 µs typ.). If the estimated input voltage or any other startup conditions are not within limits, startup phase is not entered and this single pulse will be generated again after an auto-restart duration.

The startup phase consists of soft start phase, output charging phase and ***PWM*** duty cycle measuring phase. The soft start phase is to minimize the component stress during startup. The output charging phase is to fast charge the output voltage for fast *VCC* voltage self supply takeover from the primary auxiliary winding, while the PWM duty cycle measuring phase is to determine the regulated mode output current set-point.

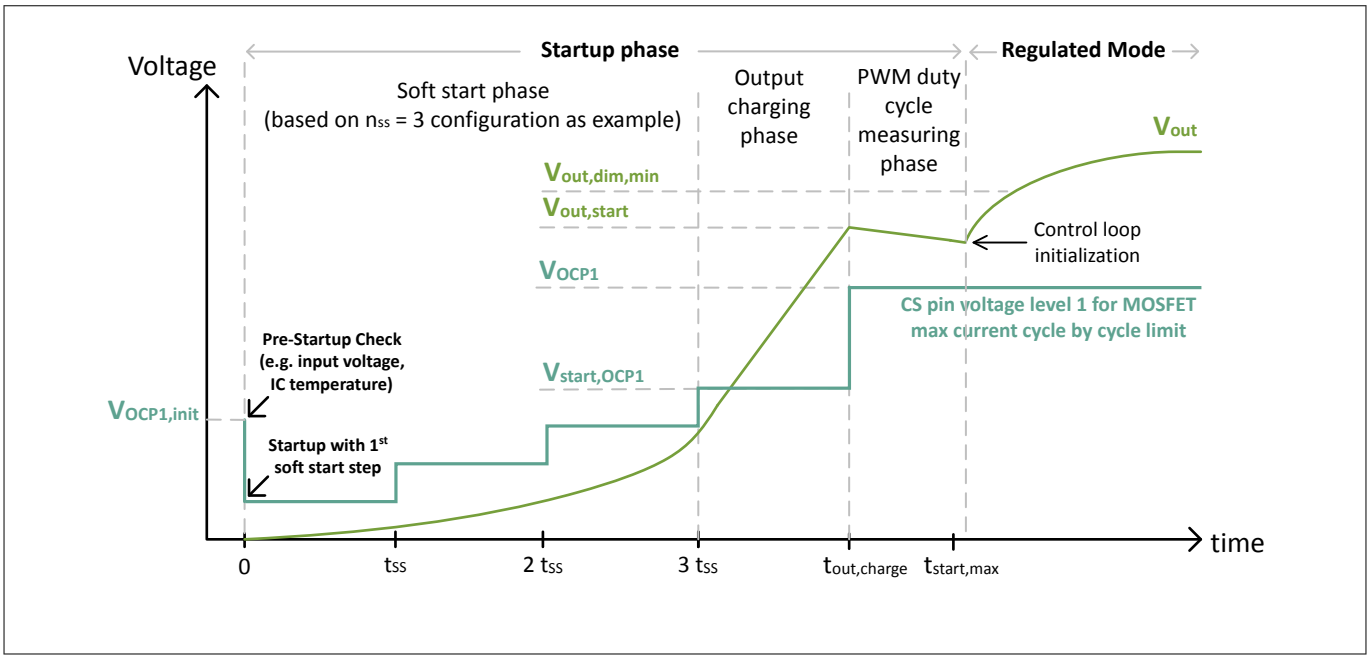


Figure 12 Start up phase with soft start step n_{ss}=3

During soft start phase, the switching frequency is fixed at 20 kHz. The MOSFET current is limited in the first soft start step based on *CS* pin maximum voltage limit of $V_{start,OCP1}/(n_{ss}+1)$, where $V_{start,OCP1}$ is the parameter for the output charging phase *CS* pin maximum voltage limit and n_{ss} is the parameter for the number of soft start steps. The soft start phase CS pin maximum voltage limit is increased by $V_{start,OCP1}/(n_{ss}+1)$ after each soft start step until $V_{start,OCP1}$ is reached, and the typical duration of each soft start step t_{ss} is $3.2/n_{ss}$ ms or 0.5 ms, whichever is lower.

During output charging phase, the output voltage is fast charged with MOSFET switching pulses based on either the output charging phase *CS* pin maximum voltage limit of $V_{start,OCP1}$ or the maximum on time of $t_{on,max}$ in ***QRM1***. To exit the startup phase and enter the regulated mode without triggering the startup output undervoltage protection, the *ZCD* pin estimated output voltage V_{out} has to reach the output charging voltage set-point of $V_{out,start}$ before the maximum allowable startup phase duration of $t_{start,max}$ is reached (see example in ***Figure 12***). To avoid output overshoot, $V_{out,start}$ should be designed below the fully dimmed minimum output LED voltage $V_{out,dim,min}$.

$t_{start,max}$ parameter can be indirectly configured with *VCC* capacitance parameter C_{VCC}, based on:

$$t_{start,\,max} = 967 \cdot C_{VCC}$$

Equation 3

Note: A typical leading edge blanking time $t_{CS,LEB}$ of 480 ns applies on $V_{OCP1,init}$, $V_{start,OCP1}$ and the CS pin maximum voltage limit for every soft start step starting from $V_{start,OCP1}/(n_{ss}+1)$.

During the PWM duty cycle measurement phase, the MOSFET switching pulses are based on very short on-time and switching frequency of $f_{sw,DIM,DCM}$ (1 kHz typically).

After the startup phase is ended with neither protection triggering nor dim-to-off entering, the control loop is initialized for output current regulation in the regulated mode.

3.4 Line synchronization

The XDPL8210 synchronizes most of its operation to the AC input half sine wave period or the rectified AC input frequency, via the *HV* pin. For instance, based on AC input frequency of 50 Hz, the line synchronization

should be based on the rectified AC input frequency of 100 Hz or AC input half sine wave period of 10 ms. Such line synchronization is used for the enhanced ***PFC*** in compensating the input current displacement caused by the line filter and DC link filter capacitor. If the line synchronization is not established, for example during startup, the controller would synchronize its operation based on an internally preset half sine wave period of approximately 9.823 ms.

3.5 Input voltage, output voltage and output current estimation

As shown in ***Figure 13***, the auxiliary winding voltage signal V_{AUX} sensed via *ZCD* pin contains information of the transformer demagnetization time t_{demag}, reflected output voltage and reflected input voltage, while the primary peak current signal $I_{p,pk}$ sensed via *CS* pin contains the secondary peak current $I_{s,pk}$ information. To estimate the output current, the t_{demag} and $I_{s,pk}$ information are necessary.

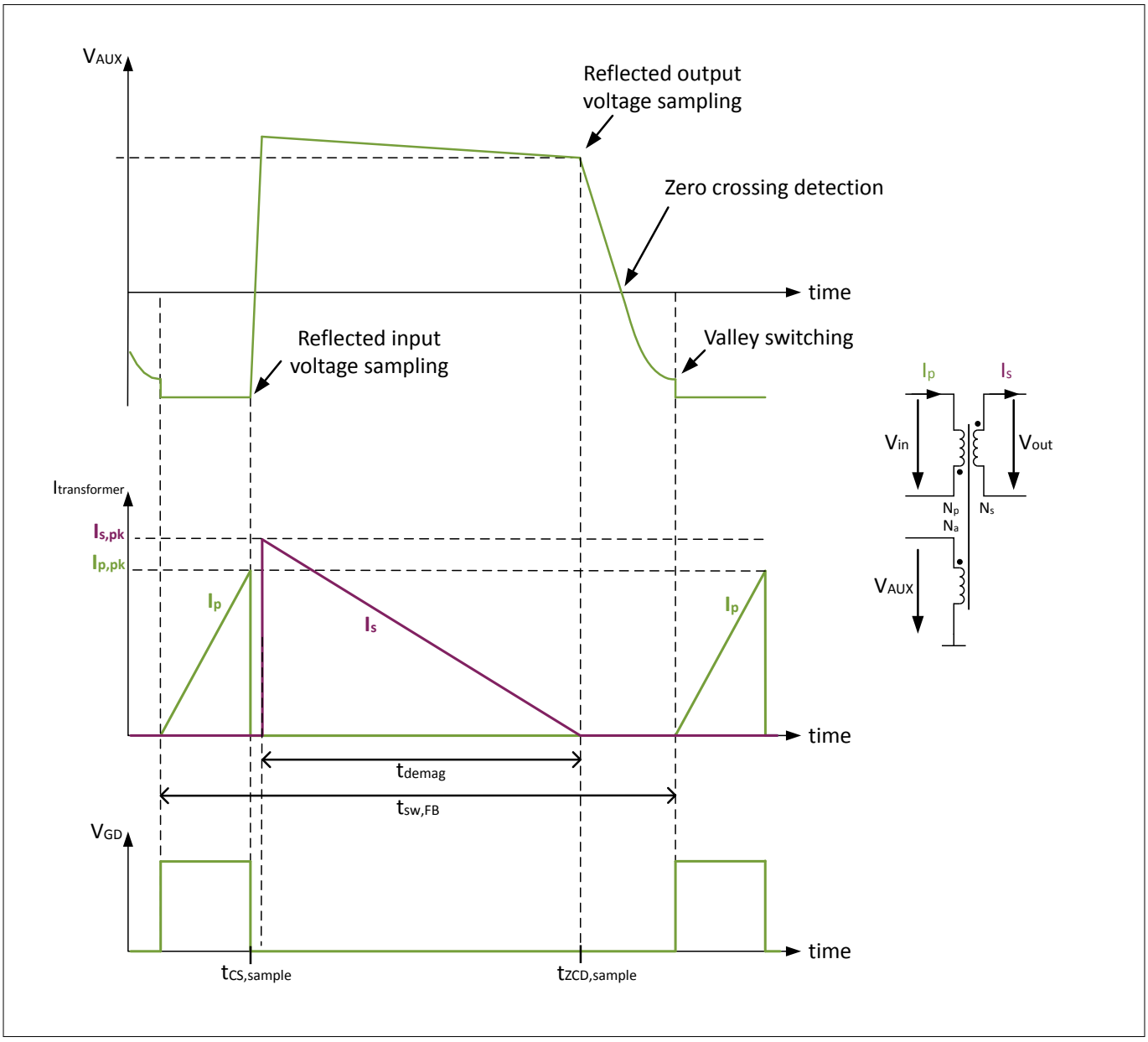


Figure 13 Flyback switching waveform example in QRM1

3.5.1 Input voltage estimation

The input voltage is estimated by sensing the reflected input voltage signal from the transformer primary auxiliary winding voltage V_{AUX}, when the MOSFET is switched on. As the reflected input voltage signal is a negative voltage which cannot be sensed directly, the voltage at *ZCD* pin is clamped to a negative voltage of V_{INPCLN}. A resistor divider with $R_{ZCD,1}$ and $R_{ZCD,2}$ adapts $-I_{IV}$ which is the clamping current flowing out of *ZCD* pin, based on its operational range, while a *ZCD* pin filter capacitor C_{ZCD} is needed for noise filtering, as shown in ***Figure 14***.

Based on the sampled clamping current $-I_{IV}$ at the timing of $t_{CS,sample}$ shown in ***Figure 13***, which is at the end of on-time, the reflected input voltage signal from V_{AUX} is sensed. The interval of each $-I_{IV}$ sample is approximately 1/64 of the half sine wave period.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

The estimated peak input voltage $V_{in,peak}$ over a half sine wave period is based on:

$$V_{\text{in, peak}} = \max\left\{\frac{N_p}{N_a} \cdot \left[\left(-I_{IV} - \frac{V_{INPCLN}}{R_{ZCD,2}}\right) \cdot R_{ZCD,1} - V_{INPCLN}\right] + \frac{R_{in}}{R_{CS}} \cdot V_{CS,peak}\right\}$$

Equation 4

Where N_p is the primary main winding turns, N_a is the primary auxiliary winding turns, R_{CS} is the *CS* pin shunt resistor value, $V_{CS,peak}$ is the peak *CS* pin voltage, and R_{in} is the fine-tuning parameter for input voltage sensing accuracy improvement by compensating the switching frequency voltage ripple on $C_{DC,filter}$.

The estimated input voltage V_{in} in rms value is assumed by the controller as 0.707 of $V_{in,peak}$ based on a filtered value over a few half sine wave periods. The update rate of V_{in} is once per half sine wave period.

$$V_{\text{in}} = 0.707 \cdot V_{\text{in, peak}}$$

Equation 5

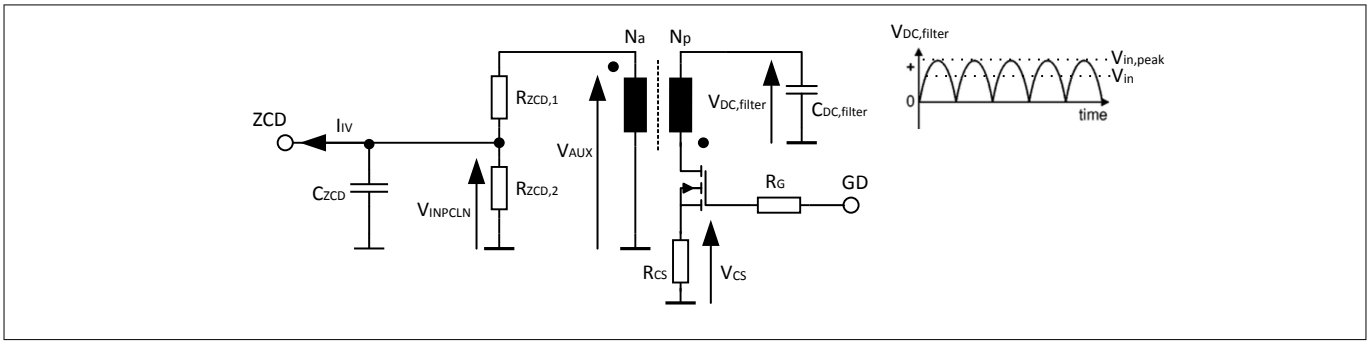


Figure 14 Input voltage estimation based on $-I_{IV}$

The estimated input voltage V_{in} is used for input voltage protections and the enhanced ***PFC*** (EPFC). Therefore, it is important to ensure that ***IC*** parameters $R_{ZCD,1}$, $R_{ZCD,2}$, N_p, N_a and R_{CS} are configured as per the actual system hardware dimensioning.

3.5.2 Output voltage estimation

The output voltage is estimated by sensing the reflected output voltage signal from the transformer primary auxiliary winding voltage V_{AUX}, when the MOSFET is switched off and near the end of transformer demagnetization. A resistor divider with $R_{ZCD,1}$ and $R_{ZCD,2}$ adapts the voltage at *ZCD* pin based on its operational range, while a *ZCD* pin filter capacitor C_{ZCD} is needed for noise filtering, as shown in ***Figure 15***.

Based on the sampled *ZCD* pin voltage $V_{ZCD,SH}$ at the timing of $t_{ZCD,sample}$ shown in ***Figure 13***, which is approximately a quarter of oscillation period ($T_{osc}/4$) before the 1st zero crossing of V_{AUX}, a ratio of the reflected

output voltage signal from V_{AUX} is sensed. The interval of each $V_{ZCD,SH}$ sampling is approximately 1/64 of the half sine wave period, while the oscillation period T_{osc} is measured once before startup and updated every 7th half sine wave period after entering the regulated mode.

Note: *The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

Note: *As V_{AUX} zero crossing can only be detected by the **IC** via ZCD pin upon its internal analog delay plus external delay caused by C_{ZCD}, t_{ZCDPD} parameter fine-tuning is needed to compensate such delays, to have the proper timing of $t_{ZCD,sample}$ for output voltage estimation.*

Attention**: **Please note that the transformer demagnetization time t_{demag} has to be longer than 2.0 µs to ensure that the reflected output voltage can be sensed properly at the ZCD pin.

The estimated output voltage V_{out} is based on:

$$V_{\text{out}} = V_{\text{ZCD, SH}} \cdot \frac{R_{\text{ZCD, 1}} + R_{\text{ZCD, 2}}}{R_{\text{ZCD, 2}}} \cdot \frac{N_s}{N_a} - V_d$$

Equation 6

Where N_s is the transformer secondary main winding turns, N_a is the transformer primary auxiliary winding turns and V_d is the secondary main output diode forward voltage (assumed by the controller as 0.7 V).

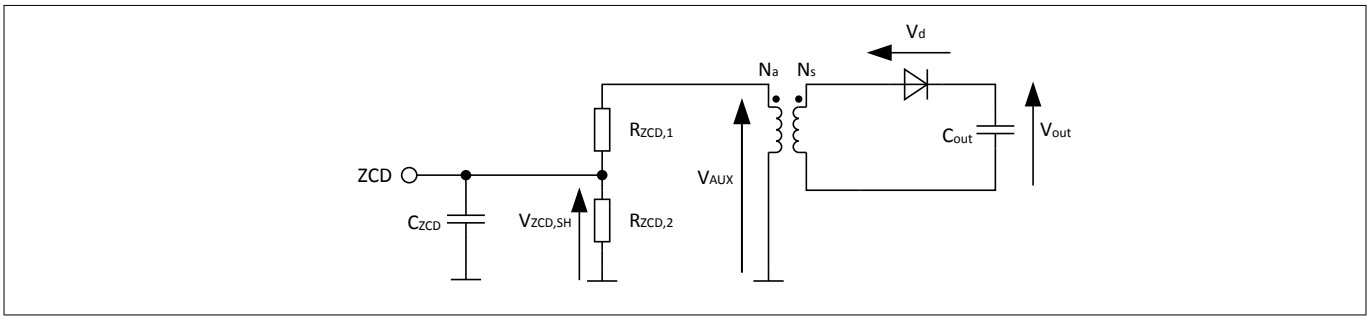


Figure 15 Output voltage estimation based on $V_{ZCD,SH}$

The estimated output voltage V_{out} is used for output voltage protections and the enhanced **PFC** (EPFC). Therefore, it is important to ensure that IC parameters $R_{ZCD,1}$, $R_{ZCD,2}$, N_s and N_a are configured as per the actual system hardware dimensioning.

3.5.3 Output current estimation

Based on the sampled *CS* pin voltage $V_{CS,SH}$ at the timing of $t_{CS,sample}$ shown in **Figure 13**, which is at the end of on-time, the primary peak current signal $I_{p,pk}$ is sensed. The interval of each $V_{CS,SH}$ sample is approximately 1/64 of the half sine wave period.

Note: *The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

To compensate the propagation delay between the falling edges of *GD* pin voltage and $I_{p,pk}$, as shown in **Figure 16**, a more accurate primary peak current $I_{p,pk}$ can be estimated by optimizing the propagation delay compensation parameter t_{PDC} value:

$$I_{p,\text{pk}} = \frac{V_{\text{CS, SH}}}{R_{\text{CS}}} \cdot \frac{t_{\text{on}} + t_{\text{PDC}}}{t_{\text{on}}}$$

Equation 7

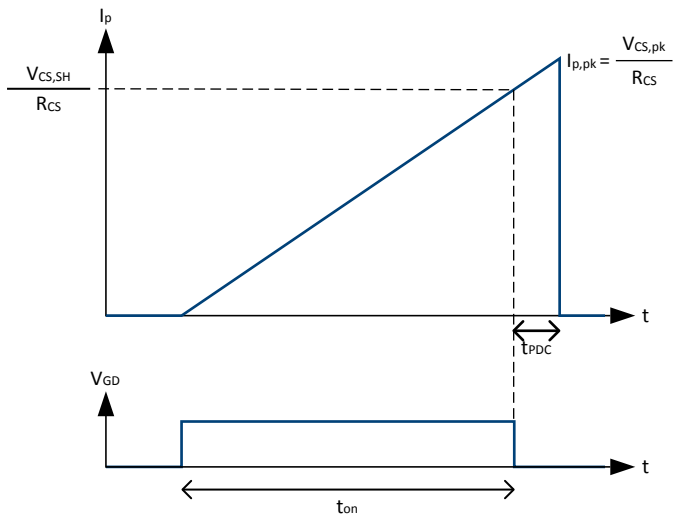


Figure 16 Propagation delay compensation for more accurate primary peak current estimation

The secondary peak current $I_{s,pk}$ can be estimated based on $I_{p,pk}$, transformer turns ratio N_p/N_s, transformer coupling coefficient $K_{coupling}$, primary main winding inductance L_p and primary leakage inductance $L_{p,lk}$:

$$I_{s,\mathrm{pk}} = I_{p,\mathrm{pk}} \cdot \frac{N_p}{N_s} \cdot K_{\mathrm{coupling}} \cdot \frac{L_p}{L_p + L_{p,\mathrm{lk}}}$$

Equation 8

Note: $L_{p,lk}$ is 1% of L_p by default.

The average output current per switching cycle $I_{out}(n)$ can be estimated based on $I_{s,pk}$, transformer demagnetization time t_{demag}, switching period t_{sw}, ***ABM*** pulse number N_{ABM}, line frequency f_{line}, ***DCM*** minimum switching frequency parameter $f_{sw,min,DCM}$, the estimated output voltage V_{out}, output undervoltage protection level V_{outUV} and the auxiliary loss compensation parameter G_{loss} which is to achieve better load regulation at low output current.

- $I_{out}(n)$ in ***QRM1*** and ***DCM***:

$$I_{\mathrm{out,\,QRM1,\,DCM}}(n) = \frac{1}{2} \cdot I_{s,\mathrm{pk}} \cdot \frac{t_{\mathrm{demag}}}{t_{\mathrm{sw}}} - G_{\mathrm{out,\,loss}} \cdot (V_{\mathrm{out}} - V_{\mathrm{outUV}})$$

Equation 9

- $I_{out}(n)$ in ***ABM***:

$$I_{\mathrm{out,\,ABM}}(n) = \frac{1}{2} \cdot I_{s,\mathrm{pk}} \cdot \frac{t_{\mathrm{demag}}}{t_{\mathrm{sw}}} \cdot N_{\mathrm{ABM}} \cdot \frac{2 \cdot f_{\mathrm{line}}}{f_{\mathrm{sw,\,min,\,DCM}}} - G_{\mathrm{out,\,loss}} \cdot (V_{\mathrm{out}} - V_{\mathrm{outUV}})$$

Equation 10

The interval of each $I_{out}(n)$ sample is approximately 1/64 of the half sine wave period. The average output current per half sine wave period for output regulation is obtained from the moving average filter based on 64 $I_{out}(n)$ samples.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

3.6 Power factor correction

For better ***PFC***, the patented enhanced PFC (EPFC) feature can be enabled by configuring C_{EMI} parameter value above zero and fine-tuning the value, to compensate the input current displacement effect which is mainly caused by the DC link filter capacitor $C_{DC,filter}$. With this feature enabled, in ***QRM1***, the regulated on-time is not constant, but modulated with a function based on the estimated input voltage V_{in}, estimated output voltage V_{out}, estimated output current, phase angle and modulation gain of C_{EMI} parameter value.

The enhanced PFC (EPFC) feature can also be disabled by configuring C_{EMI} parameter as zero.

3.7 Dimming control

The XDPL8210 senses the duty cycle of the *PWM* pin voltage signal, to determine the output current set-point based on the configured dimming curve and maximum power limit setting. In regulated mode, the output current is analogue (except for ***ABM***) and the output ripple frequency is synchronized to the double line frequency, to achieve flicker-free operation.

PWM pin internal pull up resistor

The *PWM* pin internal pull up resistor can be optionally enabled by configuring $PWM_{R,pull,up}$ parameter between 2.25 kohm and 30 kohm. The internal pull up voltage is 3.2 V typically.

PWM pin duty cycle sensing and frequency range

The XDPL8210 can sense the duty cycle based on either a normal ***PWM*** signal or an inverted PWM signal, by configuring the PWM_{type} parameter.

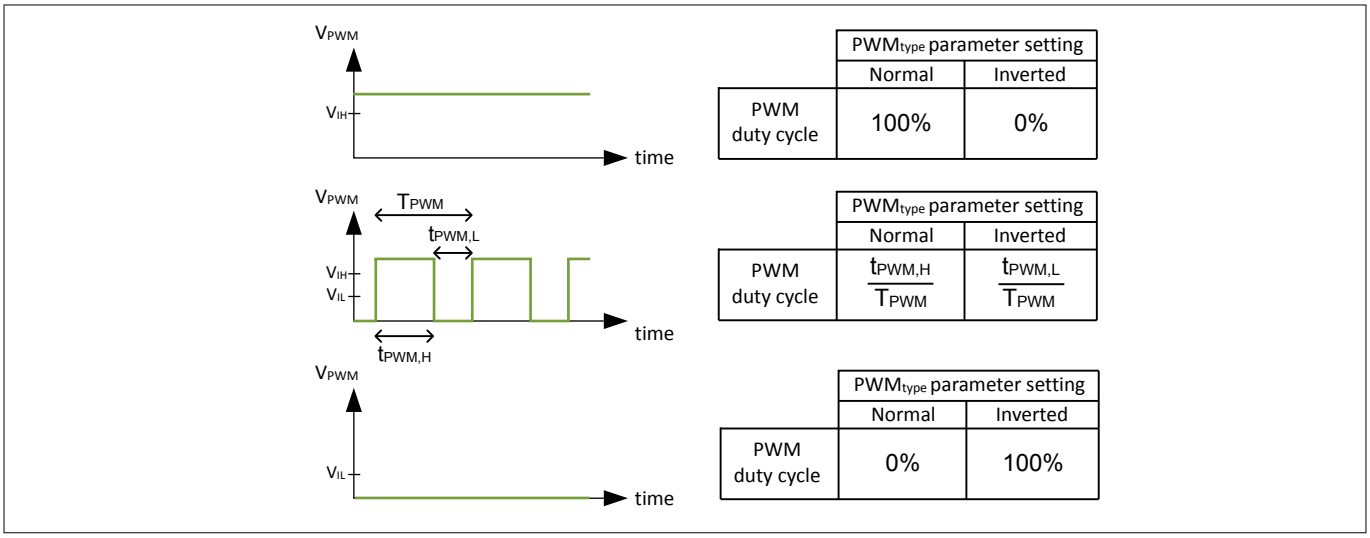


Figure 17 Duty cycle based on the selectable PWM type

To sense a stable PWM duty cycle level for the regulation based on a stable output current set-point, a hysteresis level for PWM duty cycle jittering suppression is configurable based on $PWM_{Duty,hyst}$ parameter. Any change of the PWM duty cycle within the hysteresis will not affect the output current.

The PWM frequency should be fixed in the range of 500 Hz and 2 kHz.

Dimming curve

The XDPL8210 can be configured based on C_{DIM} parameter, to use either a linear or a quadratic dimming curve for the mapping of the PWM duty cycle to the output current set-point, as shown in ***Figure 18***. The PWM duty cycle levels of $D_{DIM,min}$ and $D_{DIM,max}$ ensure that the minimum current $I_{out,min}$ and maximum current $I_{out,full}$ can always be achieved, thereby making the application robust against component tolerances.

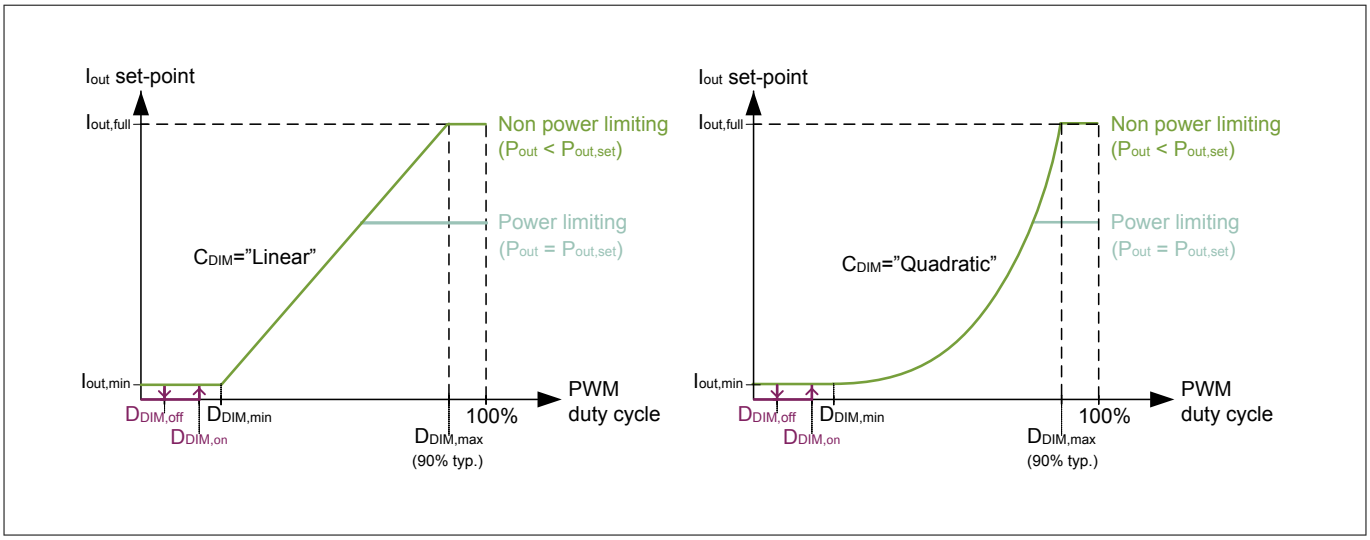


Figure 18 Selectable Dimming Curves

If the DIM_{type} parameter is configured as "Dim (to off)", dim-to-off is entered to turn off the light output when the measured PWM duty cycle gets below $D_{DIM,off}$ (see purple line in ***Figure 18***). During dim-to-off, if the measured PWM duty cycle gets above $D_{DIM,on}$, the regulated mode is entered to turn on the light output. After hardware reset, if the first measured PWM duty cycle is above $D_{DIM,off}$, the regulated mode is entered to turn on the light output.

During dim-to-off, the output voltage is recharged (based on $V_{out,start}$ parameter) to measure the PWM duty cycle, every fast auto-restart period $t_{auto,restart,fast}$ of 400 ms approximately. While the PWM duty cycle measurement is ongoing, the controller *GD* pin switching frequency is based on $f_{sw,DIM,DCM}$ of 1 kHz typically. To achieve low standby power during dim-to-off, the sleep mode is entered if the measured PWM duty cycle gets below $D_{DIM,off}$.

Note: A weak passive bleeder on the output is required for proper dim-to-off operation.

If the DIM_{type} parameter is configured as "Dim (without off)", the light output is not turned off and the output current set-point is based on $I_{out,min}$ when the measured PWM duty cycle gets below either $D_{DIM,min}$ or $D_{DIM,off}$ (see green line in ***Figure 18***).

If the output power is limited by $P_{out,set}$, the output current set-point follows the cyan line in ***Figure 18*** which would result to extended dead travel below $D_{DIM,max}$. As soon as the product of output current and output voltage drops below $P_{out,set}$, the output current will follow the green line, as shown in ***Figure 18***)).

3.8 Protection features

Protections ensure the operation of the controller under restricted conditions. The protection monitoring signal(s) sampling rate, protection triggering condition(s) and protection reaction are described in this section.

Attention: The sampled protection monitoring signal accuracy is subjective to the digital quantization, tolerances of components (including IC) and estimations with indirect sensing (e.g. input and output voltage estimations based on ZCD, CS pin signals), while the protection level triggering accuracy is subjective to the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.

3.8.1 Primary MOSFET overcurrent protection

V_{OCP2} denotes the *CS* pin voltage level 2 for primary MOSFET overcurrent protection. Under the single fault condition of shorted primary main winding, the primary MOSFET overcurrent protection is triggered when the *CS* pin voltage exceeds V_{OCP2} for longer than a blanking time based on t_{CSOCP2} parameter.

Note: t_{CSOCP2} parameter is 240 ns by default.

The level of V_{OCP2} is automatically selected based on ***#unique_39/unique_39_Connect_42_table_dxh_gzl_jhb***.

Table 2 V_{OCP2} level selection depending on V_{OCP1} parameter value

V_{OCP1} (V)	V_{OCP2} (V)
0.40 to 0.54	0.8
0.55 to 0.72	1.2
0.73 to 1.08	1.6

The reaction of primary MOSFET overcurrent protection is fixed as auto-restart.

3.8.2 Output undervoltage protection

In case of a short or too low LED load voltage, the output voltage would drop to a low level. The output undervoltage protection can be triggered, if the condition is met by monitoring the estimated output voltage V_{out} based on the *ZCD* pin switching signal (see ***Output voltage estimation*** for details).

In regulated mode, if the estimated output voltage V_{out} is lower than the V_{outUV} parameter for longer than a blanking time of $t_{VoutUV,blank}$ parameter, the regulated mode output undervoltage protection is triggered.

The reaction of the regulated mode output undervoltage protection is fixed as auto-restart.

Note: By default, V_{outUV} is fixed as 50% of the configurable $V_{out,dim,min}$ parameter. $V_{out,dim,min}$ denotes the fully dimmed minimum output LED voltage.

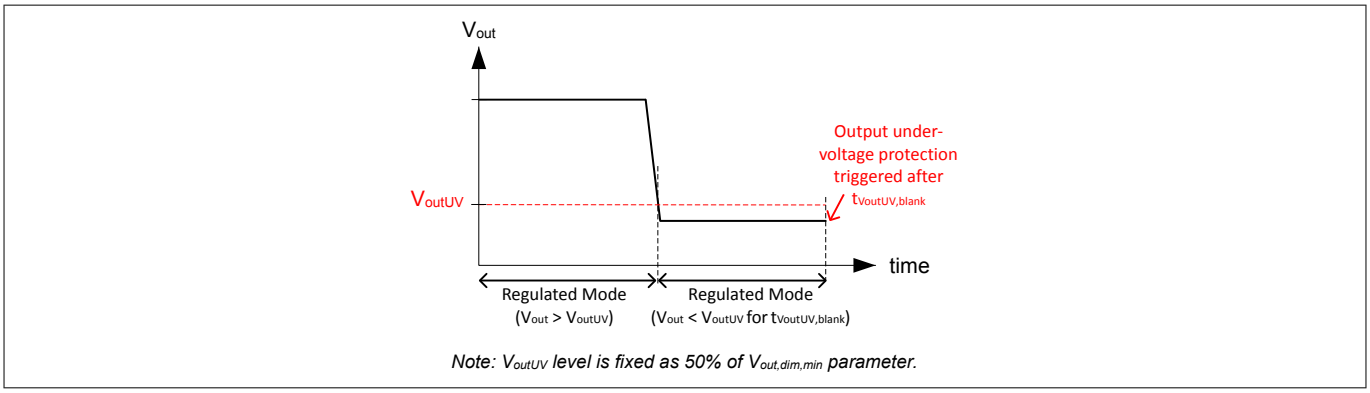


Figure 19 Regulated mode output undervoltage protection

In startup phase, if the estimated output voltage V_{out} is lower than $V_{out,start}$ parameter over a timeout period of $t_{start,max}$ parameter, the startup output undervoltage protection is triggered. $t_{start,max}$ parameter refers to the maximum allowable duration of the soft-start phase and output charging phase. It can be indirectly configured with *VCC* capacitance parameter C_{VCC}.

The reaction of startup output undervoltage protection is fixed as auto-restart.

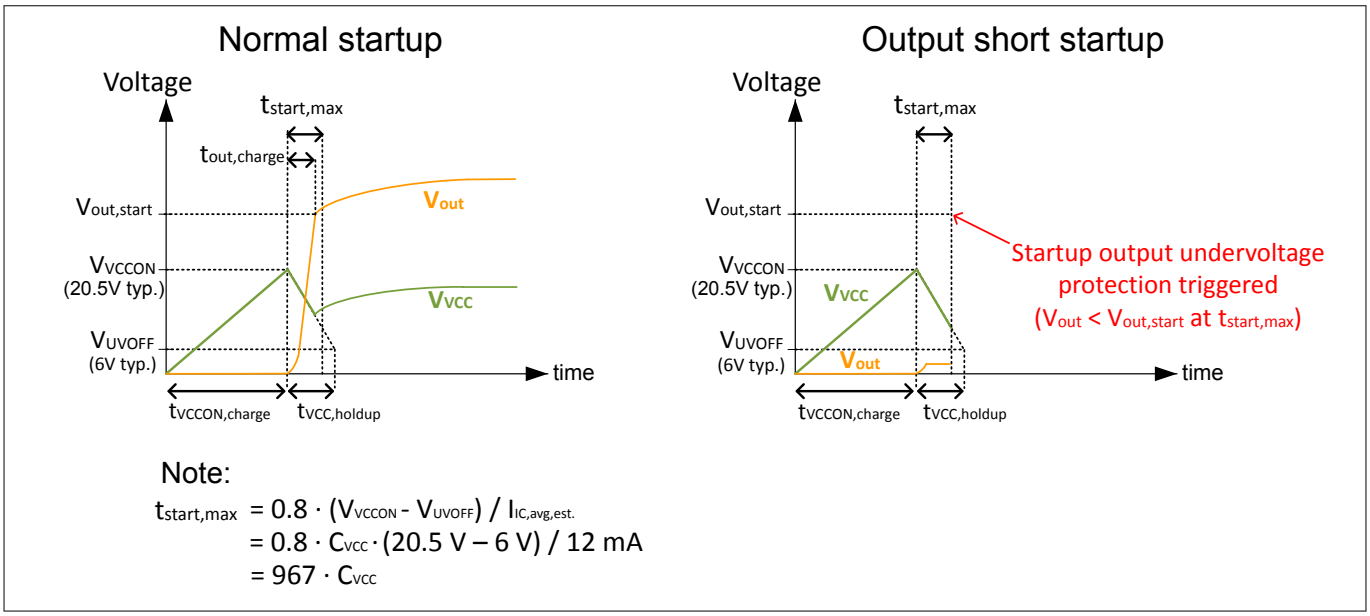


Figure 20 Normal startup and startup output undervoltage (short) protection waveforms

3.8.3 Output overvoltage protection

In case of output open, the output voltage may rise to a high level. The output overvoltage protection can be triggered, if the condition is met by monitoring the estimated output voltage V_{out} based on the *ZCD* pin switching signal (see ***Output voltage estimation*** for details).

If the estimated output voltage V_{out} is higher than V_{outOV} for longer than a blanking time, the output overvoltage protection is triggered.

*Note: In **QRM1** and **DCM**, the blanking time is typically a quarter of the half sine wave period. In **ABM**, the blanking time is configurable based on $t_{VoutOV,blank,ABM}$ parameter.*

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

The reaction of the output overvoltage protection is configurable to auto-restart or latch-mode based on $Reaction_{OVP,Vout}$ parameter. ***Figure 21*** shows an example of the output overvoltage protection and recovery waveform, based on the auto-restart reaction.

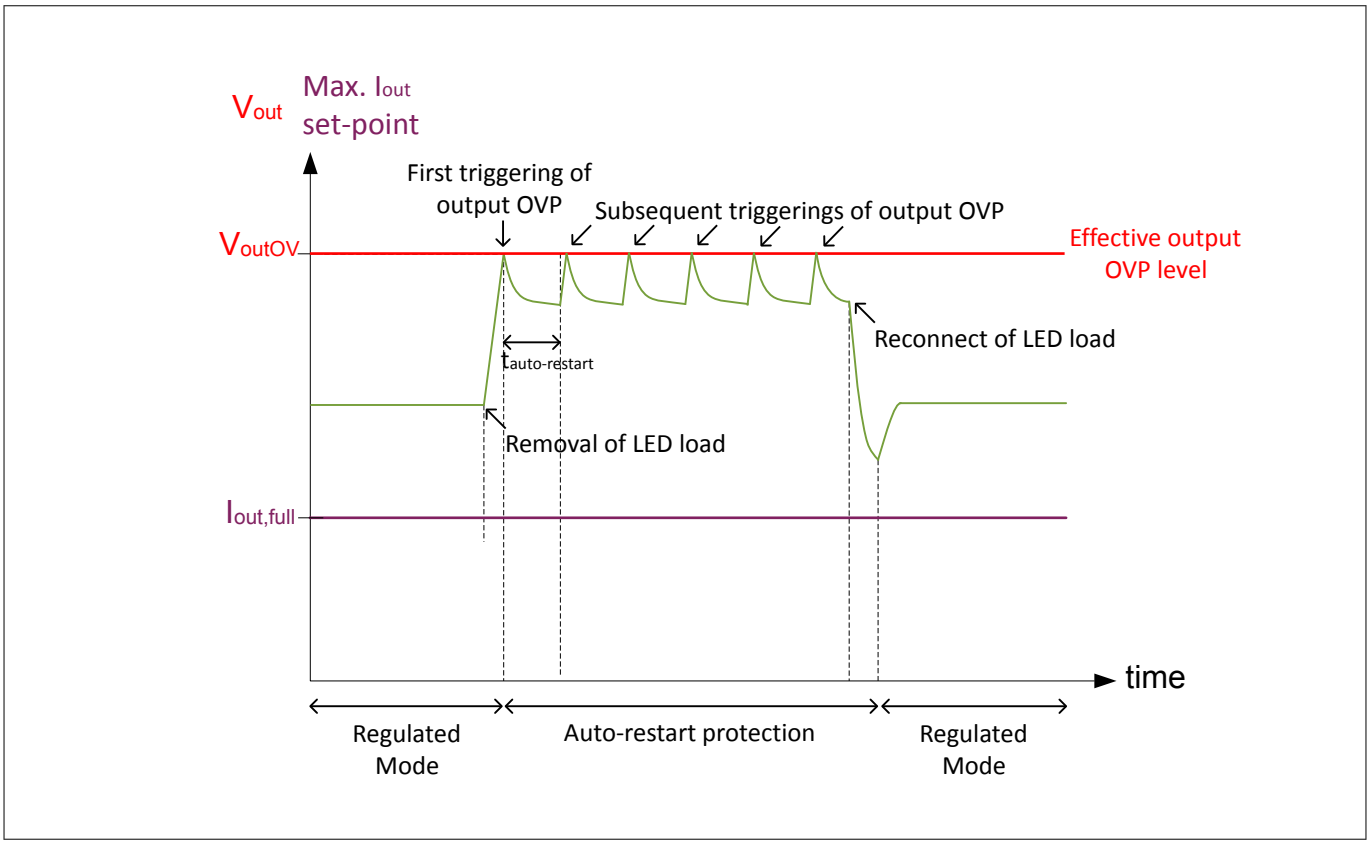


Figure 21 Output overvoltage protection and recovery waveform

***Attention**: It is mandatory to ensure that V_{outOV} is configured well below the actual output capacitor voltage rating $V_{out,cap,rating}$,while the $V_{out,cap,rating}$ is not exceeded in actual testing with all the necessary test conditions. The protection level triggering accuracy is subjective to the sampled signal accuracy, sampling delay, indirect sensing delay (e.g. reflected output voltage signal cannot be sensed by ZCD pin near AC input phase angle of 0° and 180°) and blanking time.*

***Attention**: If the minimum ABM switching pulses number parameter $N_{ABM,min}$ and minimum output current parameter $I_{out,min}$ configured values are both very low, the output overvoltage protection actual triggering level might drift up when output current set-point is $I_{out,min}$.*

Adaptive output overvoltage protection level

To have lower output open load voltage during auto-restart, the adaptive output overvoltage protection can be enabled with the $EN_{adaptive,OVP,Vout}$ parameter, as shown in ***Figure 22***.

Upon triggering the enabled adaptive output overvoltage protection for the first time, the protection level is reduced from $V_{out,OV}$ to $V_{out,OV,red}$ and the output current set-point maximum limit is reduced from $I_{out,full}$ to $I_{out,OVP,red}$.

For a successful output recovery, the estimated output voltage V_{out} upon auto-restart has to be lower than $V_{out,OV,red}$ for a number of half sine wave periods based on $N_{Vout,restore}$ parameter, in order to restore the protection level and the output current set-point maximum limit to $V_{out,OV}$ and $I_{out,full}$, respectively.

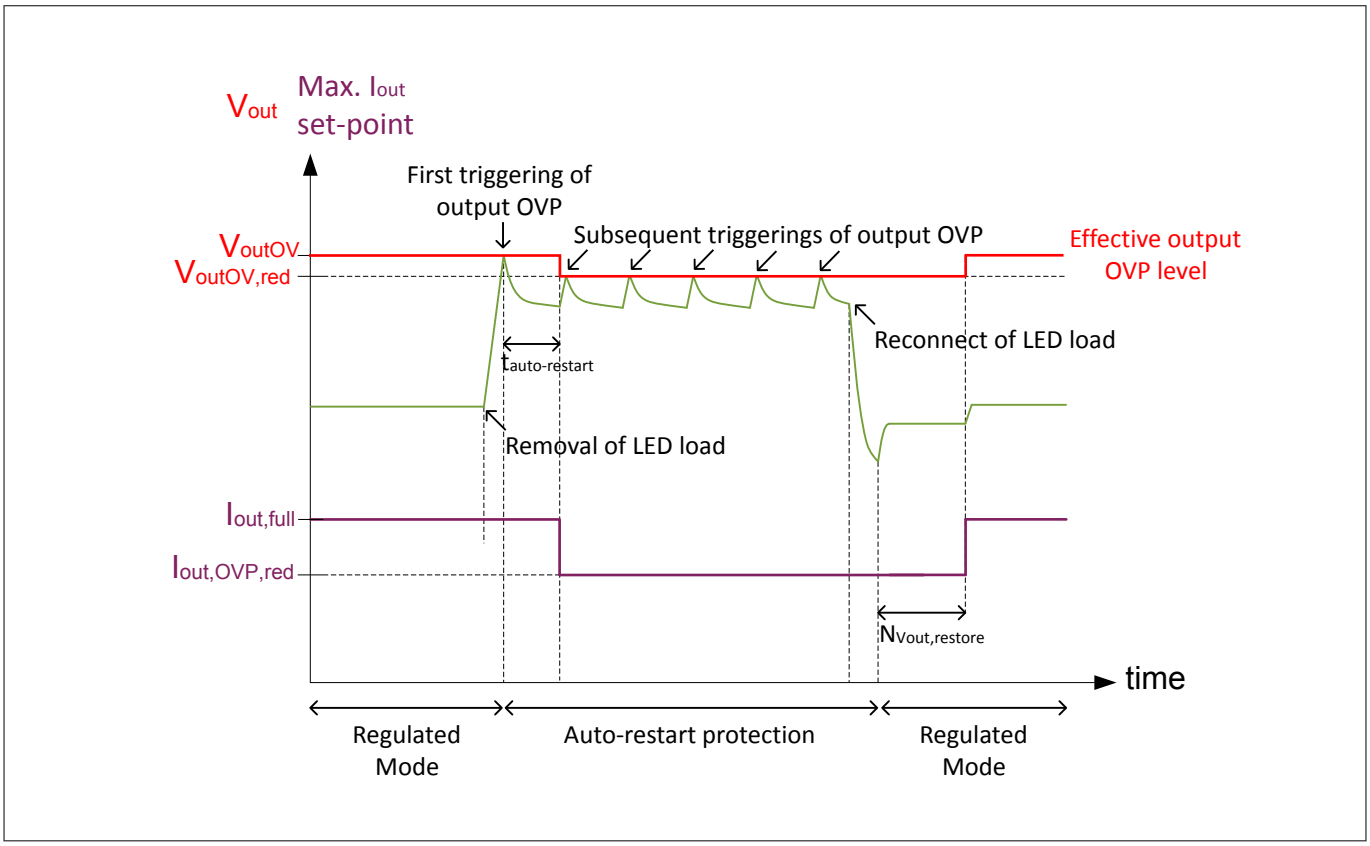


Figure 22 Adaptive output overvoltage protection and recovery waveform

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

3.8.4 Transformer demagnetization time shortage protection

In case of insufficient transformer demagnetization time, the reflected output voltage signal cannot be properly sensed via the *ZCD* pin. If such condition presents for longer than 50% of a half sine wave period, the protection will be triggered. The reaction of this protection is fixed as auto-restart.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

3.8.5 Regulated mode peak output overcurrent protection

By monitoring the estimated average output current per switching cycle based on the switching signals (see ***Output current estimation*** for details), the regulated mode peak output overcurrent protection can be triggered if the condition is met.

$EN_{Iout,max,peak}$ parameter refers to the enable switch for the regulated mode peak output overcurrent protection.

Upon startup and in the regulated mode, if $EN_{Iout,max,peak}$ parameter is enabled and the average output current per switching cycle is higher than $I_{out,max,peak}$ for longer than a blanking time, the regulated mode peak output current protection will be triggered. The blanking time is based on $I_{out,max,peak,blank}$ parameter.

The reaction of the regulated mode peak output overcurrent protection is fixed as auto-restart. The auto-restart speed is configurable based on $Speed_{OCP,Iout}$ parameter:

- If $Speed_{OCP,Iout}$ is configured as "fast", the auto-restart time is approximately 0.4 second.
- If $Speed_{OCP,Iout}$ is configured as "slow", the auto-restart time is based on the configurable $t_{auto,restart}$ parameter.

3.8.6 Minimum input voltage startup check and input undervoltage protection

By monitoring the estimated input voltage V_{in} based on the *ZCD* pin and *CS* pin switching signals (see ***Input voltage estimation*** for details), the minimum input voltage startup check can be performed, and the input undervoltage protection can be triggered if the condition is met.

$EN_{UVP,In}$ parameter refers to the enable switch for the minimum input voltage startup check (based on $V_{in,start,min}$) and input undervoltage protection (based on V_{inUV}).

Note: $V_{in,start,min}$ parameter refers to the minimum input voltage level for startup, while V_{inUV} parameter refers to the input undervoltage protection level.

During pre-startup check, if $EN_{UVP,In}$ parameter is enabled and the estimated input voltage V_{in} is lower than $V_{in,start,min}$, the startup phase will not be entered and the protection reaction of auto-restart will be performed.

Upon startup and in the regulated mode, if $EN_{UVP,In}$ parameter is enabled and the estimated input voltage V_{in} is lower than V_{inUV} for longer than a blanking time, the input undervoltage protection will be triggered. The blanking time of the input undervoltage protection is typically 10 half sine wave periods.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

The reaction of the input undervoltage protection is fixed as auto-restart.

3.8.7 Maximum input voltage startup check and input overvoltage protection

By monitoring the estimated input voltage V_{in} based on the *ZCD* pin and *CS* pin switching signals (see ***Input voltage estimation*** for details), the maximum input voltage startup check can be performed, and the input overvoltage protection can be triggered if the condition is met.

$EN_{OVP,In}$ parameter refers to the enable switch for the maximum input voltage startup check (based on $V_{in,start,max}$) and input overvoltage protection (based on V_{inOV}).

Note: $V_{in,start,max}$ parameter refers to the maximum input voltage level for startup, while V_{inOV} parameter refers to the input overvoltage protection level.

During pre-startup check, if $EN_{OVP,In}$ parameter is enabled and the estimated input voltage V_{in} is higher than $V_{in,start,max}$, the startup phase will not be entered and the protection reaction of auto-restart will be performed.

Upon startup and in the regulated mode, if $EN_{OVP,In}$ parameter is enabled and the estimated input voltage V_{in} is higher than V_{inOV} for longer than a blanking time, the input overvoltage protection will be triggered. The blanking time of the input overvoltage protection is typically 1 half sine wave period.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

The reaction of the input overvoltage protection is fixed as auto-restart.

3.8.8 VCC undervoltage lockout

The ***Undervoltage Lockout (UVLO)*** is implemented in the hardware. It ensures the enabling and disabling of the ***IC*** operation based on the defined thresholds of the operating supply voltage V_{VCC} at the *VCC* pin.

The UVLO contains a hysteresis with the voltage thresholds V_{VCCon} for enabling the controller and V_{UVOFF} for disabling the controller. Once the mains input voltage is applied, current flows through an external resistor into the *HV* pin via the integrated depletion cell and diode to the *VCC* pin. The controller is enabled once V_{VCC} exceeds the V_{VCCon} threshold and V_{VCC} will then start to drop. For normal startup, V_{VCC} supply should be taken over by either external supply or the self-supply via the auxiliary winding before V_{VCC} drops to V_{UVOFF}.

3.8.9 VCC overvoltage protection

If the sampled *VCC* voltage is higher than the *VCC* overvoltage protection level $V_{VCC,max}$, the *VCC* overvoltage protection will be triggered. The *VCC* overvoltage protection reaction is fixed as auto-restart.

The *VCC* voltage is sampled once per 7 half sine wave periods.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

3.8.10 IC overtemperature protection

If the sampled ***IC*** junction temperature T_j is higher than $T_{critical}$ parameter, the IC overtemperature protection will be triggered. The protection reaction is fixed as auto-restart, while the maximum junction temperature for startup and restart $T_{start,max}$ is fixed as 4°C below $T_{critical}$.

The IC junction temperature T_j is sampled once per 7 half sine wave periods.

*Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

Attention**: **IC lifetime is not guaranteed when operating junction temperature is above 125°C, which is possible if $T_{critical}$ is configured above 119°C, with temperature sensing tolerance of ± 6°C.

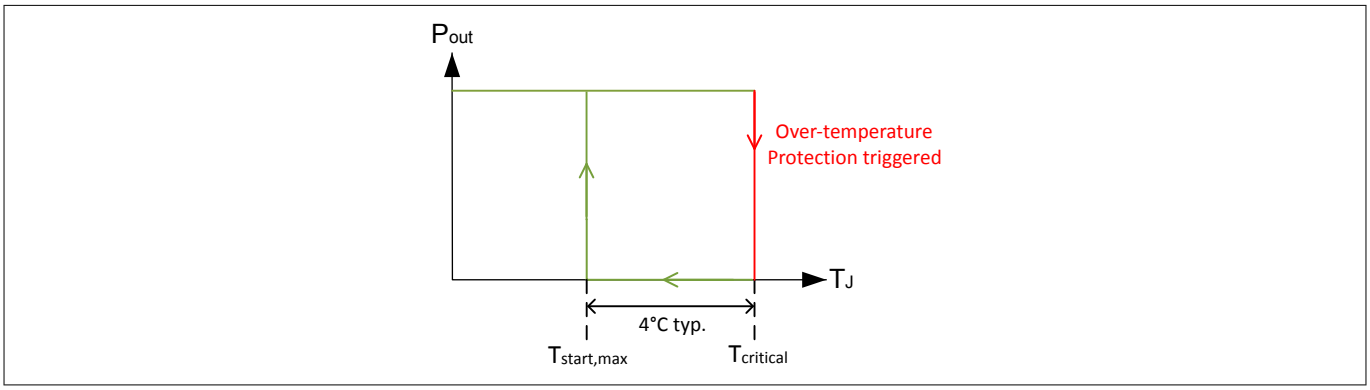


Figure 23 IC overtemperature protection

3.8.11 Other protections

- A hardware weak pull-up protects against an open *CS* pin. The reaction of this protection reaction is auto-restart.
- A firmware watchdog triggers a protection if the ADC hardware cannot provide all necessary information within a defined time period. This may occur if timing requirements for the ADC are exceeded. The reaction of this protection is fast auto-restart.
- A hardware watchdog checks correct execution of firmware. A protection is triggered in the event that the firmware does not service the watchdog within a defined period. The reaction of this protection is auto-restart.
- A hardware parity check triggers a protection if a bit in the memory changes unintentionally. The reaction of this protection is auto-restart.
- A firmware ***Cyclic Redundancy Check*** at each startup verifies the integrity of firmware and parameters. The reaction of this protection is stop mode.
- A firmware task execution watchdog triggers a protection if the firmware tasks are not executed as expected. The reaction of this protection is auto-restart.

- A protection is triggered if the configurable parameter values are empty at startup. The reaction of this protection is stop mode.
- A protection is triggered if no reflected input voltage signal sensed from the *ZCD* pin at startup. The reaction of this protection is stop mode.

3.8.12 Protection reactions

The sequence of a protection reaction (not including hardware restart reaction) is as follows:

1. Upon triggering a protection, the gate driver is disabled within a maximum time, which is 1/512 of the half sine wave period.

   *Note: The half sine wave period is either 9.823 ms or the inverse of the rectified AC input frequency, based on the operating conditions, as explained in **Line synchronization**.*

2. The reaction depends on the triggered protection:
   - In case of latch mode, the application will enter latch mode at this time. No further sequence is done until *VCC* voltage drops below V_{UVOFF}.
   - In case of auto-restart reaction, the controller will enter power saving mode PSMD2 with the auto-restart time based on $t_{auto,restart}$ parameter.
   - In case of fast auto-restart reaction, the controller will enter power saving mode PSMD2 with the fast auto-restart time of 0.4 sec.

   Note: For latch mode, auto-restart and fast auto-restart reactions, the internal HV startup cell is automatically enabled and disabled during this sequence, in order to keep the VCC voltage between the V_{UVLO} and V_{OVLO} thresholds.

   Note: For stop mode, if there is no external voltage supply for the VCC, the VCC voltage will drain to V_{UVOFF} and a hardware restart will be performed.

3. After the (fast) auto-restart time is expired, the controller executes a single discharge pulse of duration t_{pw}. This pulse partially discharges the capacitance after the bridge rectifier to improve accuracy of the next pre-startup input voltage check.
4. Any auto restart may include a new *VCC* charging cycle. The recharging time of *VCC* via *HV* pin current depends on the input voltage level and *VCC* level at the time when the (fast) auto-restart time is expired.
5. The power stage will enable its gate driver for pre-startup check. If the conditions for pre-startup check are within limits, the startup phase is entered and followed by the regulated mode. During this time, if any protection is triggered, the sequence of a protection reaction (not including hardware restart reaction) starts again from step number 1 above.

4 Debug mode

If an unexpected system protection was triggered during testing, the $Debug_{Mode}$ parameter can be enabled to enter stop mode reaction upon the protection triggering (except for *VCC* undervoltage lockout), to read out the firmware status code. For example in ***Figure 24***, the firmware status code readout in the ***GUI*** shows a number of 0040_H (in red color), which indicates that the input undervoltage protection has been triggered.

Note: If there is no protection being triggered, the firmware status code should be 0000_H (in black color).

Note: $Debug_{Mode}$ parameter should only be enabled for debugging purpose. For actual application running, it has to be disabled.

Debug mode

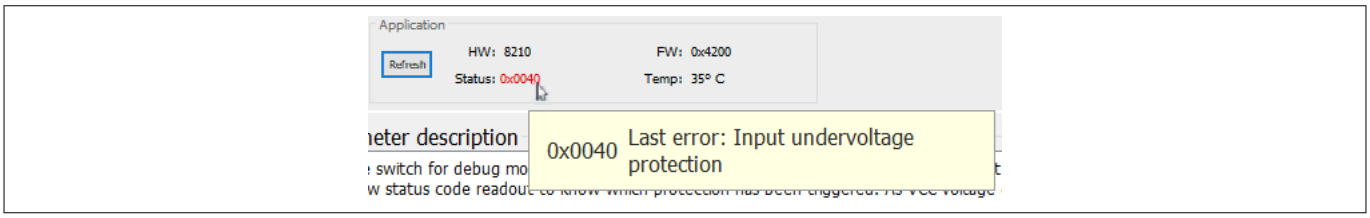


Figure 24 Firmware status code readout for debugging

Please refer to the design guide for the recommended setup & procedures to read out the firmware status code in debug mode.

5 List of Parameters

This list provides information about the configurable and fixed parameters.

This document uses symbols to ease the readability of formulas. As some tools do not support this format, the symbols are translated into plain text using underscores. For example, the parameter $f_{sw,max}$ translates to f_sw_max.

All parameter values are typical settings. The accuracy might vary due to digital quantization and tolerances.

Note: By default, the configurable parameters of a new XDPL8210 chip from Infineon are empty, so it is necessary to configure them digitally via UART pin before any application testing.

List of configurable parameters

Table 3 Configurable parameters for output set-points

Symbol	Basic description	Example	Minimum value	Maximum value
$I_{out,full}$	Steady-state maximum output current set-point	830 mA	Refer GUI	Refer GUI
$P_{out,set}$	Steady-state maximum output power limit set-point	34.5 W	Refer GUI	Refer GUI

Table 4 Configurable parameters for dimming

Symbol	Basic description	Example	Minimum value	Maximum value
DIM_{type}	Dimming type via *PWM* pin	Dim (to off)	• Non-dim • Dim (without off) • Dim (to off)	
$I_{out,min}$	Minimum output current set-point	41.5 mA	Refer GUI	$I_{out,full}$
C_{DIM}	Shape of the dimming curve	Linear	• Linear • Quadratic	
PWM_{type}	*PWM* type	Inverted	• Normal • Inverted	
$f_{PWM,max}$	Maximum switching frequency of PWM dimming signal	1050 Hz	$f_{PWM,min}$	2000 Hz
$f_{PWM,min}$	Minimum switching frequency of PWM dimming signal	950 Hz	500 Hz	$f_{PWM,max}$
$D_{DIM,max}$	*PWM* duty cycle level for maximum output current	90%	$D_{DIM,min}$	Refer GUI
$D_{DIM,min}$	*PWM* duty cycle level for minimum output current	15%	$D_{DIM,off}$	$D_{DIM,max}$
$D_{DIM,on}$	*PWM* duty cycle level for exiting dim-to-off	11%	$D_{DIM,off}$	$D_{DIM,min}$
$D_{DIM,off}$	*PWM* duty cycle level for entering dim-to-off	10%	Refer GUI	$D_{DIM,min}$
$PWM_{Duty,hyst}$	Hysteresis level for *PWM* duty cycle jittering suppression	0.1%	0%	2%

List of Parameters

Table 5 Configurable parameters for hardware configuration

Symbol	Basic description	Example	Minimum value	Maximum value
N_p	Transformer primary main winding turns	58	1	300
N_s	Transformer secondary main winding turns	17	1	300
N_a	Transformer primary auxiliary winding turns	15	1	300
L_p	Transformer primary main winding inductance	0.566 mH	Refer GUI	3 mH
R_{CS}	Current sense resistor value	0.22 Ω	0.1 Ω	3 Ω
$R_{ZCD,1}$	*ZCD* series resistor	56.2 kΩ	Refer GUI	255 kΩ
$R_{ZCD,2}$	*ZCD* shunt resistor	2.7 kΩ	Refer GUI	Refer GUI
VCC_{supply}	*VCC* voltage supply	Wide	• Wide • Narrow • External	
C_{VCC}	*VCC* capacitor value	15 µF	Refer GUI	100 µF
$V_{out,cap,rating}$	Output capacitor voltage rating	80 V	10 V	450 V
R_{HV}	*HV* series resistor	100 kΩ	Refer GUI	255 kΩ
$I_{GD,pk}$	Gate driver peak source current	30 mA	30 mA	118 mA
$PWM_{R,pull,up}$	*PWM* pin internal pull up resistor	2.25 kΩ	2.25 kΩ to 30 kΩ, or Disabled	

Table 6 Configurable parameters for startup

Symbol	Basic description	Example	Minimum value	Maximum value
n_{ss}	Number of soft start steps	20	1	20
$V_{out,dim,min}$	Minimum output voltage when fully dimmed	12 V	$V_{out,start}$	V_{outOV}
$V_{out,start}$	Output charging phase output voltage set-point	10.5 V	*50% of* $V_{out,dim,min}$	$V_{out,dim,min}$
$V_{start,OCP1}$	Output charging phase *CS* pin voltage level 1 for MOSFET max. current cycle by cycle limit	0.5 V	Refer GUI	V_{OCP1}
$V_{OCP1,init}$	Initial *CS* pin voltage level 1 for MOSFET max. current limit on the input voltage measurement pulse before startup	0.3 V	Refer GUI	V_{OCP1}

Table 7 Configurable parameters for protections

Symbol	Basic description	Example	Minimum value	Maximum value
$t_{auto,restart}$	Auto-restart time	1.6 s	0.4 s	4.0 s
V_{OCP1}	Regulated mode *CS* pin voltage level 1 for MOSFET max. current cycle by cycle limit	0.5 V	Refer GUI	1.08 V
$Reaction_{OVP,Vout}$	Output overvoltage protection reaction	Auto-restart	Auto-restart	Latch-Mode
V_{outOV}	Output overvoltage protection level	56.9 V	$V_{out,dim,min}$	Refer GUI

(table continues...)

Table 7 (continued) Configurable parameters for protections

Symbol	Basic description	Example	Minimum value	Maximum value
$t_{VoutOV,blank,ABM}$	Output overvoltage protection blanking time in ***ABM***	0.5 ms	0.2 ms	5.0 ms
$EN_{adaptive,OVP,Vout}$	Enable switch for adaptive output overvoltage protection level	Enabled	Enabled	Disabled
$V_{outOV,red}$	Output overvoltage protection level applied during auto-restart when the last triggered protection is output overvoltage protection with $EN_{adaptive,OVP,Vout}$ enabled.	51.3 V	$V_{out,dim,min}$	V_{outOV}
$I_{out,OVP,red}$	Output current set point max. limit applied during auto-restart when the last triggered protection is output overvoltage protection with $EN_{adaptive,OVP,Vout}$ enabled.	41.5 mA	$I_{out,min}$	$I_{out,full}$
$N_{Vout,\ restore}$	Blanking time for output voltage below $V_{outOV,red}$ to exit output overvoltage protection with $EN_{adaptive,OVP,Vout}$ enabled.	500	0	5000
$t_{VoutUV,blank}$	Blanking time for regulated mode output undervoltage protection	40 ms	40 ms	1000 ms
$EN_{Iout,max,peak}$	Enable switch for peak output overcurrent protection	Enabled	Enabled	Disabled
$I_{out,max,peak}$	Peak output overcurrent protection level	2100 mA	Refer GUI	Refer GUI
$t_{Iout,max,peak,blank}$	Blanking time for peak output overcurrent protection	1 ms	0 ms	5 ms
$Speed_{OCP,Iout}$	Auto-restart speed for peak output overcurrent protection	Fast	Slow	Fast
$EN_{OVP,In}$	Enable switch for maximum input voltage startup check and input overvoltage protection	Enabled	Enabled	Disabled
$EN_{UVP,In}$	Enable switch for minimum input voltage startup check and input undervoltage protection	Enabled	Enabled	Disabled
V_{inOV}	Input overvoltage protection level (rms in case of AC input)	352 V_{rms}	$V_{in,start,max}$	Refer GUI
$V_{in,start,max}$	Maximum input voltage level at startup (rms in case of AC input)	326 V_{rms}	$V_{in,start,min}$	V_{inOV}
$V_{in,start,min}$	Minimum input voltage level at startup (rms in case of AC input)	80 V_{rms}	V_{inUV}	Refer GUI
V_{inUV}	Input undervoltage protection level (rms in case of AC input)	63 V_{rms}	Refer GUI	$V_{in,start,min}$
$T_{critical}$	Temperature threshold for IC overtemperature protection	119°C	Refer GUI	143°C
$Debug_{Mode}$	Enable switch for debug mode	Disabled	Enabled	Disabled

List of Parameters

Table 8 Configurable parameters for multimode

Symbol	Basic description	Example	Minimum value	Maximum value
$f_{sw,max}$	Maximum switching frequency for ***QRM1*** and ***DCM***	70 kHz	20 kHz	Refer GUI
$N_{DCM,mod,gain}$	Switching period modulation attenuation	16	0 (disabled), 4, 8, 16, 32	
$t_{on,min}$	Minimum on-time $t_{on,min}(V_{in})$ value when $t_{on,min,V,out,sense}(V_{in})$ is lower than $t_{on,min}$	2 µs	Refer GUI	$t_{on,max}$
$t_{min,demag}$	Minimum transformer demagnetizing time value used for $t_{on,min,V,out,sense}(V_{in})$ variable calculation internally	3 µs	3 µs	Refer GUI
$t_{on,max}$	Maximum on-time	11.5 µs	Refer GUI	30 µs
$f_{sw,min,DCM}$	Minimum switching frequency in DCM	20 kHz	Refer GUI	20 kHz
EN_{ABM}	Enable switch for ABM	Enabled	Enabled	Disabled
$N_{ABM,min}$	Minimum number of pulses per burst	11	4	Refer GUI
$N_{ABM,init,VinUV}$	Initial number of pulses per burst when EN_{ABM} is enabled and V_{in} is near to input undervoltage protection level V_{inUV}	132	$N_{ABM,min}$	Refer GUI
$V_{in,high}$	Input voltage level which when exceeded, the initial number of pulses per burst is fixed as $N_{ABM,min}$ if EN_{ABM} is enabled	277 V_{rms}	$V_{in,start,min}$	V_{inOV}

Table 9 Configurable parameters for control loop response

Symbol	Basic description	Example	Minimum value	Maximum value
$K_{P,QRM}$	Proportional gain of control loop in QRM1	512	10	3000
$K_{I,QRM}$	Integral gain of control loop in QRM1	32	1	1000
$K_{P,DCM}$	Proportional gain of control loop in DCM	2048	100	30000
$K_{I,DCM}$	Integral gain of control loop in DCM	512	10	10000
$K_{P,ABM}$	Proportional gain of control loop in ABM	128	1	600
$K_{I,ABM}$	Integral gain of control loop in ABM	32	1	200
$ABM_{thrs,multiplier}$	Minimum set-point error threshold multiplier to activate control loop response in ABM	3	0	10

Table 10 Parameters for power factor correction

Symbol	Basic description	Example	Minimum value	Maximum value
C_{EMI}	Input current displacement compensation gain parameter for enhanced PFC	0.1 µF	0 µF	1 µF

Table 11 Configurable parameters for fine tuning

Symbol	Basic description	Example	Minimum value	Maximum value
$t_{ZCD,PD}$	*ZCD* pin propagation delay compensation parameter	270 ns	0 ns	1000 ns

(table continues...)

List of Parameters

Table 11 (continued) Configurable parameters for fine tuning

Symbol	Basic description	Example	Minimum value	Maximum value
t_{zcddel}	Rising edge delay of *ZCD* signal after gated turn off	380 ns	0 ns	1000 ns
t_{PDC}	*CS* pin propagation delay compensation parameter	200 ns	0 ns	1000 ns
$K_{coupling}$	Transformer coupling coefficient parameter	0.96	0	2
$G_{out,loss}$	Auxiliary loss compensation parameter	11.9 Ω	0 mS	2 mS
R_{in}	DC link filter capacitor voltage ripple compensation parameter to improve input voltage estimation accuracy	11.0 Ω	0 Ω	30 Ω

Table 12 Configurable parameter for user ID

Symbol	Basic description	Example	Minimum value	Maximum value
$User_{ID,A}$	User ID A	1018	0	65535

List of fixed parameters

Table 13 Fixed parameters for hardware configuration

Symbol	Basic description	Default	Minimum value	Maximum value
$L_{p,lk}$	Transformer primary leakage inductance	1% of L_p	-	-
V_d	Secondary main output diode forward voltage assumption for output voltage estimation	0.7 V	-	-
V_{GD}	*GD* pin peak voltage	12 V	-	-

Table 14 Fixed parameter for startup

Symbol	Basic description	Default	Minimum value	Maximum value
t_{ss}	Soft start time step	0.5 ms or $3.2/t_{ss}$, whichever is lower	-	-

Table 15 Fixed parameters for protections

Symbol	Basic description	Default	Minimum value	Maximum value
V_{outUV}	Regulated mode output undervoltage protection level	$V_{out,dim,min}$ / 2	-	-
$V_{VCC,max}$	*VCC* overvoltage protection level	24 V	-	-
$T_{start,max}$	Maximum IC junction temperature for startup	$T_{critical}$-4°C	-	-
$t_{blank,Vin,OV}$	Blanking time for input overvoltage threshold	$1/(2f_{line})$	-	-
$t_{blank,Vin,UV}$	Blanking time for input undervoltage threshold	$10/(2f_{line})$	-	-

Table 16 Fixed parameters for multimode

Symbol	Basic description	Default	Minimum value	Maximum value
$f_{sw,min,QRM}$	Minimum switching frequency in QRM1	20 kHz	-	-
$f_{DCM,init,VinUV}$	Initial DCM switching frequency when EN_{ABM} is disabled and V_{in} is near to input undervoltage protection level V_{inUV}	20 kHz	-	-

Table 17 Other fixed parameters

Symbol	Basic description	Default	Minimum value	Maximum value
$t_{CS,LEB}$	*CS* leading edge blanking time	480 ns	-	-
t_{CSOCP2}	MOSFET overcurrent protection blanking time	240 ns	-	-
$t_{ZCD,ring}$	*ZCD* ringing suppression	1200 ns	-	-
$t_{blank,CCM}$	Blanking time for protection	10 ms	-	-
t_{pw}	Discharge pulse duration	1.5 µs	-	-

6 Electrical Characteristics and Parameters

All signals are measured with respect to the ground pin, GND. The voltage levels are valid provided other ratings are not violated.

6.1 Package Characteristics

Table 18 Package Characteristics

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Thermal resistance for PG-DSO-8-58	R_{thJA}	—	178	K/W	JEDEC 1s0p for 140 mW power dissipation

6.2 Absolute Maximum Ratings

Attention: ***Stresses above the values listed below may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.***

Table 19 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Voltage externally supplied to pin VCC	V_{VCCEXT}	–0.5	26	V	voltage that can be applied to pin VCC by an external voltage source
Voltage at pin GDx	V_{GDx}	–0.5	V_{VCC} + 0.3	V	if gate driver is not configured for digital I/O
Junction temperature	T_J	–40	125	°C	max. operating frequency 66 MHz f_{MCLK}
Junction temperature	T_J	–40	150[1]	°C	$f_{sw,max} \leq 136$ kHz
Storage temperature	T_S	–55	150	°C	
Soldering temperature	T_{SOLD}	—	260	°C	Wave Soldering [2]
Latch-up capability	I_{LU}	—	150	mA	[3] Pin voltages acc. to abs. max. ratings
ESD capability HBM	V_{HBM}	—	1500	V	[4][5]
ESD capability CDM	V_{CDM}	—	500	V	[6]

(table continues...)

1 Auto-restart may be delayed at low input voltage condition when junction temperature is above 125°C. The lifetime is not guaranteed when IC operating junction temperature is above 125°C.
2 According to JESD22-A111 Rev A.
3 Latch-up capability according to JEDEC JESD78D, T_A= 85°C.
4 ESD-HBM according to ANSI/ESDA/JEDEC JS-001-2012.
5 product resp. package specific rating up to 2000 V
6 ESD-CDM according to JESD22-C101F.

Table 19 (continued) Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Input Voltage Limit	V_{IN}	–0.5	3.6	V	Voltage externally supplied to pins GPIO, MFIO, CS, ZCD, GPIO, VS, GDx (if GDx is configured as digital I/O). (If not stated different)
Maximum permanent negative clamping current for ZCD and CS	$-I_{CLN\_DC}$	—	2.5	mA	RMS
Maximum transient negative clamping current for ZCD and CS	$-I_{CLN\_TR}$	—	10	mA	pulse < 500ns
Maximum negative transient input voltage for ZCD	$-V_{IN\_ZCD}$	—	1.5	V	pulse < 500ns
Maximum negative transient input voltage for CS	$-V_{IN\_CS}$	—	3.0	V	pulse < 500ns
Maximum permanent positive clamping current for CS	I_{CLP_DC}	—	2.5	mA	RMS
Maximum transient positive clamping current for CS	I_{CLP_TR}	—	10	mA	pulse < 500ns
Maximum current into pin VIN	I_{AC}	—	10	mA	for charging operation
Maximum sum of input clamping high currents for digital input stages of device	I_{CLH_sum}	—	300	µA	limits for each individual digital input stage have to be respected
Voltage at HV pin	V_{HV}	-0.5	600	V	

6.3 Operating conditions

The recommended operating conditions are shown for which the DC Electrical Characteristics are valid.

Table 20 Operating range

Parameter	Symbol	Limit Values		Unit	Remarks
		min	max		
Ambient temperature	T_A	–40	85	°C	
Junction Temperature	T_J	–40	125	°C	max. 66 MHz f_{MCLK}
Lower VCC limit	V_{VCC}	V_{UVOFF}	—	V	device is held in reset when $V_{VCC} < V_{UVOFF}$
Voltage externally supplied to VCC pin	V_{VCCEXT}	—	24	V	maximum voltage that can be applied to pin VCC by an external voltage source
Gate driver pin voltage	V_{GD}	–0.5	V_{VCC} + 0.3	V	
Line frequency	f_{line}	45	66	Hz	

6.4 DC Electrical characteristics

The electrical characteristics provide the spread of values applicable within the specified supply voltage and junction temperature range, T_J from -40 °C to +125 °C.

Devices are tested in production at T_A = 25 °C. Values have been verified either with simulation models or by device characterization up to 125 °C.

Typical values represent the median values related to T_A = 25 °C. All voltages refer to GND, and the assumed supply voltage is V_{VCC} = 18 V if not otherwise specified.

Note: Not all values given in the tables are tested during production testing. Values not tested are explicitly marked.

Table 21 Power supply characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VCC_ON threshold	V_{VCCon}	—	V_{SELF}	—	V	Self-powered startup (default)
VCC_ON_SELF threshold	V_{SELF}	19	20.5	22	V	dV_{VCC}/dt = 0.2 V/ms
VCC_ON_SELF delay	t_{SELF}	—	—	2.1	µs	Reaction time of V_{VCC} monitor
VCC_UVOFF current	$I_{VCCUVOFF}$	5	20	40	µA	$V_{VCC} < V_{SELF}$(min) - 0.3 V or $V_{VCC} < V_{EXT}$(min) - 0.3 V[7)]
UVOFF threshold	V_{UVOFF}	—	6.0	—	V	SYS_CFG0.SELUVTHR = 0_B
UVOFF threshold tolerance	Δ_{UVOFF}	—	—	±5	%	This value defines the tolerance of V_{UVOFF}
UVOFF filter constant	t_{UVOFF}	600	—	—	ns	1V overdrive
UVLO (UVWAKE) threshold	V_{UVLO}	—	V_{UVOFF} · 1.25	—	V	
UVWAKE threshold tolerance	Δ_{UVLO}	—	—	±5	%	This value defines the tolerance of V_{UVLO}
UVLO (UVWAKE) filter constant	t_{UVLO}	0.6	—	2.2	µs	1 V overdrive
OVLO (OVWAKE) threshold	V_{OVLO}	—	V_{SELF}	—	V	
OVLO (OVWAKE) filter constant	t_{OVLO}	0.6	—	2.4	µs	1 V overdrive
VDDP voltage	V_{VDDP}	3.04	3.20	3.36	V	At PMD0/PSMD1. Some internal values refer to V_{VDDP} / V_{VDDA} and V_{VDDPPS} / V_{VDDAPS} respectively.

(table continues...)

7 Tested at V_{VCC} = 5.5 V

Table 21 (continued) Power supply characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
VDDA voltage	V_{VDDA}	3.20	3.31	3.42	V	At PMD0/PSMD1. Some internal values refer to V_{VDDP} / V_{VDDA} and V_{VDDPPS} / V_{VDDAPS} respectively.
Nominal range 0% to 100%	V_{ADCVCC}	0	—	V_{REF}	V	$V_{ADCVCC} = 0.09 \cdot V_{VCC}$ [8]
Reduced VCC range for ADC measurement	R_{ADCVCC}	8	—	92	%	[9][10]
Maximum error for ADC measurement (8-bit result)	$TET0_{VCC}$	—	—	3.8	LSB_8	
Maximum error for ADC measurement (8-bit result)	$TET256_{VCC}$	—	—	5.2	LSB_8	
Gate driver current consumption excl. gate charge current	I_{VCCGD}	—	0.26	0.35	mA	$T_j \leq 125°C$
VCC quiescent current in PMD0	$I_{VCCPMD0}$	—	3.5	4.7	mA	All registers have reset values, clock is active, CPU is stopped
VCC quiescent current in PSMD2	$I_{VCCPSMD2}$	—	0.3	0.48	mA	$T_j \leq 85$ °CWU_PWD_CFG = $2C_H$
VCC quiescent current in PSMD2	$I_{VCCPSMD2}$	—	—	1.2	mA	$T_j \leq 125$ °CWU_PWD_CFG = $2C_H$
VCC quiescent current in power saving mode PSDM4 with standby logic active	$I_{VCCPSMD4}$	—	0.13	0.18	mA	$T_j \leq 125$ °C WU_PWD_CFG = 00_H

Table 22 Electrical characteristics of the GD pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	µA	only digital input
Input clamping current, high	I_{CLH}	—	—	100	µA	only digital input

(table continues...)

8 Theoretical minimum value, real minimum value is related to V_{UVOFF} threshold.
9 Operational values.
10 Note that the system is turned off if $V_{VCC} < V_{UFOFF}$.

Table 22 (continued) Electrical characteristics of the GD pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
APD low voltage (active pull-down while device is not powered or gate driver is not enabled)	V_{APD}	—	—	1.6	V	I_{GD} = 5 mA
R_{PPD} value	R_{PPD}	—	600	—	kΩ	Permanent pull-down resistor inside gate driver
R_{PPD} tolerance	Δ_{PPD}	—	—	±25	%	Permanent pull-down resistor inside gate driver
Driver output low impedance	R_{GDL}	—	—	7.0	Ω	$T_J \leq 125$ °C, I_{GD} = 0.1 A
Nominal output high voltage in PWM mode	V_{GDH}	—	12	—	V	GDx_CFG.VOL = 2, I_{GDH} = –1 mA
Output voltage tolerance	Δ_{VGDH}	—	—	±5	%	Tolerance of programming options if V_{GDH} > 10 V, I_{GDH} = –1 mA
Rail-to-rail output high voltage	V_{GDHRR}	V_{VCC}– 0.5	—	V_{VCC}	V	If V_{VCC} < programmed V_{GDH} and output at high state
Output high current in PWM mode for GD0	$-I_{GDH}$	—	100	—	mA	GDx_CFG.CUR = 8
Output high current tolerance in PWM mode	Δ_{IGDH}	—		±15	%	Calibrated [11]
Discharge current for GD0	I_{GDDIS}	800	—	—	mA	V_{GD} = 4 V and driver at low state
Output low reverse current	$-I_{GDREVL}$	—	—	100	mA	Applies if V_{GD} < 0 V and driver at low state
Output high reverse current in PWM mode	I_{GDREVH}	—	1/6 of I_{GDH}	—		Applies if V_{GD} > V_{GDH} + 0.5 V (typ) and driver at high state

Table 23 Electrical characteristics of the CS pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.0	V	

(table continues...)

11 referred to GDx_CFG.CUR = 16

Table 23 (continued) Electrical characteristics of the CS pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	1.6	—	V	SYS_CFG0.OCP2 = 00_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	1.2	—	V	SYS_CFG0.OCP2 = 01_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	0.8	—	V	SYS_CFG0.OCP2 = 10_B
OCP2 comparator reference voltage, derived from V_{VDDA}, given values assuming $V_{VDDA} = V_{VDDA,typ}$	V_{OCP2}	—	0.6	—	V	SYS_CFG0.OCP2 = 11_B
Threshold voltage tolerance	Δ_{VOCP2}	—	—	±5	%	Voltage divider tolerance
Comparator propagation delay	t_{OCP2PD}	15	—	35	ns	
Minimum comparator input pulse width	t_{OCP2PW}	—	—	30	ns	
OCP2F comparator propagation delay	$t_{OCP2FPD}$	70	—	170	ns	dV_{CS}/dt = 100 V/µs
Delay from V_{CS} crossing V_{CSOCP2} to begin of GDx turn-off (I_{GD0} > 2mA)	$t_{CSGDxOCP2}$	125	135	190	ns	dV_{CS}/dt = 100 V/µs; f_{MCLK} = 66 MHz. GDx driven by QR_GATE FIL_OCP2.STABLE = 3
OCP1 operating range	V_{OCP1}	0	—	$V_{REF}/2$	V	RANGE =00_B
OCP1 threshold at full scale setting (CS_OCP1LVL=FF_H)	V_{OCP1FS}	1187	1209	1243	mV	RANGE =00_B
Delay from V_{CS} crossing V_{CSOCP1} to CS_OCP1 rising edge, 1.2 V range	t_{CSOCP1}	90	170	250	ns	Input signal slope dV_{CS}/dt = 150 mV/µs. This slope represents a use case of a switch-mode power supply with minimum input voltage.

(table continues...)

Table 23 (continued) Electrical characteristics of the CS pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Delay from CS_OCP1 rising edge to QR_GATE falling edge	$t_{OCP1GATE}$	—	—	130	ns	
Delay from QR_GATE falling edge to start of GDx turn-off	$t_{GATEGDx}$	1	3	5	ns	GDx driven by QR_GATE. Measured up to I_{GDx} > 2 mA
OCP1 comparator input single pulse width filter	t_{OCP1PW}	60	—	95	ns	Shorter pulses than min. are suppressed, longer pulses than max. are passed
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/2$	V	CS_ICR.RANGE =00_B
Reduced S&H operating range	RR_{CVSH}	8	—	92	%	CS_ICR.RANGE =00_B Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	4.7	LSB	CS_ICR.RANGE =00_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	6.0	LSB	CS_ICR.RANGE =00_B
Nominal S&H operating range 0% to 100%	V_{CSH}	0	—	$V_{REF}/6$	V	CS_ICR.RANGE =11_B
Reduced S&H operating range	RR_{CVSH}	20	—	80	%	CS_ICR.RANGE =11_B Operational values
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET0_{CS0S}$	—	—	8.0	LSB	CS_ICR.RANGE =11_B
Maximum error of CS0 S&H for corrected measurement (8-bit result)	$TET256_{CS0S}$	—	—	8.7	LSB	CS_ICR.RANGE =11_B
S&H delay of input buffer	t_{CSHST}	—	—	510	ns	Referring to jump in input voltage. Limits the minimum gate driver T_{on} time.

Table 24 Electrical characteristics of the ZCD pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input voltage operating range	V_{INP}	–0.5	—	3.3	V	
Input clamping current, high	I_{CLH}	—	—	100	µA	
Zero-crossing threshold	V_{ZCTHR}	15	40	70	mV	
Comparator propagation delay	t_{ZCPD}	30	50	70	ns	dV_{ZCD}/dt = 4 V/µs
Input voltage negative clamping level	$-V_{INPCLN}$	140	180	220	mV	Analog clamp activated
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	0.5	mA	CRNG =11_BGain = 4800 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	1	mA	CRNG =10_BGain = 2400 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	2	mA	CRNG =01_BGain = 1200 mV/mA
Nominal I/V-conversion operating range 0% to 100%	$-I_{IV}$	0	—	4	mA	CRNG =00_B Gain = 600 mV/mA
Reduced I/V-conversion operating range	RR_{IV}	5	—	80	%	
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{IV}$	—	—	4.1	LSB_8	CRNG =00_B
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{IV}$	—	—	9.7	LSB_8	CRNG =00_B
Maximum deviation between ZCD clamp voltage and trim result stored in OTP	E_{ZCDClp}	—	—	±5	%	$-I_{IV}$ > 0.25 mA
IV-conversion delay of input buffer	t_{IVST}	—	—	900	ns	Refers to jump in input current[12)]

(table continues...)

12 Limits the minimum gate driver T_{on} time.

Table 24 (continued) Electrical characteristics of the ZCD pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	0	—	$2/3 \cdot V_{REF}$	V	SHRNG $=0_B$
Nominal S&H input voltage range 0% to 100%	V_{ZSH}	$V_{REF}/2$	—	$7/6 \cdot V_{REF}$	V	SHRNG $=1_B$
Reduced S&H input voltage range	RR_{ZVSH}	4	—	95	%	
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS0}$	—	—	3.7	LSB_8	SHRNG $=0_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS0}$	—	—	4.9	LSB_8	SHRNG $=0_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET0_{ZVS1}$	—	—	4.2	LSB_8	SHRNG $=1_B$
Maximum error for corrected ADC measurement (8-bit result)	$TET256_{ZVS1}$	—	—	5.8	LSB_8	SHRNG $=1_B$
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.0	µs	SHRNG $=0_B T_j \le 125$ °C
S&H delay of input buffer referring to jump of input voltage	t_{ZSHST}	—	—	1.6	µs	SHRNG $=1_B T_j \le 125$ °C

Table 25 Electrical characteristics of the HV pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Current for V_{CC} cap charging	I_{LD}	3.0	5	7.5	mA	$V_{HV} = 30$ V; $V_{VCC} < V_{VCCon} - 0.3$ V; $T_j \ge 0$°C
Current for V_{CC} cap charging	I_{LD}	2.4	5	7.5	mA	$V_{HV} = 30$ V; $V_{VCC} < V_{VCCon} - 0.3$ V;-25°C < T_j < 0°C
Current for V_{CC} cap charging	I_{LD}	2.0	5	7.5	mA	$V_{HV} = 30$ V; $V_{VCC} < V_{VCCon} - 0.3$ V;T_j < -25°C

(table continues...)

Table 25 (continued) Electrical characteristics of the HV pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	9.6	mA	CURRNG = 11_B
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	4.8	mA	CURRNG = 10_B
Nominal current for measurement path 0% to 100%	I_{MEAS}	0	—	1.6	mA	CURRNG = 01_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	15	20	25	%	COMPTHR= 00_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	25	30	35	%	COMPTHR= 01_B
Comparator threshold (in % of full range of I_{MEAS})	THR_{COMP}	45	50	55	%	COMPTHR= 11_B

Table 26 Electrical characteristics of the PWM pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
MFIO reference voltage	$V_{MFIOREF}$	—	V_{VDDP}	—	V	Selection = V_{VDDP}, not power down
Input low voltage	V_{IL}	—	—	1.0	V	
Input high voltage	V_{IH}	2.0	—	—	V	
Pull-up resistor tolerance	Δ_{RPU}	—	—	±20	%	Overall tolerance
PWM frequency	f_{PWM}	500	—	2000	Hz	

Table 27 Electrical characteristics of the UART pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Input clamping current, low	$-I_{CLL}$	—	—	100	µA	only digital input
Input clamping current, high	I_{CLH}	—	—	100	µA	only digital input
Input capacitance	C_{INPUT}	—	—	25	pF	
Input low voltage	V_{IL}	—	—	1.0	V	
Input high voltage	V_{IH}	2.1	—	—	V	
Input low current with active weak pull-up WPU	$-I_{LPU}$	30	—	90	µA	Measured at max. V_{IL}

(table continues...)

Table 27 (continued) Electrical characteristics of the UART pin

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Max. input frequency	f_{INPUT}	15	—	—	MHz	
Output low voltage	V_{OL}	—	—	0.8	V	I_{OL} = 2 mA
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = –2 mA
Output sink current	I_{OL}	—	—	2	mA	
Output source current	$-I_{OH}$	—	—	2	mA	
Output rise time (0 → 1)	t_{RISE}	—	—	50	ns	20 pF load, push/pull output
Output fall time (1 → 0)	t_{FALL}	—	—	50	ns	20 pF load, push/pull or open-drain output
Max. output switching frequency	f_{SWITCH}	10	—	—	MHz	
UART baudrate	f_{UART}	-10%	57600	+10%	baud	

Table 28 Electrical characteristics of the A/D converter

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Integral non-linearity	INL	—	—	1	LSB_8	*13)*

Table 29 Electrical characteristics of the reference voltage

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Reference voltage	V_{REF}	—	2.428	—	V	
VREF overall tolerance	Δ_{VREF}	—	—	±1.5	%	Trimmed, $T_j \leq 125$ °C and aging

Table 30 Electrical characteristics of the OTP programming

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
OTP programming voltage at the VCC pin for range $C000_H$ to $CFFF_H$	V_{PP}	7.35	7.5	7.65	V	Operational values
OTP programming current	I_{PP}	—	1.6	—	mA	Programming of 4 bits in parallel

13 ADC capability measured via channel MFIO without errors due to switching of neighbouring pins, e.g. gate drivers, measured with STC = 5. MFIO buffer non-linearity masked out by taking ADC output values ≥ 30 only.

Table 31 Electrical characteristics of the clock oscillators

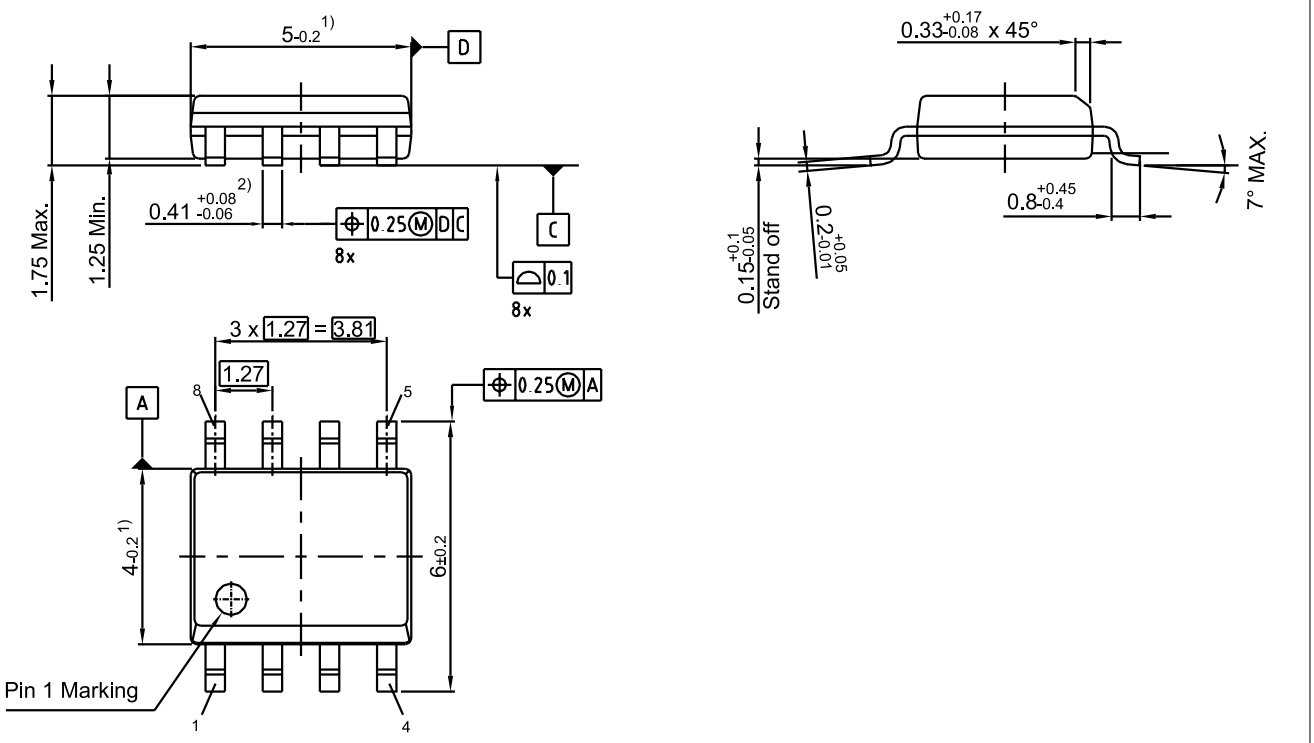
Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Master clock oscillation period including all variations	t_{MCLK}	15.0	15.8	16.6	ns	In reference to 66 MHz f_{MCLK}
Main clock oscillator frequency variation of stored DPARAM frequency	Δ_{MCLK}	–3.2	—	+3.5	%	Temperature drift and aging only, 66 MHz f_{MCLK}
Standby clock oscillator frequency	f_{STBCLK}	96	100	104	kHz	Trimming tolerance at T_A = 25 °C
Standby clock oscillator frequency	f_{STBCLK}	90	100	110	kHz	Overall tolerance, $T_j \leq$ 125 °C

Table 32 Electrical characteristics of the temperature sensor

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Temperature sensor ADC output operating range	ADC_{TEMP}	0	—	190	LSB	ADC_{TEMP} = 40 + temperature / °C)
Temperature sensor tolerance	Δ_{TEMP}	—	—	±6	K	Incl. ADC conversion accuracy at 3 σ

7 Package dimensions

The package dimensions of PG-DSO-8 are provided.



1) Does not include plastic or metal protrusion
2) Does not include dambar protrusion of 0.127 Max. in excess of the lead width dimension
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [ ]

Figure 25 Package dimensions for PG-DSO-8

Package dimensions

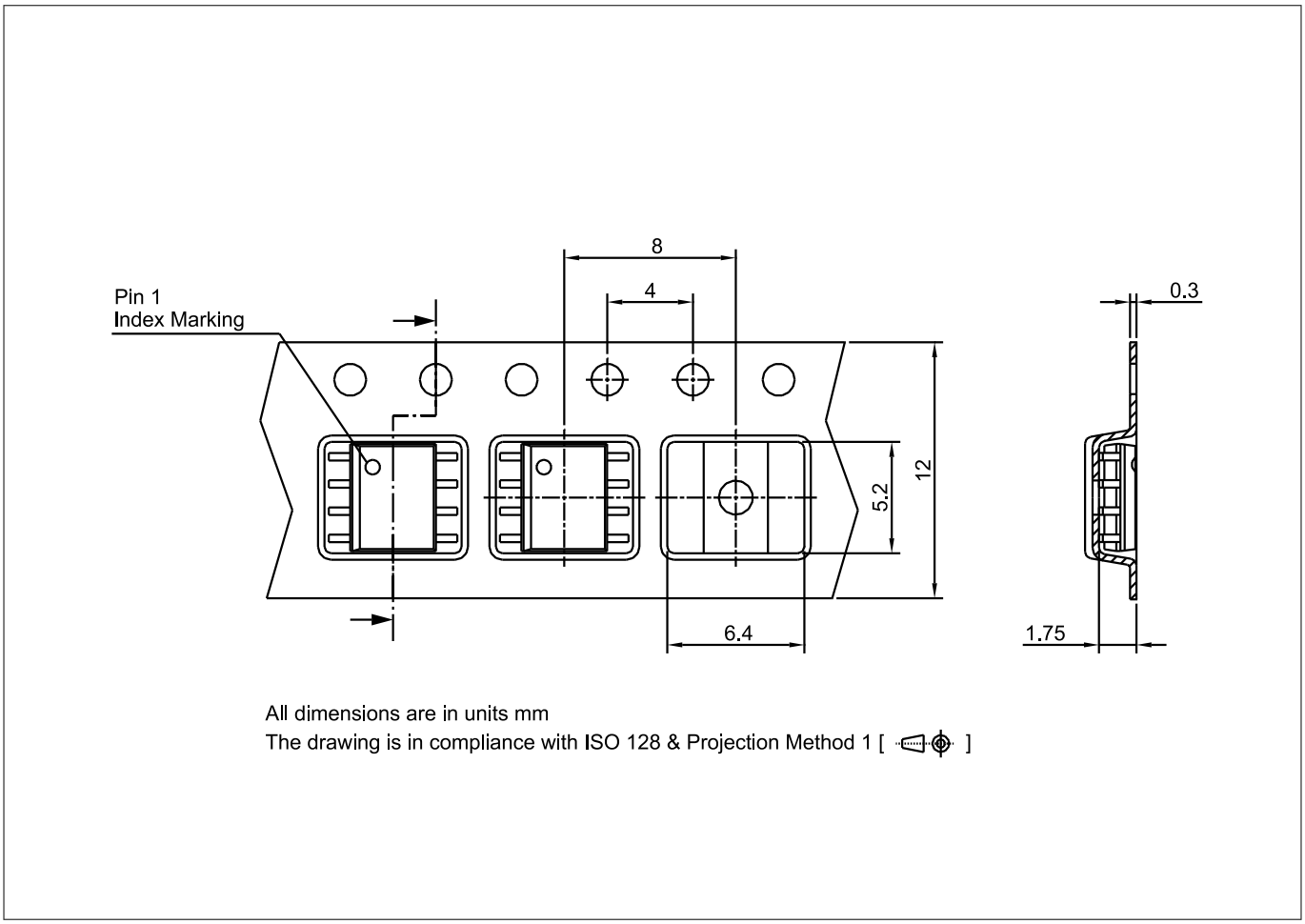


Figure 26 Tape and reel for PG-DSO-8

Note: You can find all of our packages, packing types and other package information on our Infineon Internet page “Products”: http://www.infineon.com/products.

8 References

1. Infineon Technologies AG: *XDPL8210 Design Guide*
2. Infineon Technologies AG: *XDPL8210 CDM10VD 35 W reference design with IPN80R900P7*
3. Infineon Technologies AG: *CoolMOS P7 power MOSFETs*, ***http://www.infineon.com/P7***
4. Infineon Technologies AG: *.dp Vision User Manual*
5. Infineon Technologies AG: *.dp Interface Gen2* which can be ordered at ***https://www.infineon.com/cms/en/product/evaluation-boards/if-board.dp-gen2/***
6. Infineon Technologies AG: *.dp Interface Gen2 User Manual*
7. Infineon Technologies AG: *XDP Programming Manual*

Revision History

Major changes since previous revision

Revision History

Revision	Description
1.1	• Remove DC input related text • Update .dp Interface Gen2 ordering link • Remove $D_{DIM,max}$ from list of fixed parameters • Add $D_{DIM,max}$, $f_{PWM,max}$ and $f_{PWM,min}$ to list of configurable parameters • Change maximum value of configurable parameter $D_{DIM,min}$ • Change minimum value of configurable parameter $D_{DIM,off}$
1.0	Initial release

Glossary

ABM

Active Burst Mode (ABM)

Active Burst Mode is an operating mode of a switched-mode power supply for very light load conditions. The controller switches in bursts of pulses with a pause between bursts in which no switching is done.

CC

Constant Current (CC)

Constant Current is a mode of a power supply in which the output current is kept constant regardless of the load.

CRC

Cyclic Redundancy Check

A cyclic redundancy check is an error-detecting code commonly used to detect accidental changes to raw data.

DCM

Discontinuous Conduction Mode (DCM)

Discontinuous Conduction Mode is an operational mode of a switching power supply in which the current starts and returns to zero.

Glossary

ECG

Electronic Control Gear (ECG)

An electronic control gear is a power supply which provides one or more light module(s) with the appropriate voltage or current.

EMI

Electro-Magnetic Interference (EMI)

Also called Radio Frequency Interference (RFI), this is a (usually undesirable) disturbance that affects an electrical circuit due to electromagnetic radiation emitted from an external source. The disturbance may interrupt, obstruct, or otherwise degrade or limit the effective performance of the circuit.

FB

Flyback (FB)

A flyback converter is a power converter with the inductor split to form a transformer, so that the voltage ratios are multiplied with an additional advantage of galvanic isolation between the input and any outputs.

GUI

Graphic User Interface

A graphical user interface is a type of interface that allows users to interact with electronic devices through graphical icons and visual indicators.

IC

Integrated Circuit (IC)

A miniaturized electronic circuit that has been manufactured in the surface of a thin substrate of semiconductor material. An IC may also be referred to as micro-circuit, microchip, silicon chip, or chip.

LED

Light Emitting Diode (LED)

A light-emitting diode is a two-lead semiconductor light source which emits light when activated.

LP

Limited Power (LP)

Limited Power is a mode of a power supply in which the output power is limited regardless of the load.

MCU

Microcontroller Unit (MCU)

A microcontroller is a small computer on a single integrated circuit containing a processor core, memory, and programmable input/output peripherals.

PC

Personal Computer

A personal computer is a general-purpose computer whose size, capabilities, and original sale price make it useful for individuals, and which is intended to be operated directly by an end-user with no intervening computer time-sharing models that allowed larger, more expensive minicomputer and mainframe systems to be used by many people, usually at the same time.

PFC

Power Factor Correction (PFC)

Power factor correction increases the power factor of an AC power circuit closer to 1 which corresponds to minimizing the reactive power of the power circuit.

Glossary

PF

Power Factor (PF)

Power factor is the ratio between the real power and the apparent power.

PWM

Pulse Width Modulation (PWM)

Pulse-width modulation is a technique to encode an analog value into the duty cycle of a pulsing signal with arbitrary amplitude.

QRM1

Quasi-Resonant Mode, switching in first valley (QRM1)

Quasi-Resonant Mode is an operating mode of a switched-mode power supply which maximizes efficiency. This is achieved by switching at the occurrence of the first valley of a signal which corresponds to a time when switching losses are low.

THD

Total Harmonic Distortion (THD)

The total harmonic distortion of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.

UART

Universal Asynchronous Receiver Transmitter

A universal asynchronous receiver transmitter is used for serial communications over a peripheral device serial port by translating data between parallel and serial forms.

USB

Universal Serial Bus

Universal Serial Bus is an industry standard that defines cables, connectors and communications protocols used in a bus for connection, communication, and power supply between computers and electronic devices.

UVLO

Undervoltage Lockout (UVLO)

The Undervoltage-Lockout is an electronic circuit used to turn off the power of an electronic device in the event of the voltage dropping below the operational value.

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