

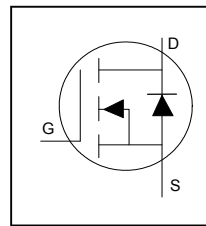
### Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

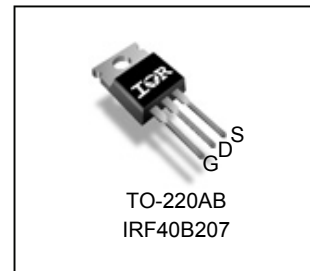
### Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free\*
- RoHS Compliant, Halogen-Free

HEXFET® Power MOSFET



$V_{DSS}$	40V
$R_{DS(on)}$ typ.	3.6mΩ
	max
$I_D$	95A



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRF40B207	TO-220	Tube	50	IRF40B207

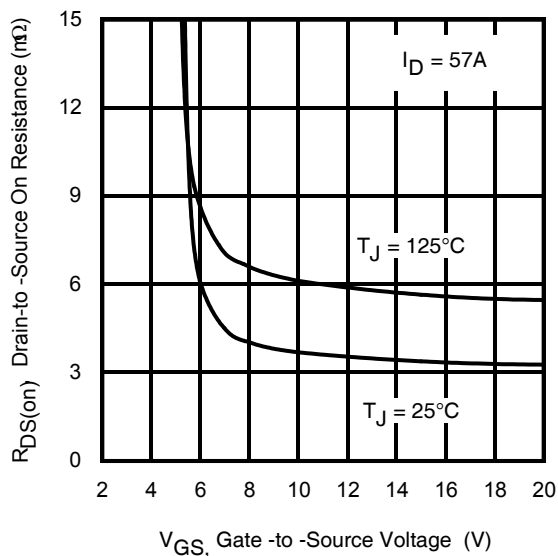


Fig 1. Typical On-Resistance vs. Gate Voltage

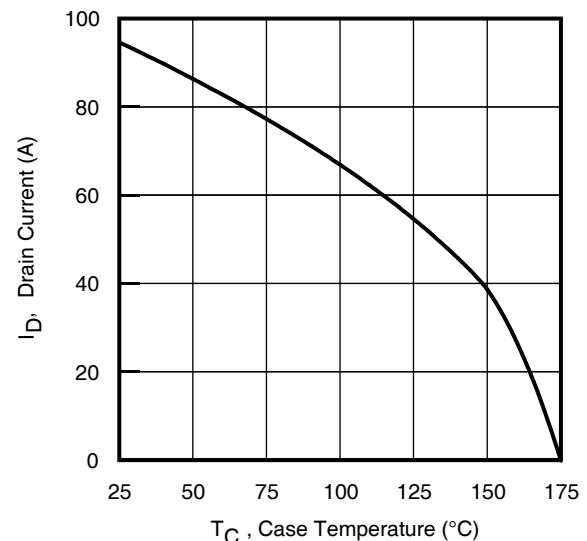


Fig 2. Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	95	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$ (Silicon Limited)	67	
$I_{DM}$	Pulsed Drain Current ①	380	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	83	W
	Linear Derating Factor	0.56	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$	Operating Junction and	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ②	85	mJ
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	167	
$I_{AR}$	Avalanche Current ①	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ①		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑦	—	1.8	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.039	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	3.6	4.5	mΩ	$V_{GS} = 10\text{V}, I_D = 57\text{A}$ ④
		—	5.4	—		$V_{GS} = 6.0\text{V}, I_D = 29\text{A}$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.2	3.0	3.9	V	$V_{DS} = V_{GS}, I_D = 50\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 40\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.0	—	Ω	

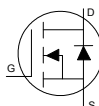
**Notes:**

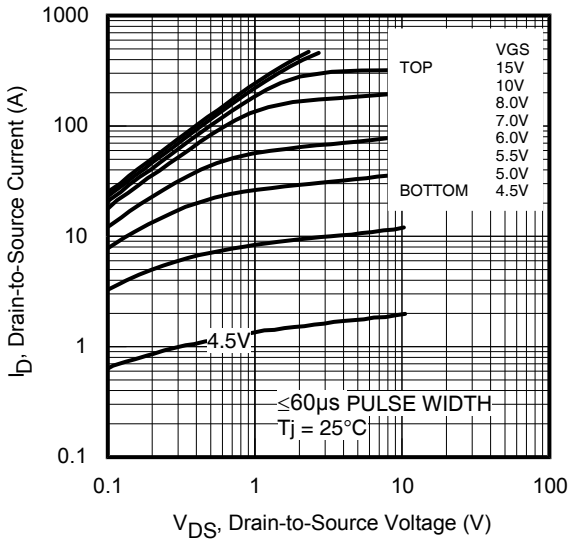
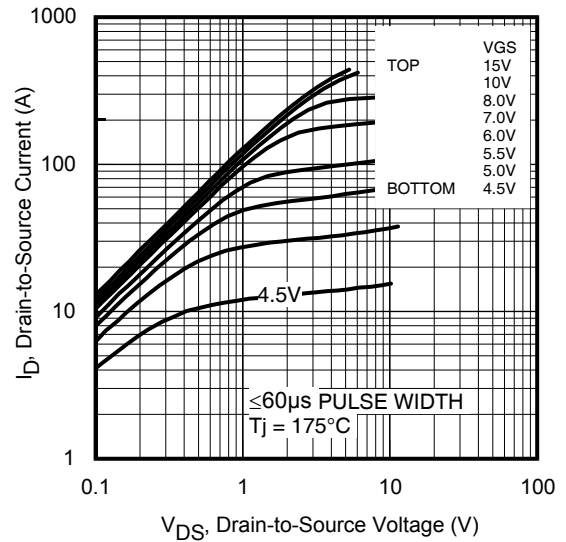
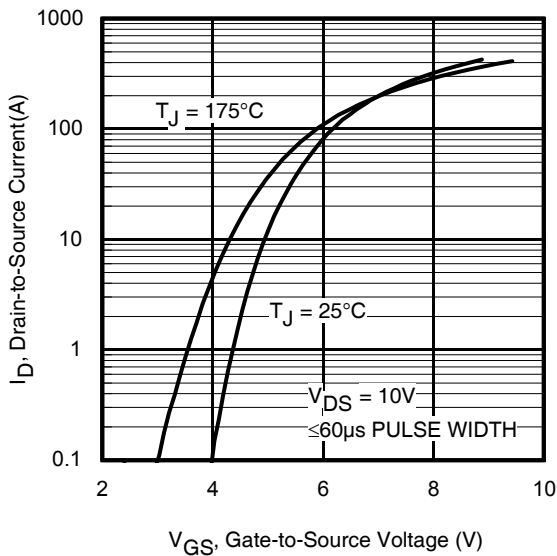
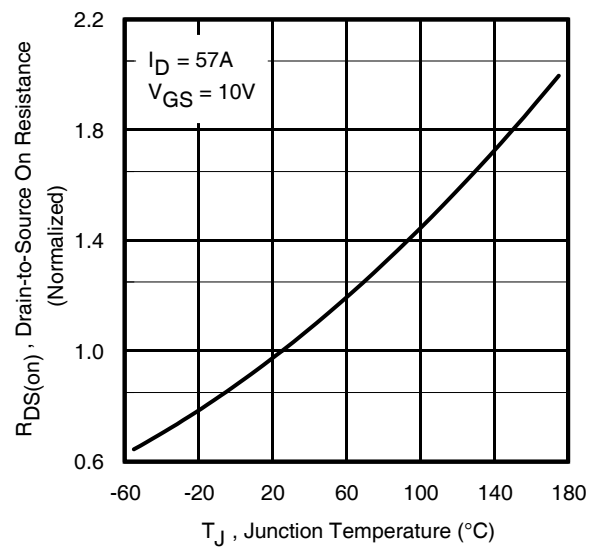
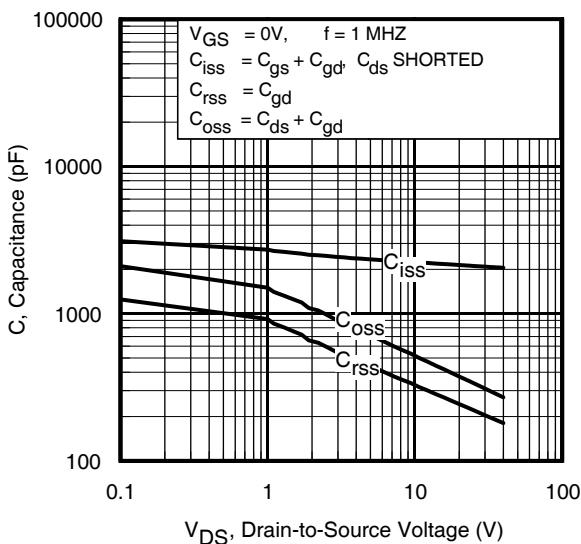
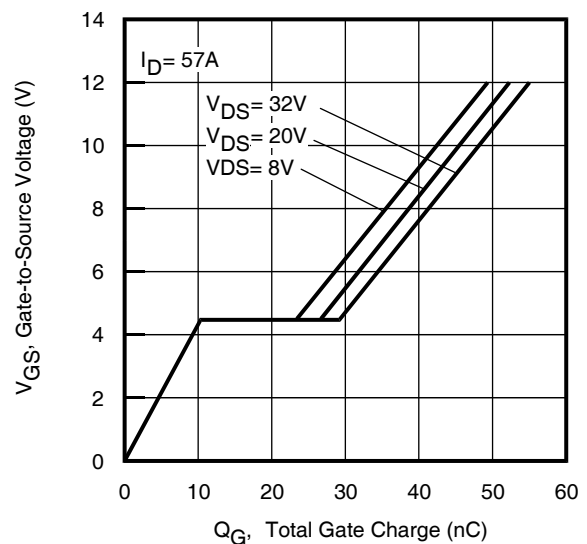
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.052\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 57\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③  $I_{SD} \leq 57\text{A}$ ,  $di/dt \leq 860\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .
- ⑧ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 1\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 18\text{A}$ ,  $V_{GS} = 10\text{V}$ .

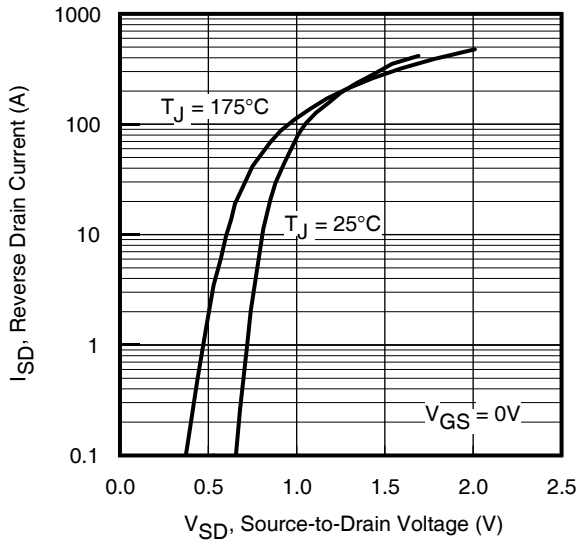
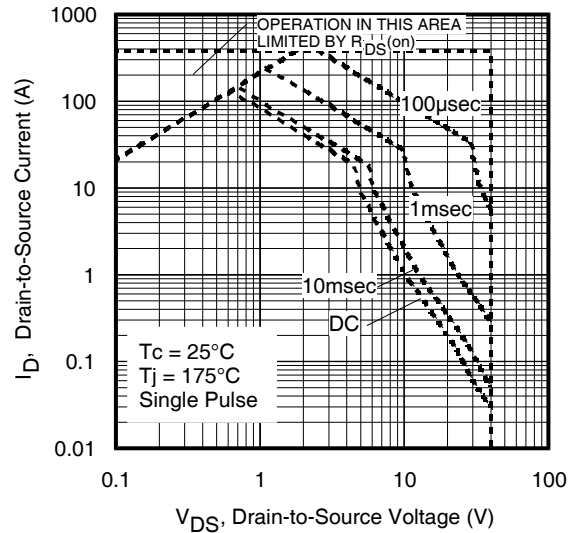
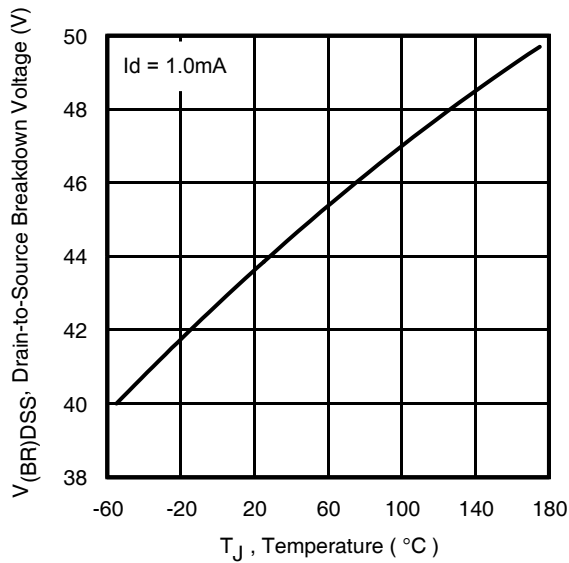
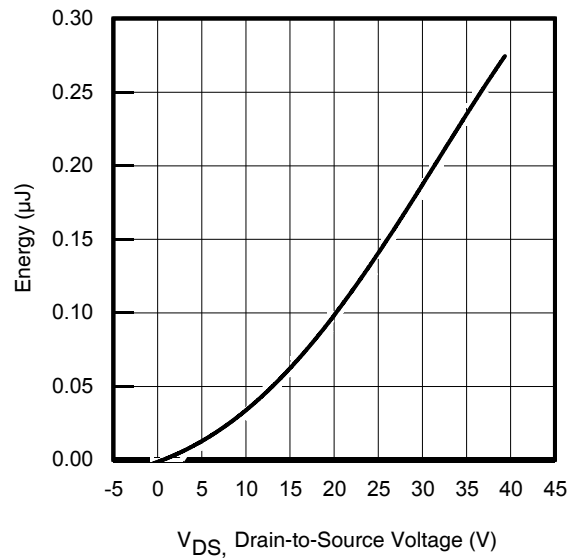
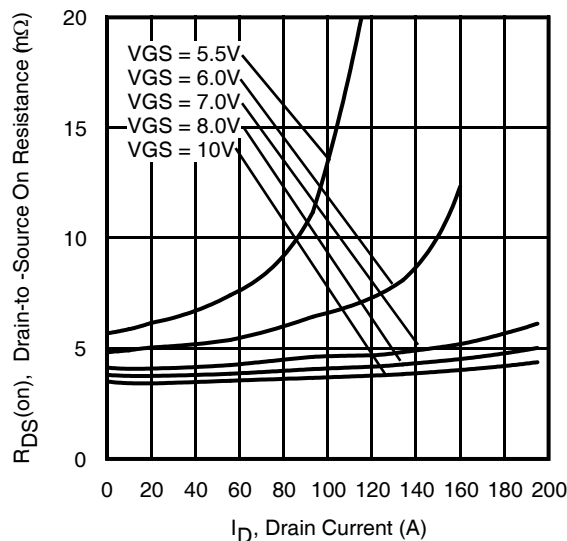
**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

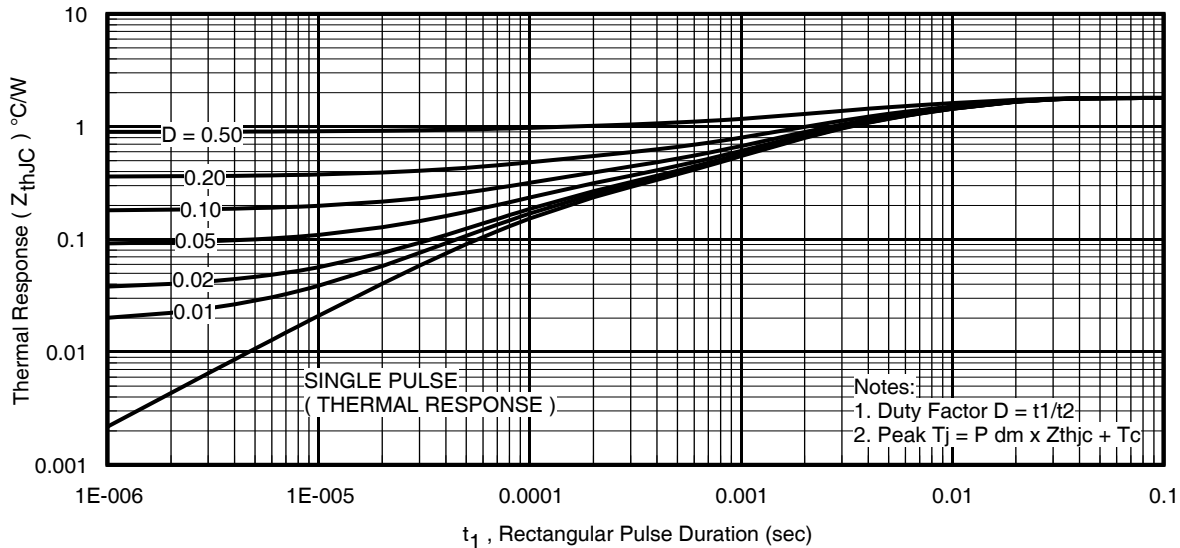
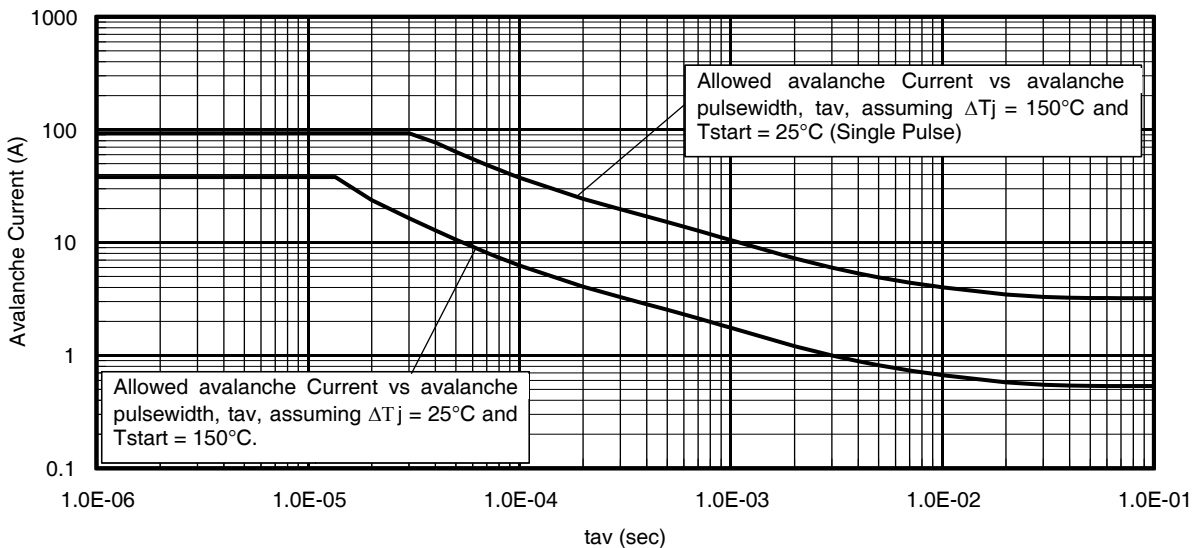
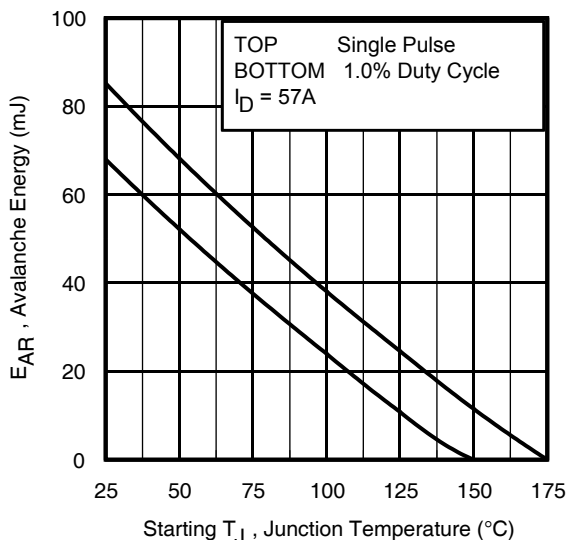
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	170	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 57A
Q <sub>g</sub>	Total Gate Charge	—	45	68	nC	I <sub>D</sub> = 57A V <sub>DS</sub> = 20V V <sub>GS</sub> = 10V <sup>④</sup>
Q <sub>gs</sub>	Gate-to-Source Charge	—	12	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	15	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> – Q <sub>gd</sub> )	—	30	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	7.8	—	ns	V <sub>DD</sub> = 20V I <sub>D</sub> = 30A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V <sup>④</sup>
t <sub>r</sub>	Rise Time	—	35	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	25	—		
t <sub>f</sub>	Fall Time	—	19	—		
C <sub>iss</sub>	Input Capacitance	—	2110	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig.7 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V <sup>⑥</sup> V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V <sup>⑤</sup>
C <sub>oss</sub>	Output Capacitance	—	340	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	220	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	400	—		
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	498	—		

**Diode Characteristics**

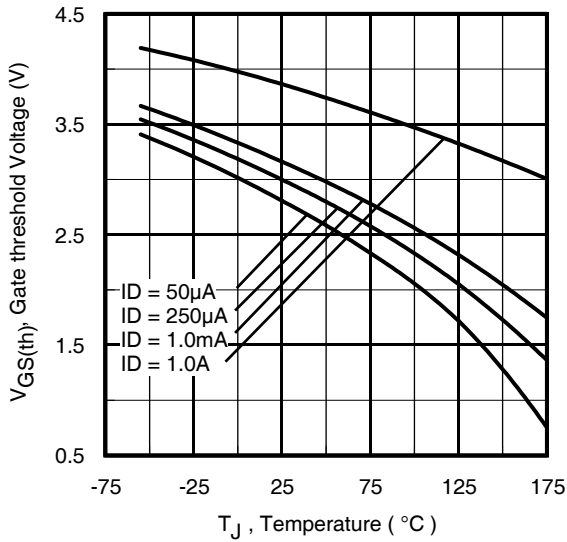
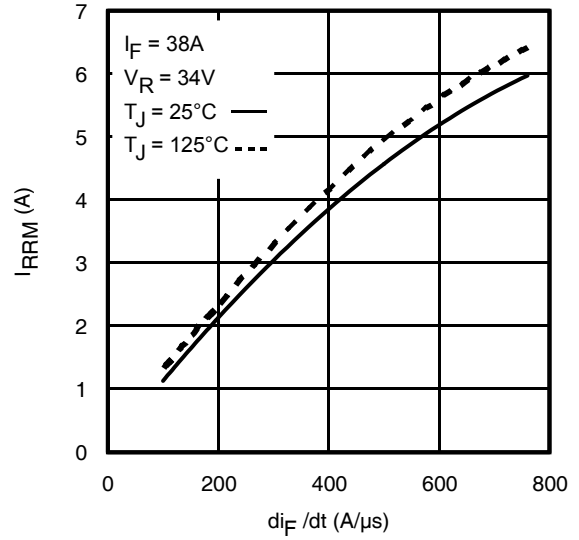
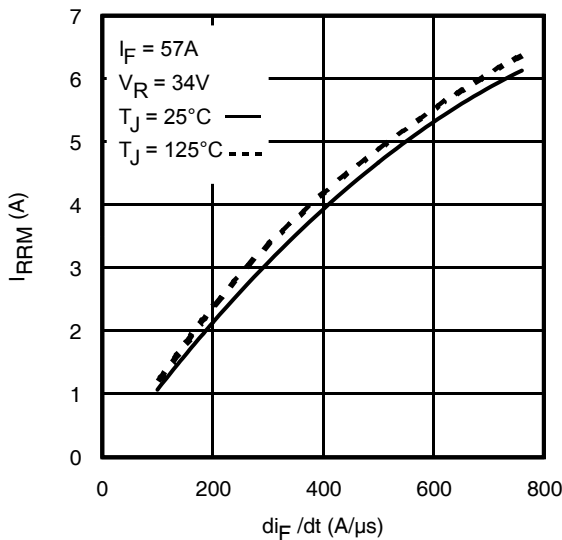
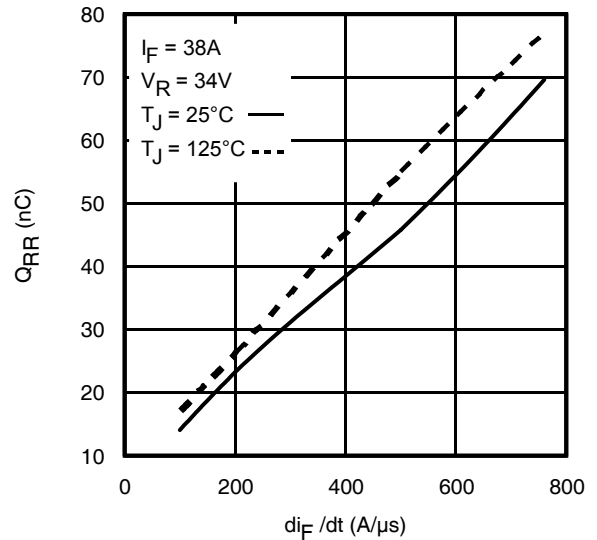
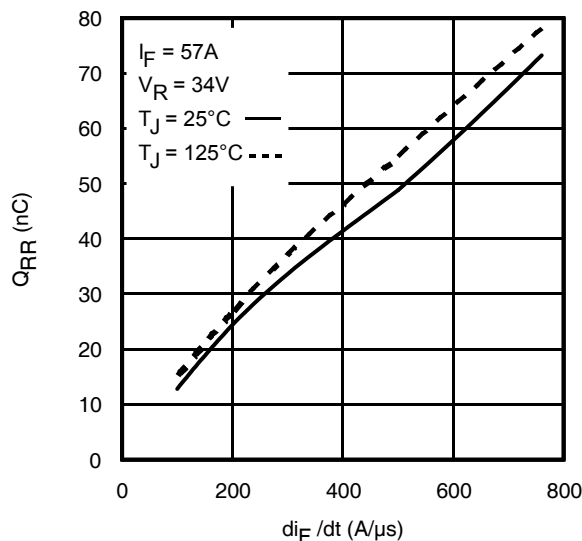
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	95	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	380		
V <sub>SD</sub>	Diode Forward Voltage	—	0.9	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 57A, V <sub>GS</sub> = 0V <sup>④</sup>
dv/dt	Peak Diode Recovery dv/dt <sup>③</sup>	—	6.4	—	V/ns	T <sub>J</sub> = 175°C, I <sub>S</sub> = 57A, V <sub>DS</sub> = 40V
t <sub>rr</sub>	Reverse Recovery Time	—	21	—	ns	V <sub>DD</sub> = 34V I <sub>F</sub> = 57A, di/dt = 100A/μs <sup>④</sup>
		—	22	—		
Q <sub>rr</sub>	Reverse Recovery Charge	—	13	—	nC	T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C
		—	15	—		
I <sub>RRM</sub>	Reverse Recovery Current	—	1.1	—	A	T <sub>J</sub> = 25°C

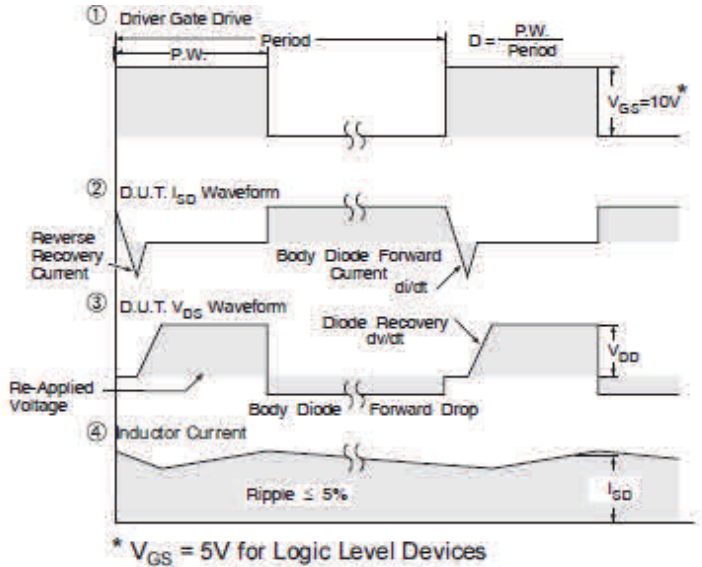
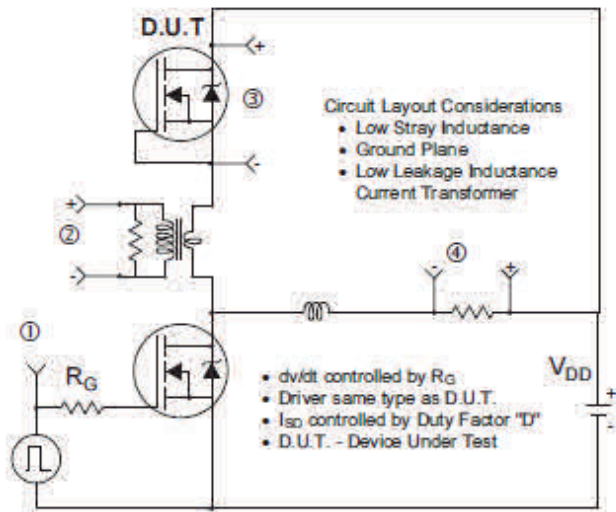
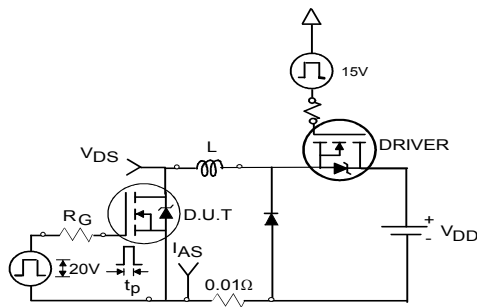
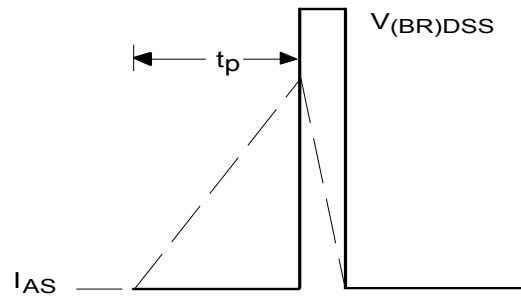
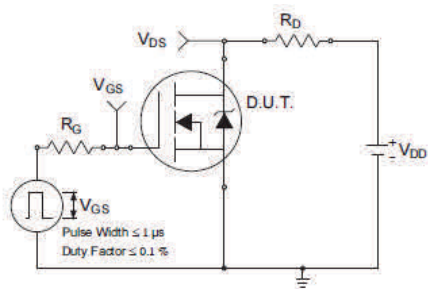
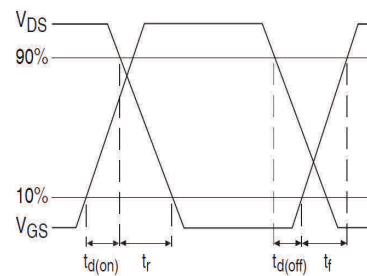

**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**

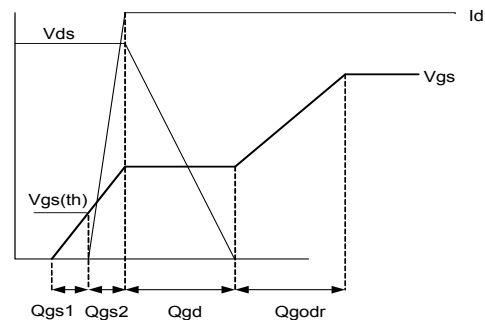

**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current


**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse Width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

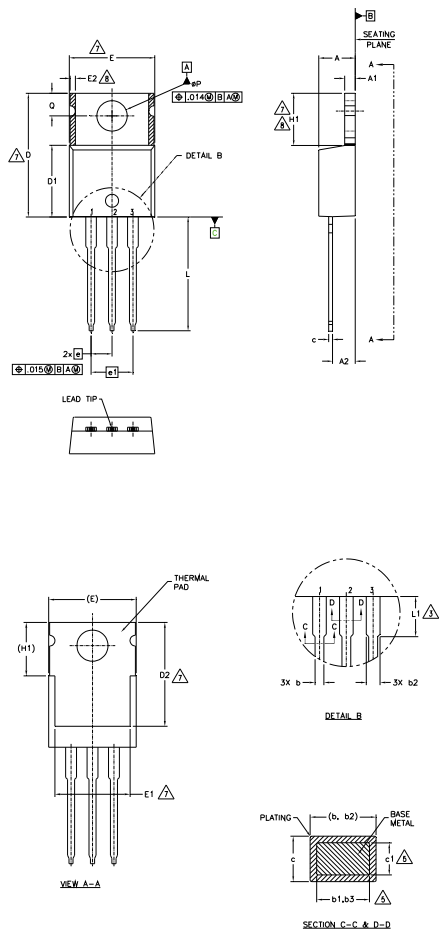
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 14)  
 $P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


**Fig 17.** Threshold Voltage vs. Temperature

**Fig 18.** Typical Recovery Current vs.  $di/dt$ 

**Fig 19.** Typical Recovery Current vs.  $di/dt$ 

**Fig 20.** Typical Stored Charge vs.  $di/dt$ 

**Fig 21.** Typical Stored Charge vs.  $di/dt$


**Fig 22.** Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs

**Fig 23a.** Unclamped Inductive Test Circuit

**Fig 23b.** Unclamped Inductive Waveforms

**Fig 24a.** Switching Time Test Circuit

**Fig 24b.** Switching Time Waveforms

**Fig 25a.** Gate Charge Test Circuit

**Fig 25b.** Gate Charge Waveform



**TO-220AB Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

- 1.- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- 3.- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
- 4.- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- 5.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- 6.- CONTROLLING DIMENSION : INCHES.
- 7.- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- 8.- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
- 9.- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	1.14	1.40	.045	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
H1	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER

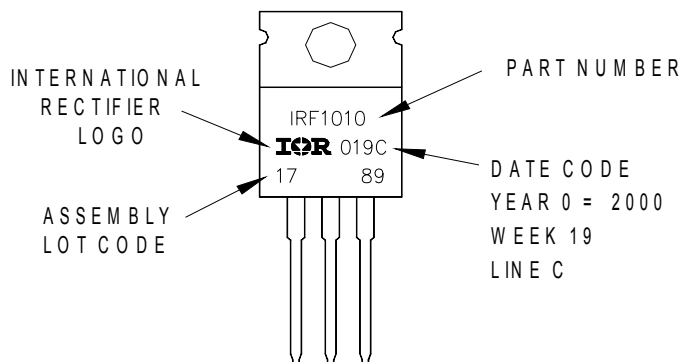
**DIODES**

- 1.- ANODE
- 2.- CATHODE
- 3.- ANODE

**TO-220AB Part Marking Information**

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

<b>Qualification Level</b>	Industrial (per JEDEC JESD47F) <sup>††</sup>	
<b>Moisture Sensitivity Level</b>	TO-220	N/A
<b>RoHS Compliant</b>	Yes	

† Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

†† Applicable version of JEDEC standard at the time of product release.

## IMPORTANT NOTICE

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