

# Protection Device

TVS (Transient Voltage Suppressor)

## ESD110-B1 Series

Bi-directional, 18.5 V (AC), 0.3 pF, 0201, 0402, RoHS and Halogen Free compliant

ESD110-B1-02ELS  
ESD110-B1-02EL

## Data Sheet

Revision 1.4, 2014-10-23  
Final

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# 1 Product Overview

## 1.1 Features

- ESD / transient protection according to:
  - IEC61000-4-2 (ESD):  $\pm 15$  kV (air),  $\pm 12$  kV (contact)
  - IEC61000-4-5 (Surge):  $\pm 2$  A ( $t_p = 8 / 20 \mu s$ )
- Bi-directional, working voltage up to  $V_{RWM} = \pm 18.5$  V (AC)
- Ultra-low capacitance:  $C_L = 0.3$  pF (typical)
- Low clamping voltage:  $V_{CL} = 28$  V (typical) at  $I_{TLP} = 16$  A
- Very low reverse current:  $I_R < 1$  nA (typical)
- Pb-free (RoHS compliant) and halogen free package



## 1.2 Application Examples

- ESD Protection of RF signal lines in Near Field Communication (NFC) applications

## 1.3 Product Description

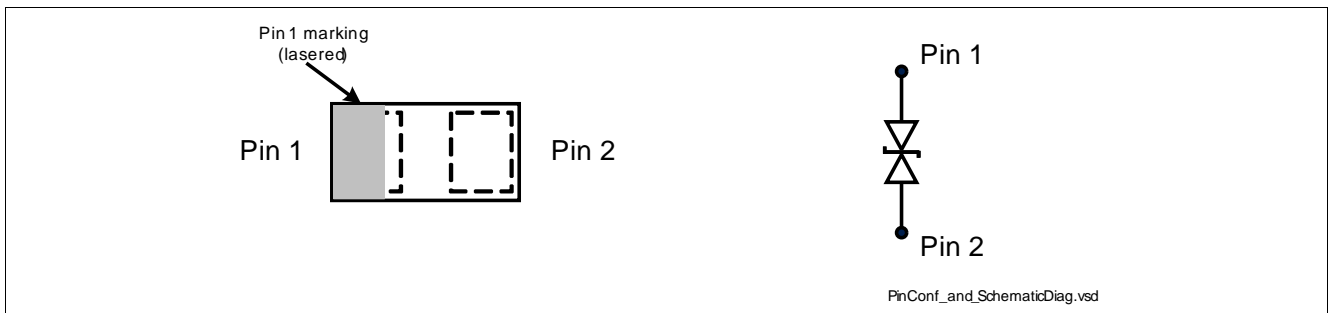


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD110-B1-02ELS	TSSLP-2-4	1 line, bi-directional	X
ESD110-B1-02EL	TSLP-2-20	1 line, bi-directional	XX

## 2 Maximum Ratings

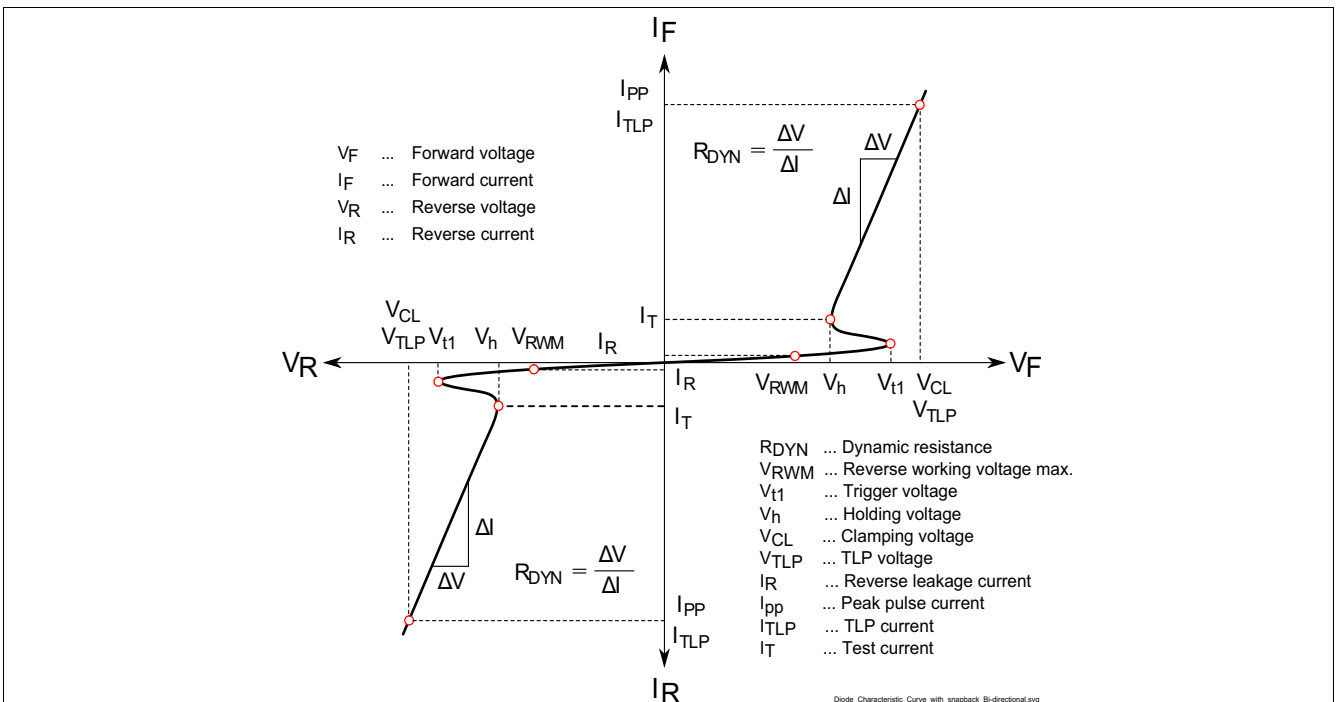
**Table 2-1** Maximum Ratings at  $T_A = 25\text{ °C}$ , unless otherwise specified<sup>1)</sup>

Parameter	Symbol	Values	Unit
ESD air discharge <sup>2)</sup>	$V_{ESD}$	$\pm 15$	kV
ESD contact discharge <sup>2)</sup>		$\pm 12$	
Peak pulse power <sup>3)</sup>	$P_{PK}$	58	W
Peak pulse current <sup>3)</sup>	$I_{PP}$	$\pm 2$	A
Operating temperature	$T_{OP}$	-40 to 125	°C
Storage temperature	$T_{stg}$	-55 to 150	°C

- 1) Device is electrically symmetrical
- 2)  $V_{ESD}$  according to IEC61000-4-2
- 3) Non-repetitive current pulse 8/20µs exponential decay waveform according to IEC61000-4-5

**Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

## 3 Electrical Characteristics at $T_A = 25\text{ °C}$ , unless otherwise specified



**Figure 3-1** Definitions of electrical characteristics

**Electrical Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**
**Table 3-1 DC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	$V_{RWM}$	-18.5	–	18.5	V	for AC voltages (NFC)
		-15	–	15		for DC voltages
Trigger voltage	$V_{t1}$	20	–	–	V	
Holding voltage	$V_h$	20	21	26	V	$T_A = 25\text{ }^\circ\text{C}$ , $I_T = 0.5\text{ mA}$
		–	19	–		$T_A = 125\text{ }^\circ\text{C}$ , $I_T = 0.5\text{ mA}$
Reverse leakage current	$I_R$	–	<1	30	nA	$T_A = 25\text{ }^\circ\text{C}$ , $V_R = 18.5\text{ V}$
		–	10	–		$T_A = 125\text{ }^\circ\text{C}$ , $V_R = 18.5\text{ V}$

1) Device is electrically symmetrical

**Table 3-2 AC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	0.15	0.3	0.5	pF	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$
		0.15	0.3	0.5		$V_R = 0\text{ V}$ , $f = 1\text{ GHz}$
Serie inductance	$L_S$	–	0.2	–	nH	ESD110-B1-02ELS
		–	0.4	–		ESD110-B1-02EL

**Table 3-3 ESD and Surge Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>2)</sup>	$V_{CL}$	–	30	35	V	$I_{TLP} = 16\text{ A}$ , $t_p = 100\text{ ns}$
		–	39	44		$I_{TLP} = 30\text{ A}$ , $t_p = 100\text{ ns}$
Clamping voltage <sup>3)</sup>	$V_{CL}$	–	19	24		$I_{PP} = 1\text{ A}$ , $t_p = 8/20\text{ }\mu\text{s}$
		–	24	29		$I_{PP} = 2\text{ A}$ , $t_p = 8/20\text{ }\mu\text{s}$
Dynamic resistance <sup>2)</sup>	$R_{DYN}$	–	0.6	–	$\Omega$	$t_p = 100\text{ ns}$

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1]. TLP parameter:  $Z_0 = 50\text{ }\Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 300\text{ ps}$

3) Non-repetitive current pulse 8/20 $\mu\text{s}$  exponential decay waveform according to IEC61000-4-5

## 4 Typical Characteristics Diagrams

Typical characteristics diagrams at  $T_A=25^\circ\text{C}$ , unless otherwise specified

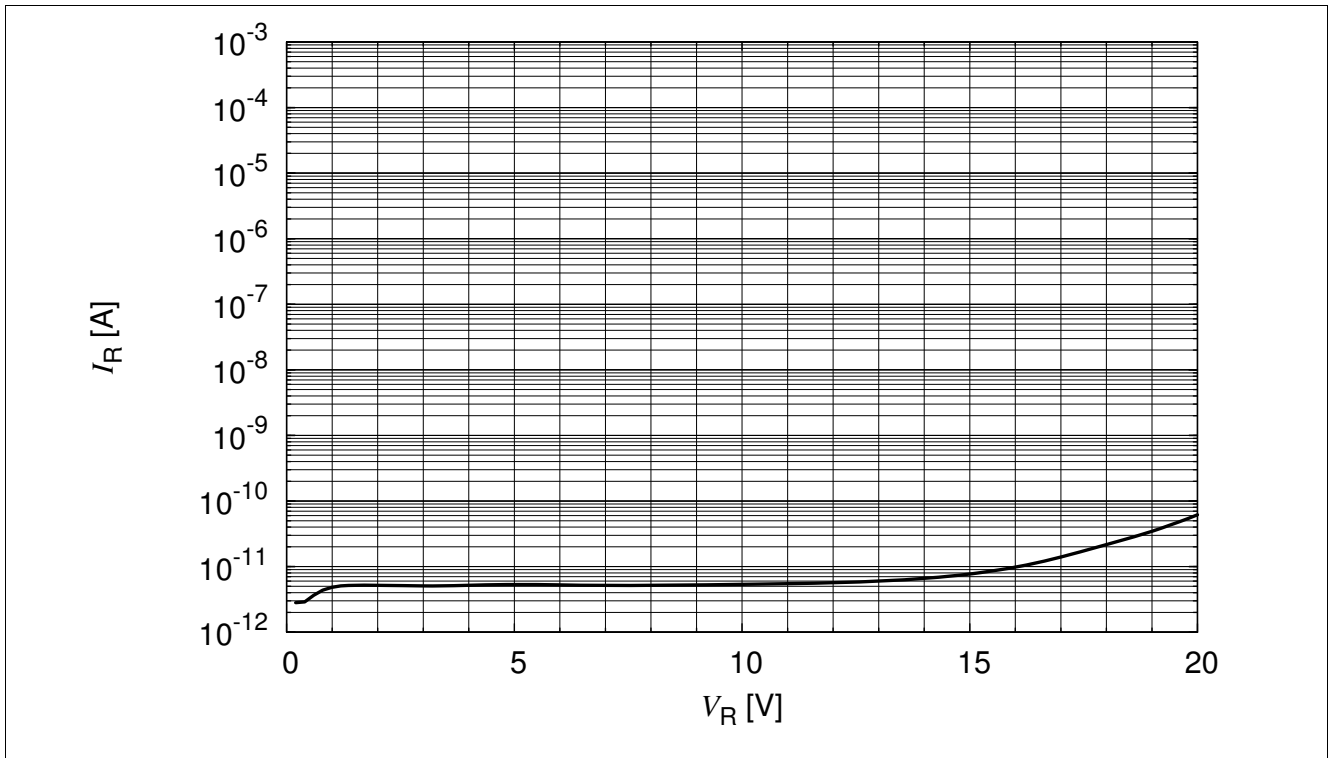


Figure 4-1 Reverse leakage current:  $I_R = f(V_R)$

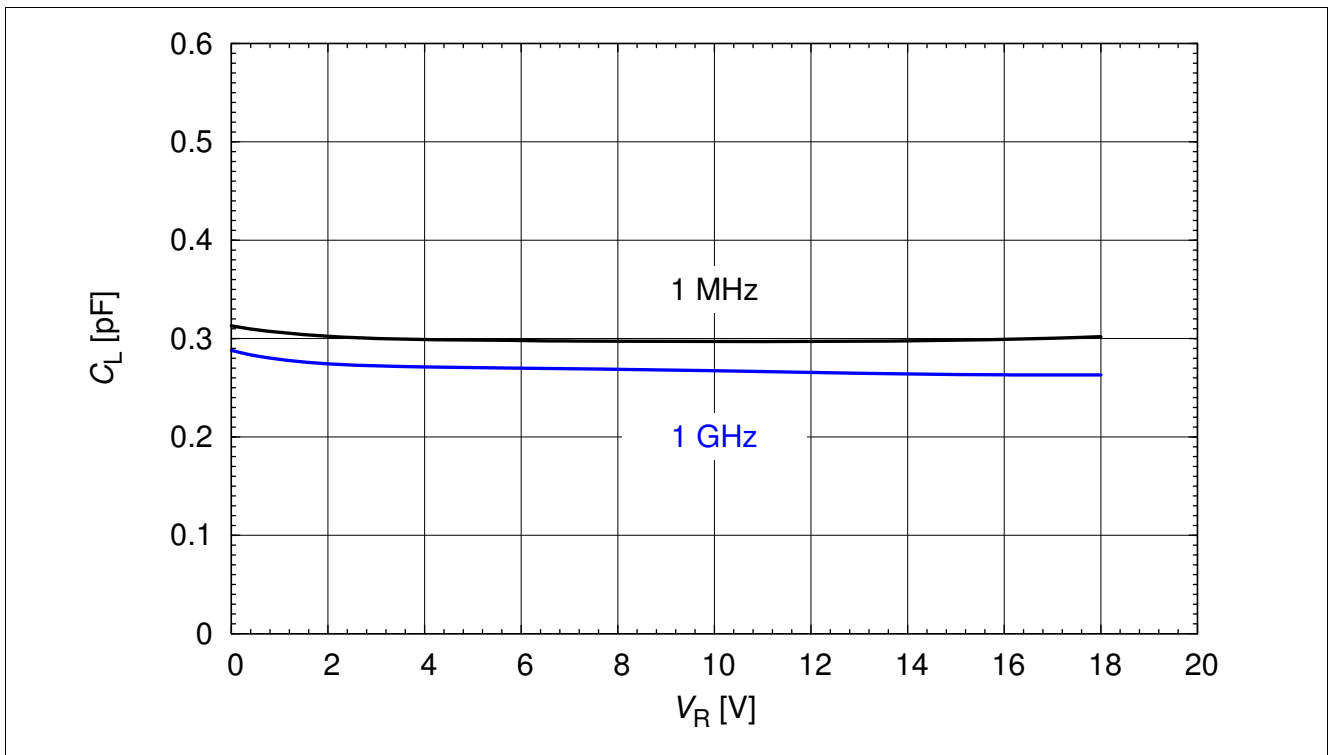


Figure 4-2 Line capacitance:  $C_L = f(V_R)$

Typical Characteristics Diagrams

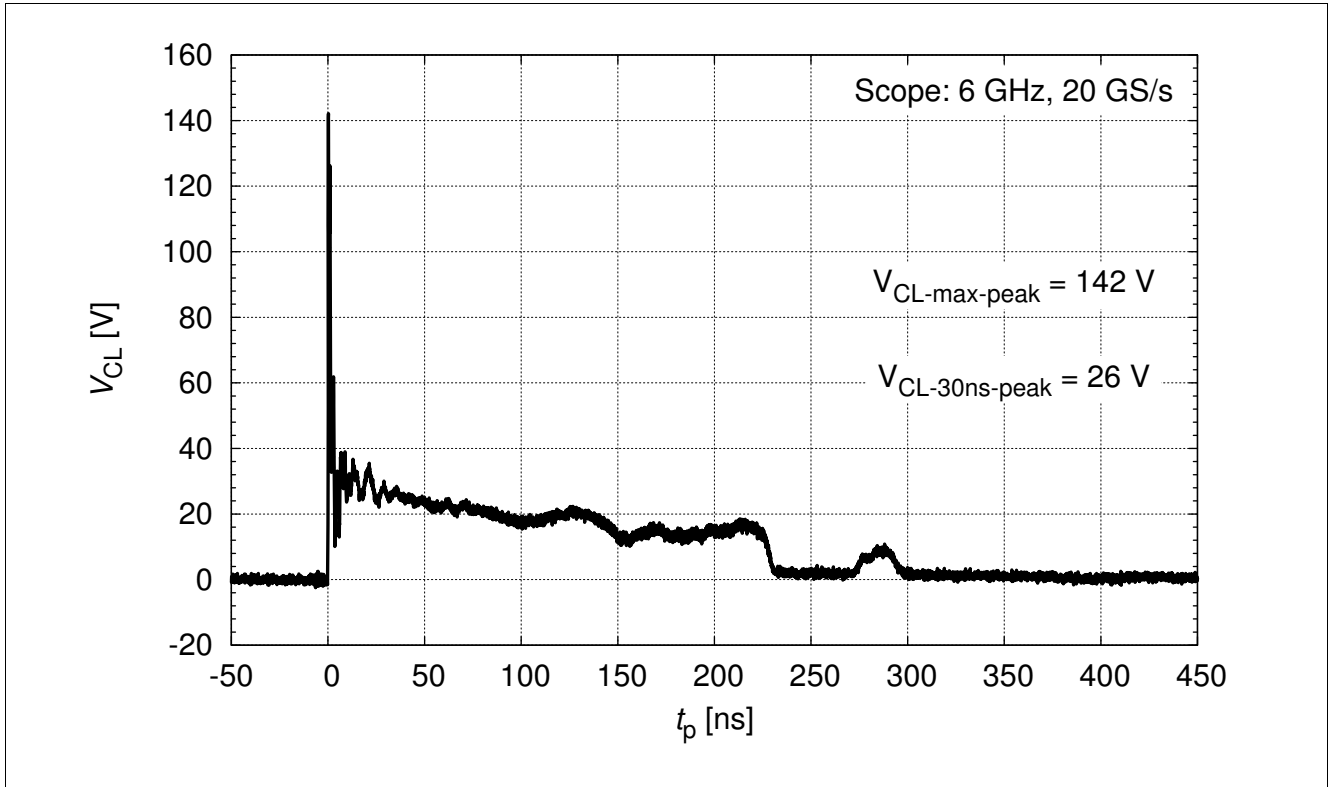


Figure 4-3 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV positiv pulse from pin 1 to pin 2

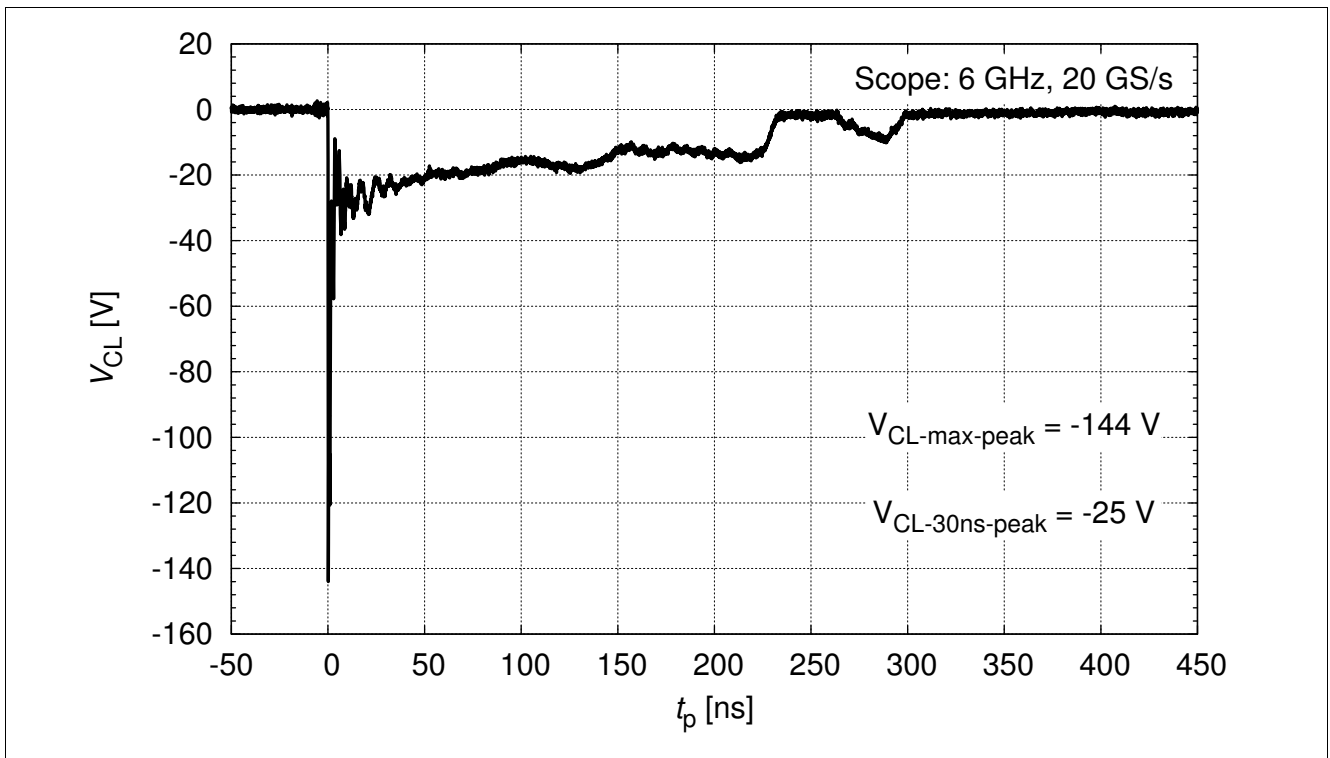


Figure 4-4 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV negativ pulse from pin 1 to pin 2

Typical Characteristics Diagrams

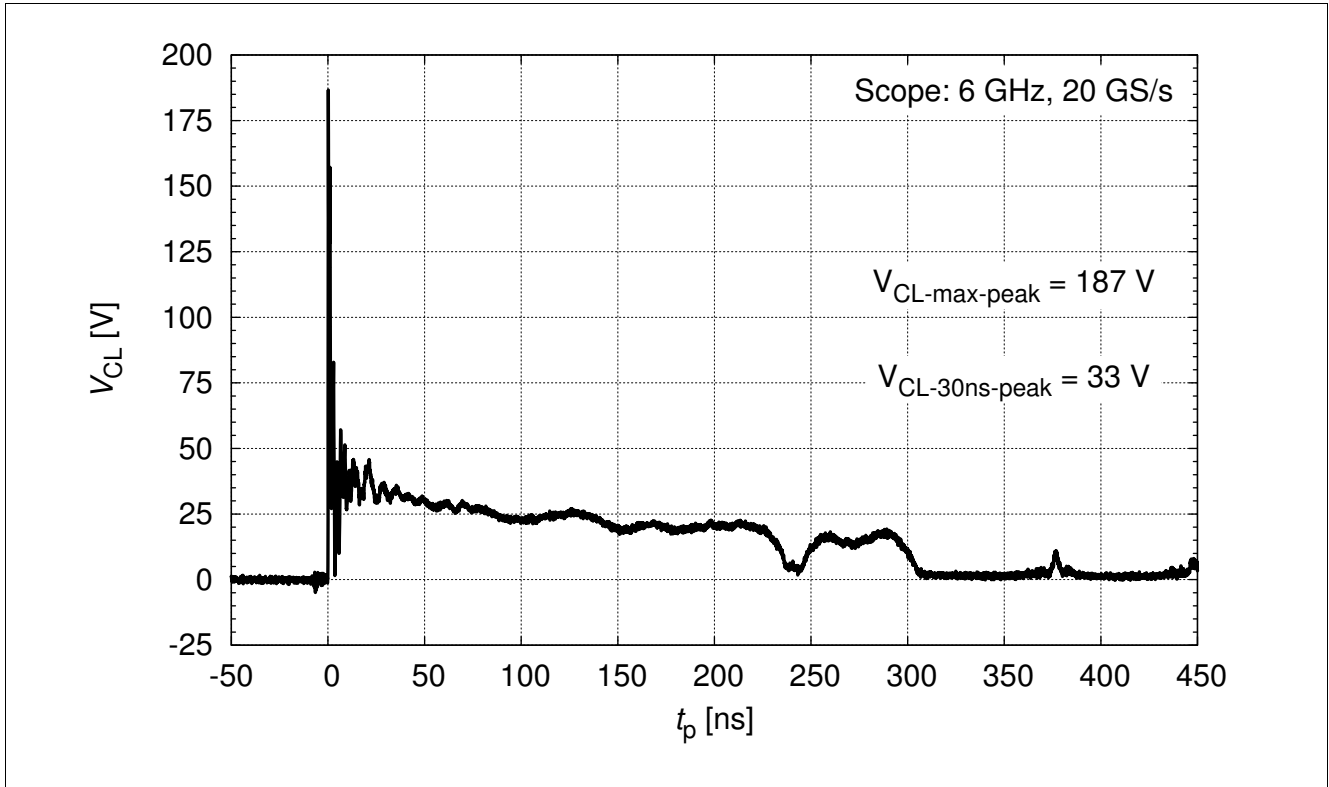


Figure 4-5 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV positiv pulse from pin 1 to pin 2

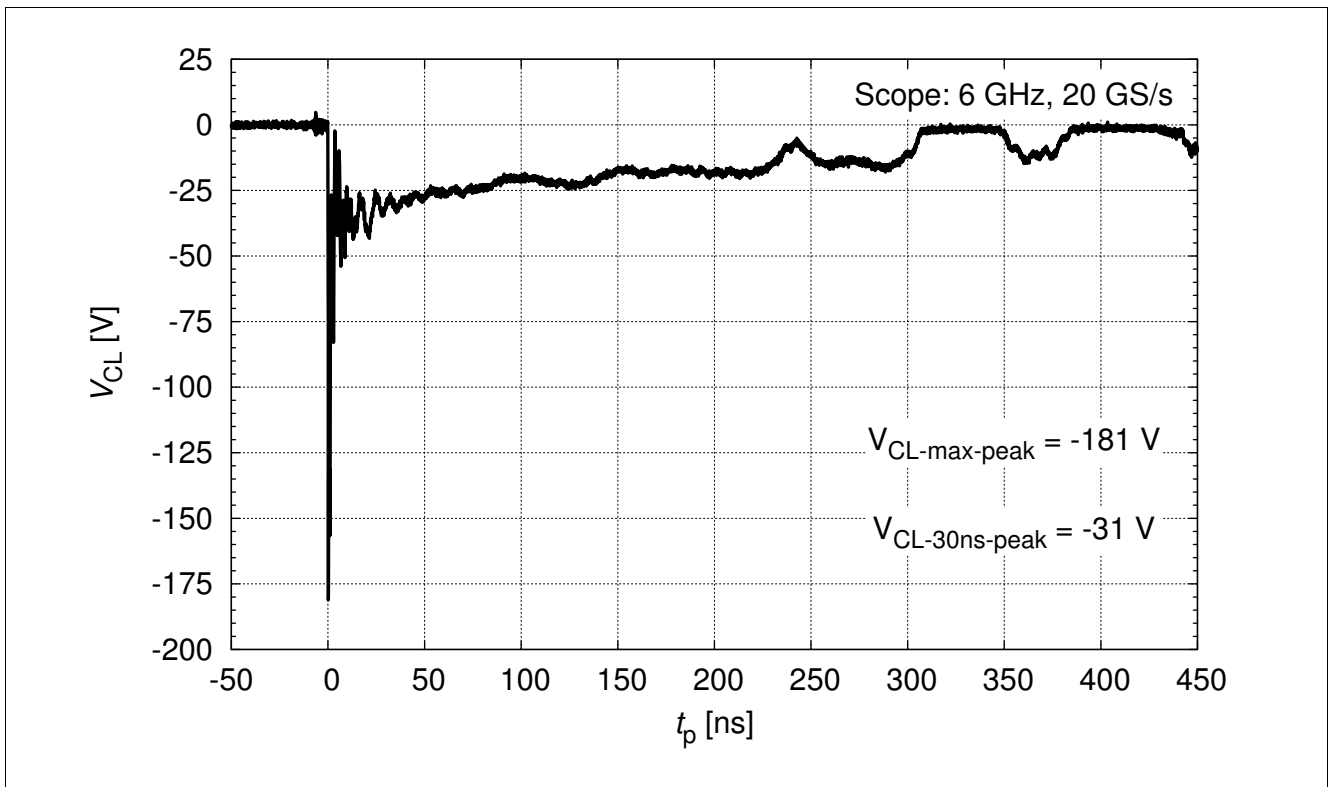


Figure 4-6 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV negativ pulse from pin 1 to pin 2



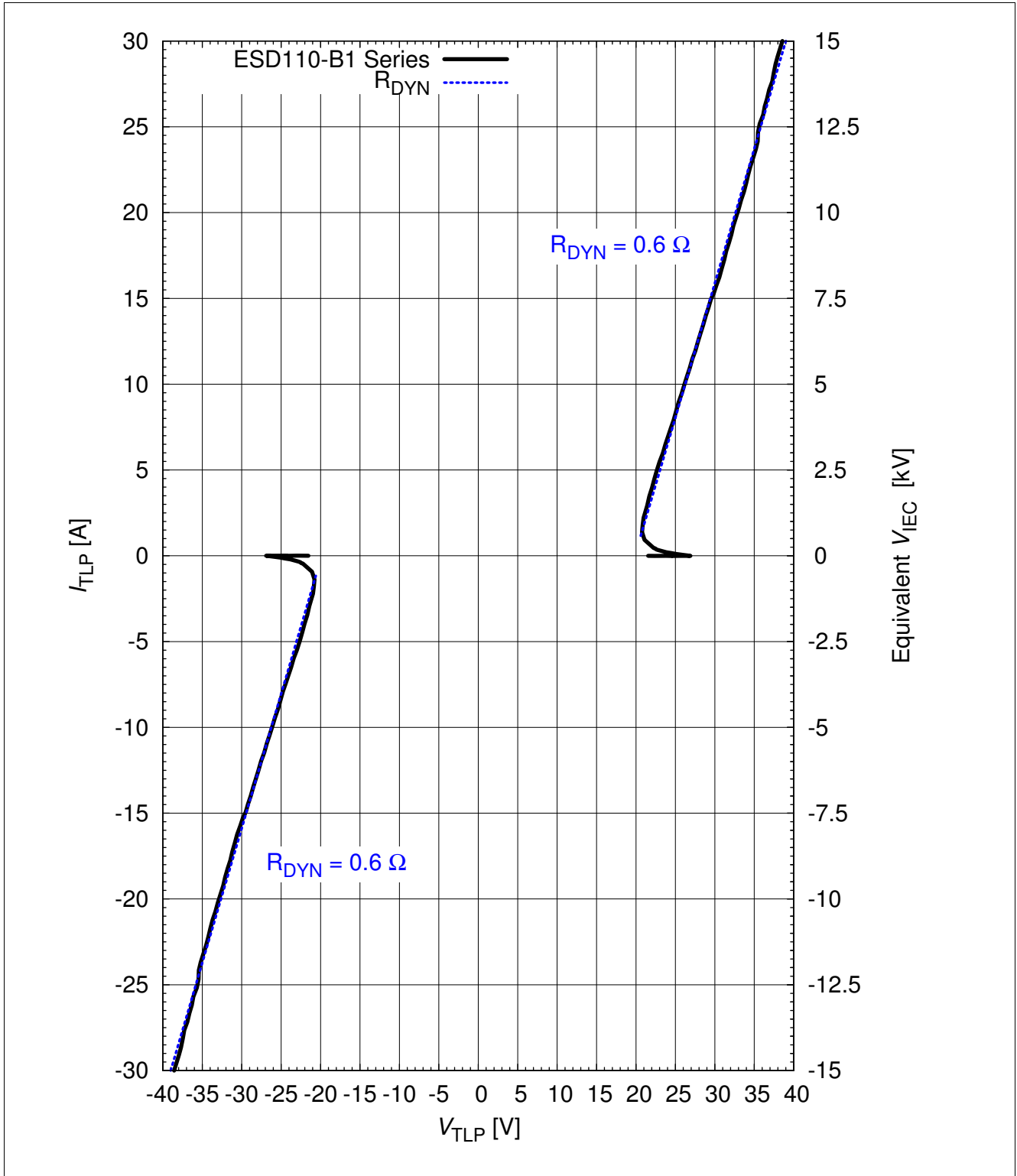


Figure 4-7 Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$  [1], pin 1 to pin 2

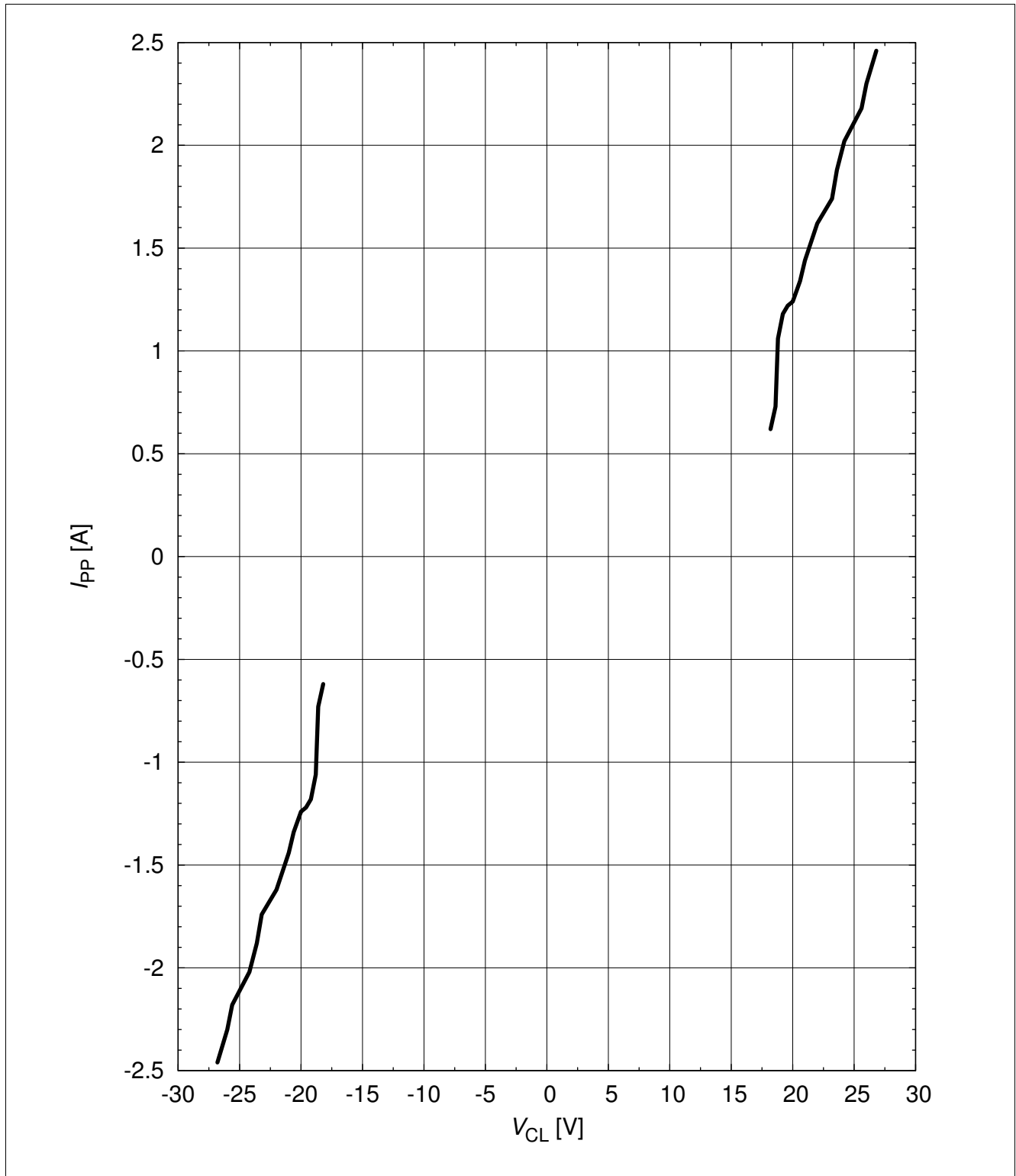


Figure 4-8 Clamping voltage(Surge):  $I_{PP} = f(V_{CL})$

Typical Characteristics Diagrams

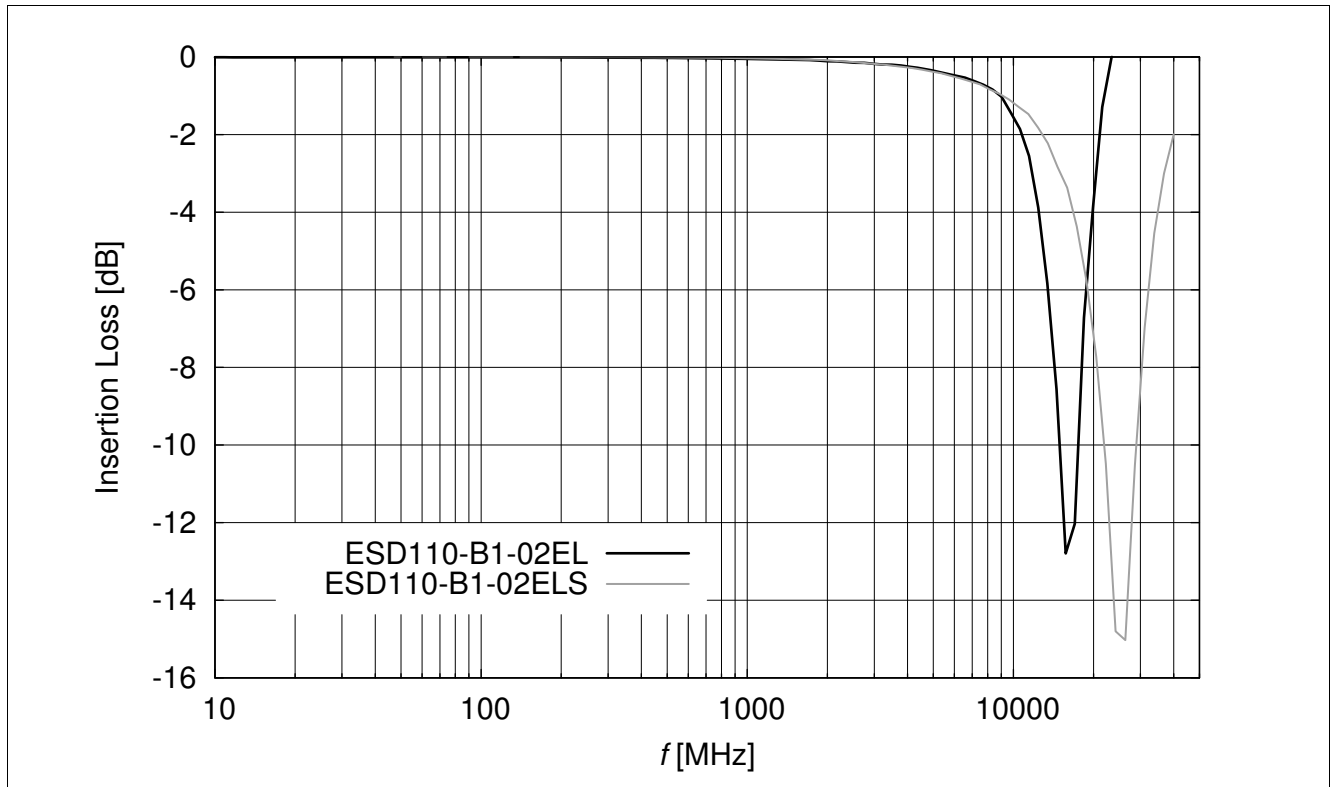


Figure 4-9 Insertion loss vs. frequency in a 50 Ω system

5 Application Information

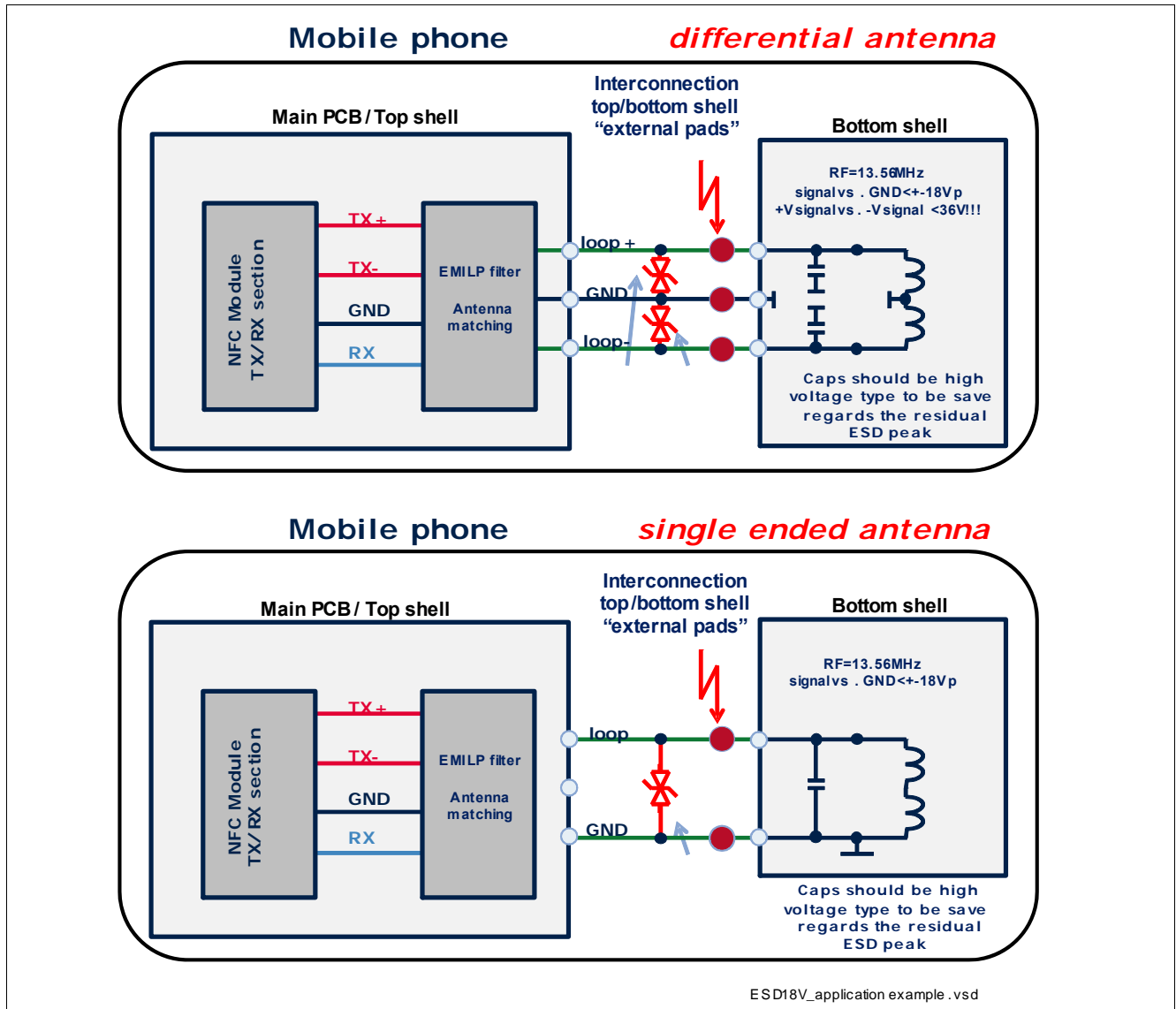


Figure 5-1 Bi-directional ESD / Transient protection for NFC Frontend [3]

## 6 Package Information

### 6.1 TSSLP-2-4

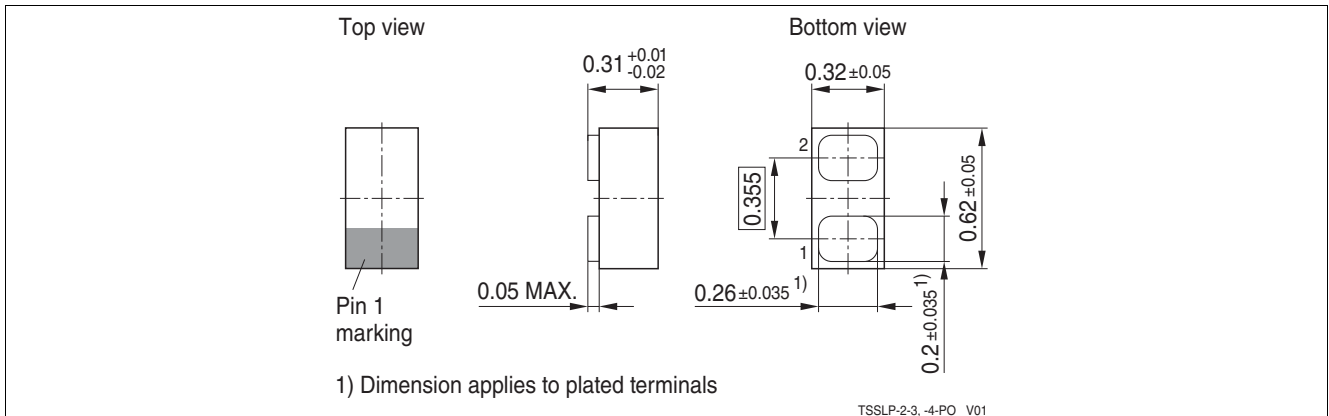


Figure 6-1 TSSLP-2-4: Package outline

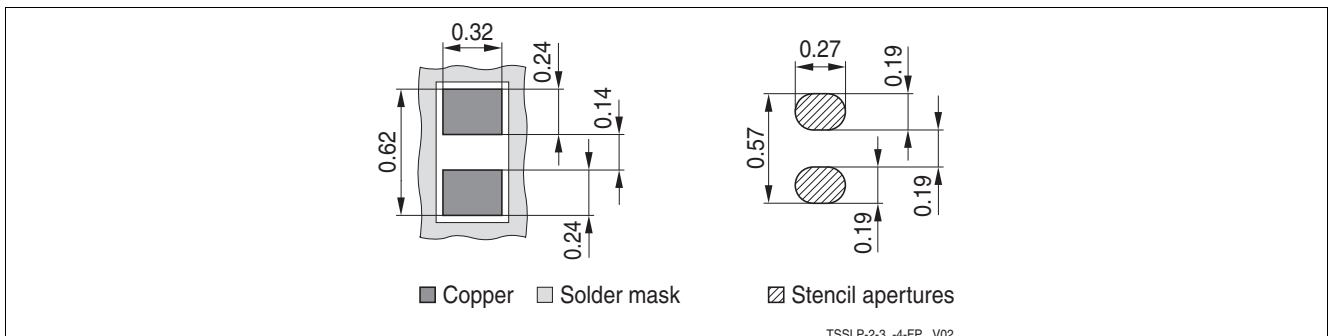


Figure 6-2 TSSLP-2-4: Footprint

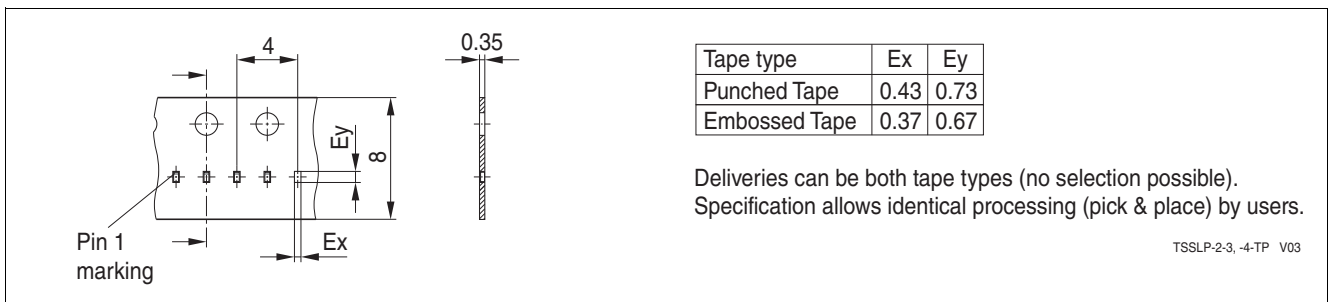


Figure 6-3 TSSLP-2-4: Packing

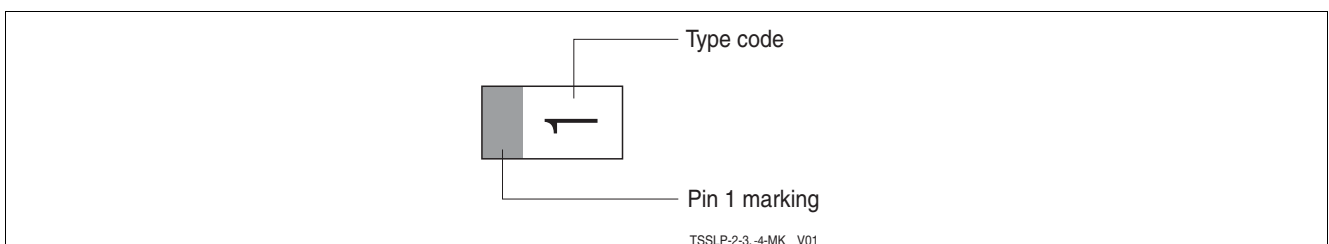


Figure 6-4 TSSLP-2-4: Marking (example) [Table 1-1 "Part Information" on Page 3](#)

6.2 TSLP-2-20

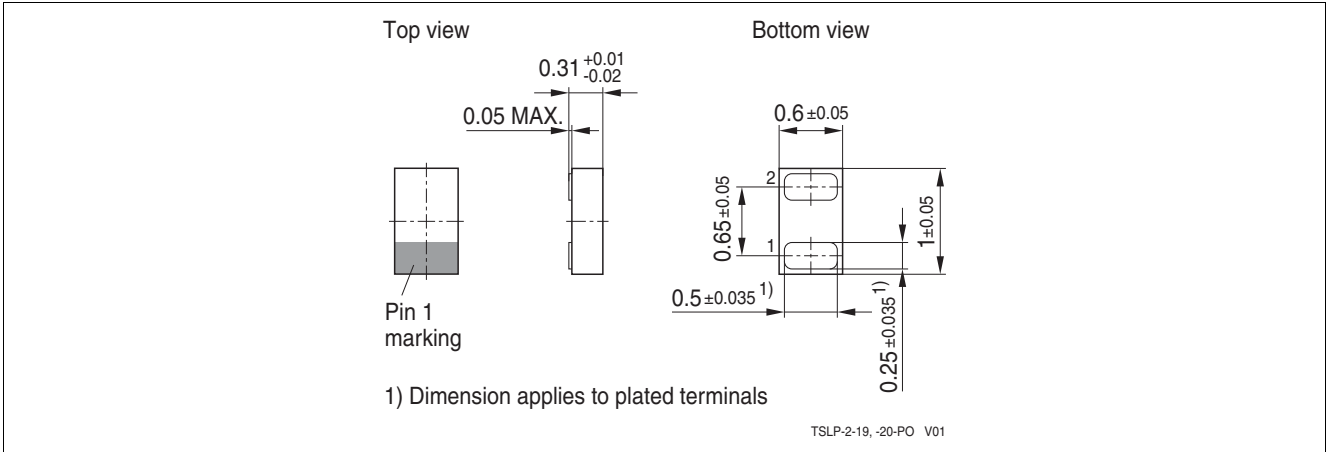


Figure 6-5 TSLP-2-20: Package overview

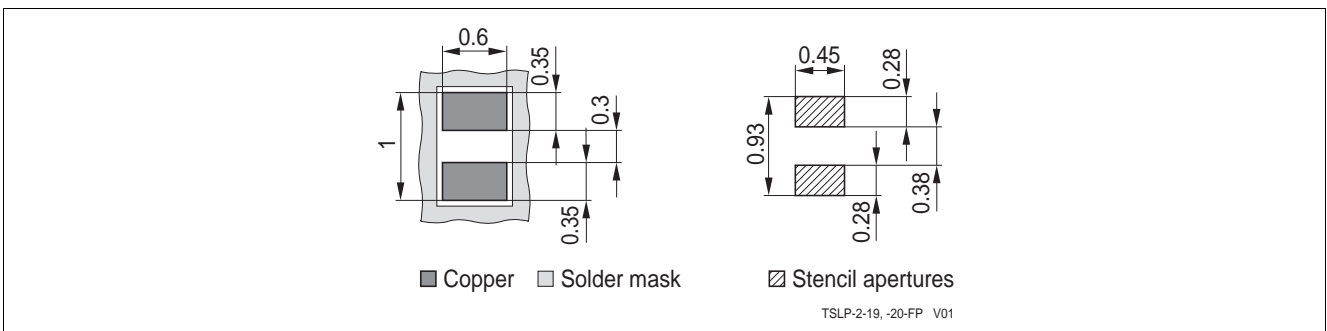


Figure 6-6 TSLP-2-20: Footprint

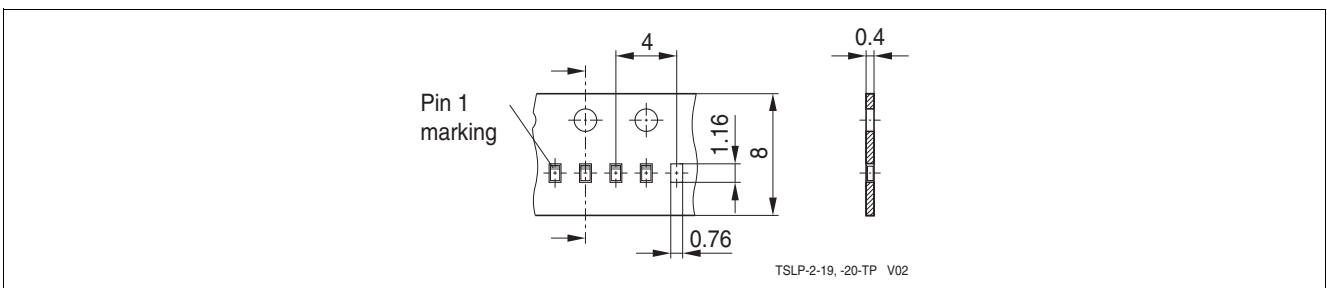


Figure 6-7 TSLP-2-20: Packing

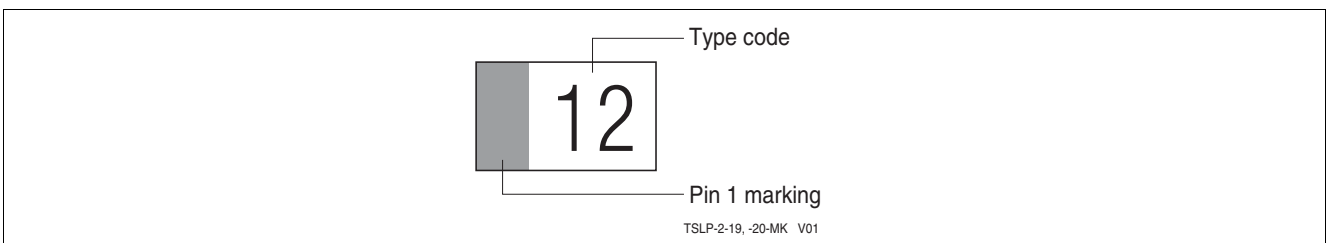


Figure 6-8 TSLP-2-20: Marking example [Table 1-1 "Part Information" on Page 3](#)

## References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Packages
- [3] Infineon AG - **Application Note AN244**: Tailored ESD Protection for the NFC Frontend

**Revision History: Rev. 1.3, 2014-04-08**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.4, 2014-10-23</b>	
4	Table 2-1) updated

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