

**HIGH AND LOW SIDE DRIVER**

**Features**

- Floating channel designed for bootstrap operation
- Fully operational to +200 V
- Tolerant to negative transient voltage, dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout
- 3.3 V, 5 V, and 15 V logic input compatible
- Matched propagation delay for both channels
- Outputs in phase with inputs
- RoHS compliant

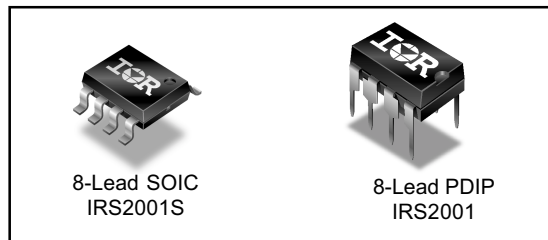
**Description**

The IRS2001 is a high voltage, high speed power MOSFET and IGBT driver with independent high-side and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration which operates up to 200 V.

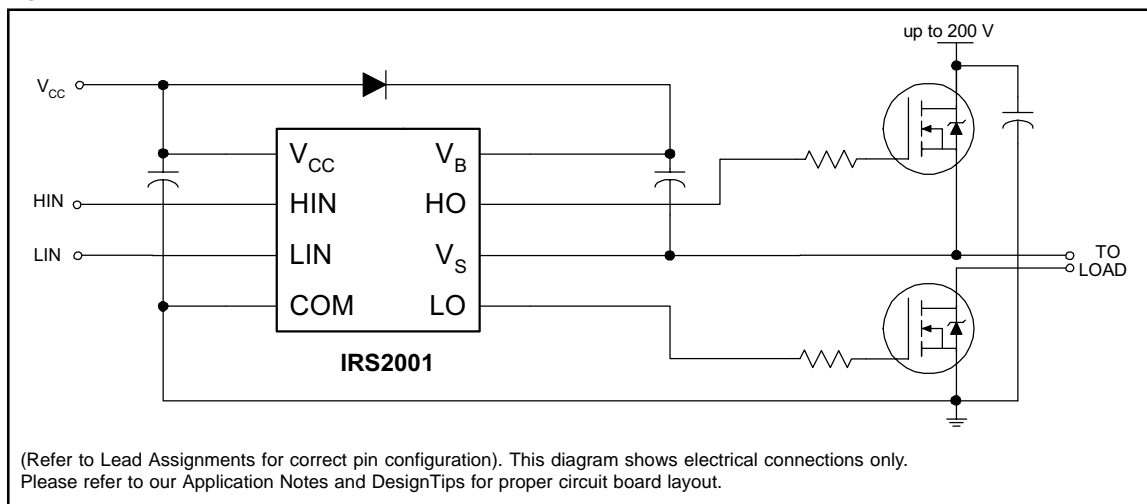
**Product Summary**

$V_{\text{OFFSET}}$	200 V max.
$I_{\text{O}+/-}$	200 mA/420 mA
$V_{\text{OUT}}$	10 V - 20 V
$t_{\text{on/off}}$ (typ.)	160 ns/150 ns
Delay Matching	50 ns

**Packages**



**Typical Connection**



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units	
V <sub>B</sub>	High-side floating supply voltage	-0.3	225	V	
V <sub>S</sub>	High-side floating supply offset voltage	V <sub>B</sub> - 25	V <sub>B</sub> + 0.3		
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3		
V <sub>CC</sub>	Low-side and logic fixed supply voltage	-0.3	25		
V <sub>LO</sub>	Low-side output voltage	-0.3	V <sub>CC</sub> + 0.3		
V <sub>IN</sub>	Logic input voltage (HIN & LIN)	-0.3	V <sub>CC</sub> + 0.3		
dV <sub>S</sub> /dt	Allowable offset supply voltage transient	—	50	V/ns	
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25 °C	(8 lead PDIP)	—	1.0	W
		(8 lead SOIC)	—	0.625	
R <sub>thJA</sub>	Thermal resistance, junction to ambient	(8 lead PDIP)	—	125	°C/W
		(8 lead SOIC)	—	200	
T <sub>J</sub>	Junction temperature	—	150	°C	
T <sub>S</sub>	Storage temperature	-55	150		
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300		

## Recommended Operating Conditions

The input/output logic timing diagram is shown in Fig. 1. For proper operation the device should be used within the recommended conditions. The V<sub>S</sub> offset rating is tested with all supplies biased at a 15 V differential.

Symbol	Definition	Min.	Max.	Units
V <sub>B</sub>	High-side floating supply absolute voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	V
V <sub>S</sub>	High-side floating supply offset voltage	Note 1	200	
V <sub>HO</sub>	High-side floating output voltage	V <sub>S</sub>	V <sub>B</sub>	
V <sub>CC</sub>	Low-side and logic fixed supply voltage	10	20	
V <sub>LO</sub>	Low-side output voltage	0	V <sub>CC</sub>	
V <sub>IN</sub>	Logic input voltage (HIN & LIN)	0	V <sub>CC</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

**Note 1:** Logic operational for V<sub>S</sub> of -5 V to +200 V. Logic state held for V<sub>S</sub> of -5 V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$ ,  $C_L = 1000\text{ pF}$  and  $T_A = 25\text{ °C}$  unless otherwise specified.

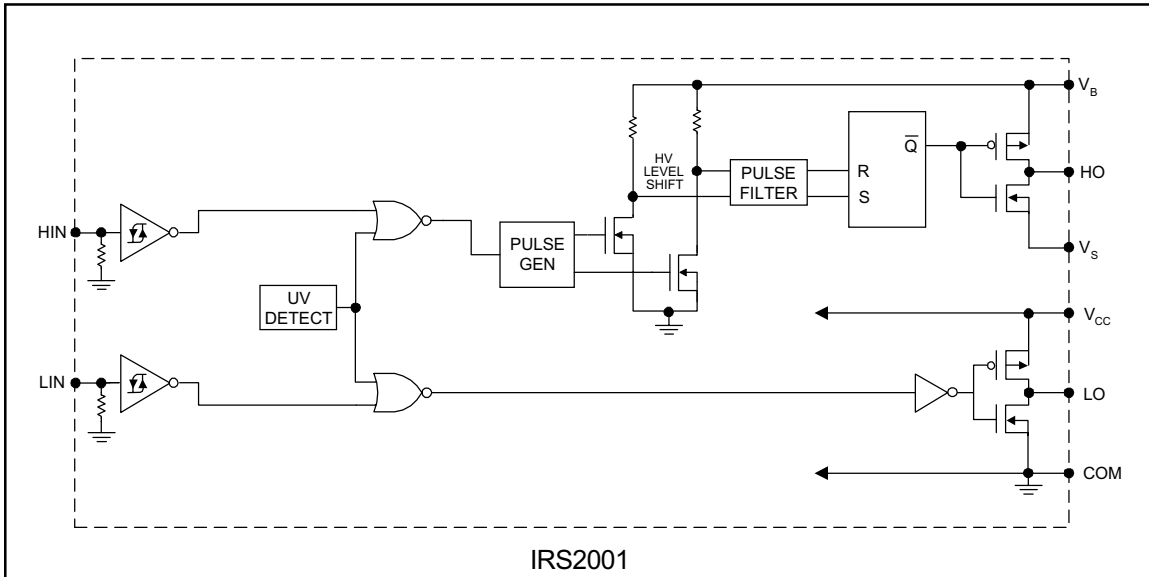
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	160	220	ns	$V_S = 0\text{ V}$
$t_{off}$	Turn-off propagation delay	—	150	220		$V_S = 200\text{ V}$
$t_r$	Turn-on rise time	—	70	100		
$t_f$	Turn-off fall time	—	35	60		
MT	Delay matching, HS & LS turn-on/off	—	—	50		

## Static Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15\text{ V}$  and  $T_A = 25\text{ °C}$  unless otherwise specified. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{IH}$	Logic "1" input voltage	2.5	—	—	V	$V_{CC} = 10\text{ V to } 20\text{ V}$
$V_{IL}$	Logic "0" input voltage	—	—	0.8		
$V_{OH}$	High level output voltage, $V_{BIAS} - V_O$	—	0.05	0.1		$I_O = 2\text{ mA}$
$V_{OL}$	Low level output voltage, $V_O$	—	0.02	0.05		
$I_{LK}$	Offset supply leakage current	—	—	50	$\mu\text{A}$	$V_B = V_S = 200\text{ V}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	30	55		$V_{IN} = 0\text{ V or } 5\text{ V}$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	150	270		$V_{IN} = 5\text{ V}$
$I_{IN+}$	Logic "1" input bias current	—	3	10		$V_{IN} = 0\text{ V}$
$I_{IN-}$	Logic "0" input bias current	—	—	5		
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	8	8.9	9.8	V	
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.2	9		
$I_{O+}$	Output high short circuit pulsed current	200	290	—	mA	$V_O = 0\text{ V}$ $V_{IN} = \text{Logic "1"}$ $PW \leq 10\text{ }\mu\text{s}$
$I_{O-}$	Output low short circuit pulsed current	420	600	—		$V_O = 15\text{ V}$ $V_{IN} = \text{Logic "0"}$ $PW \leq 10\text{ }\mu\text{s}$

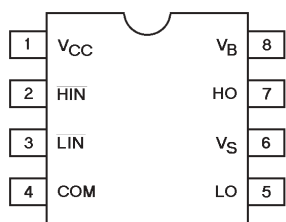
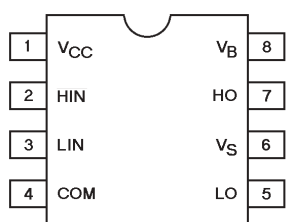
## Functional Block Diagram



## Lead Definitions

Symbol	Description
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side gate driver output (LO), in phase
V <sub>B</sub>	High-side floating supply
HO	High-side gate drive output
V <sub>S</sub>	High-side floating supply return
V <sub>CC</sub>	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return

## Lead Assignments

 <p>8 Lead PDIP</p>	 <p>8 Lead SOIC</p>
<b>IRS2001PbF</b>	<b>IRS2001SPbF</b>
<b>Part Number</b>	

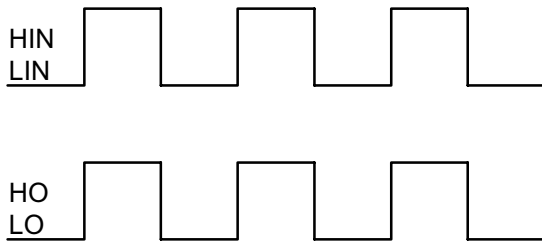


Figure 1. Input/Output Timing Diagram

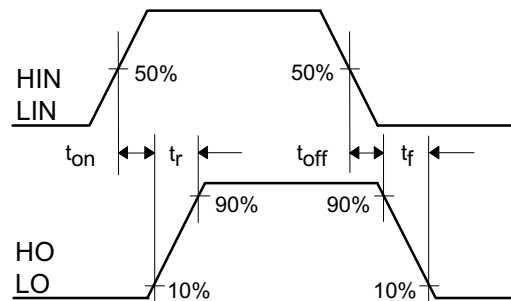


Figure 2. Switching Time Waveform Definitions

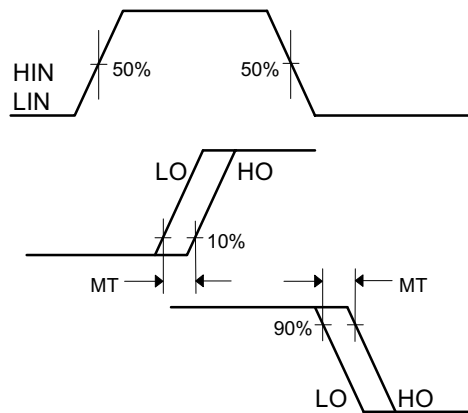
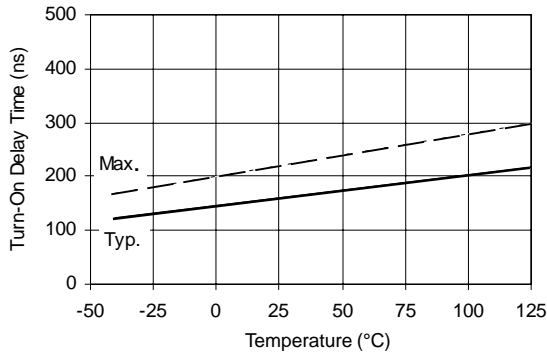
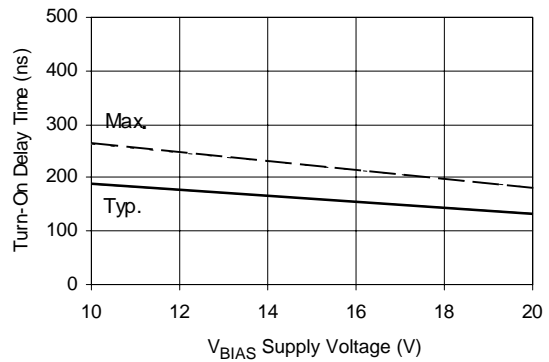


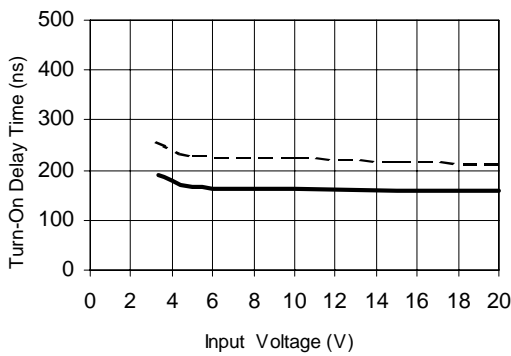
Figure 3. Delay Matching Waveform Definitions



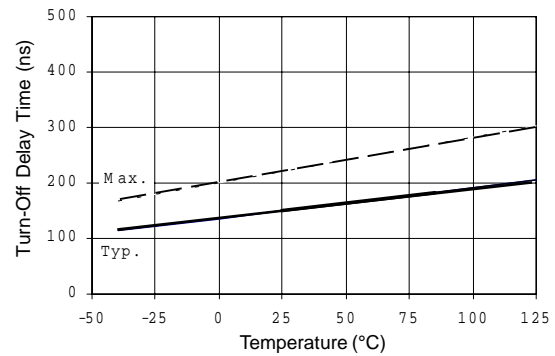
**Figure 6A. Turn-On Time vs. Temperature**



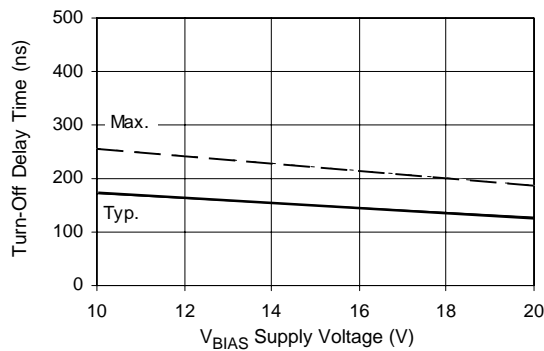
**Figure 6B. Turn-On Time vs. Supply Voltage**



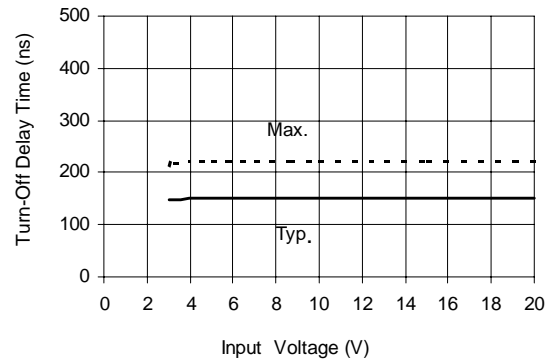
**Figure 6C. Turn-On Time vs. Input Voltage**



**Figure 7A. Turn-Off Time vs. Temperature**



**Figure 7B. Turn-Off Time vs. Supply Voltage**



**Figure 7C. Turn-Off Time vs. Input Voltage**

# IRS2001(S)PbF

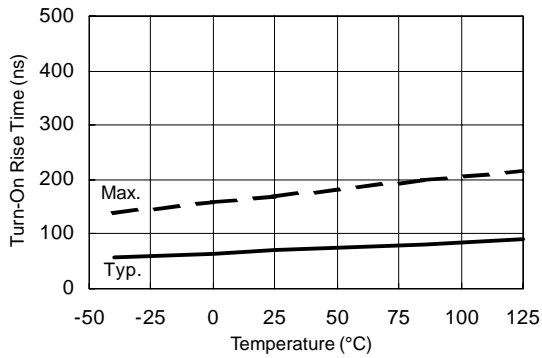


Figure 9A. Turn-On Rise Time vs. Temperature

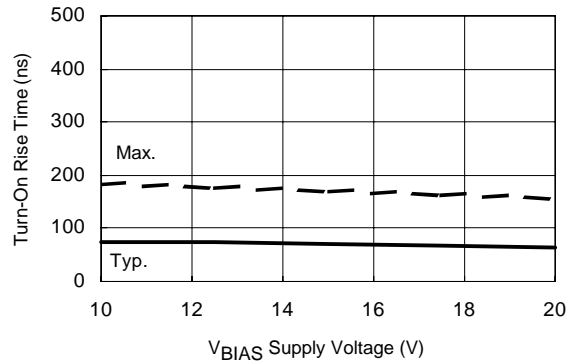


Figure 9B. Turn-On Rise Time vs. Voltage

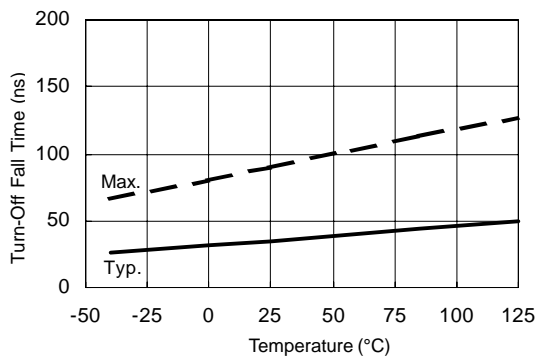


Figure 10A. Turn-Off Fall Time vs. Temperature

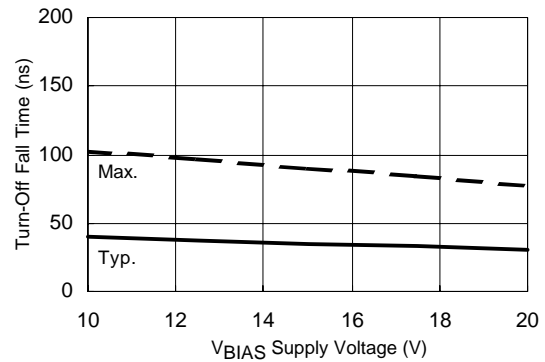


Figure 10B. Turn-Off Fall Time vs. Voltage

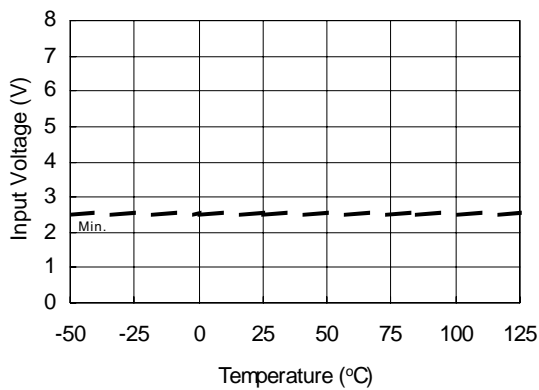


Figure 12A. Logic "1" Input Voltage vs. Temperature

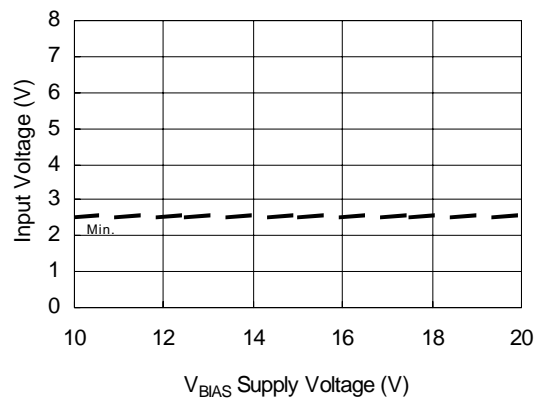
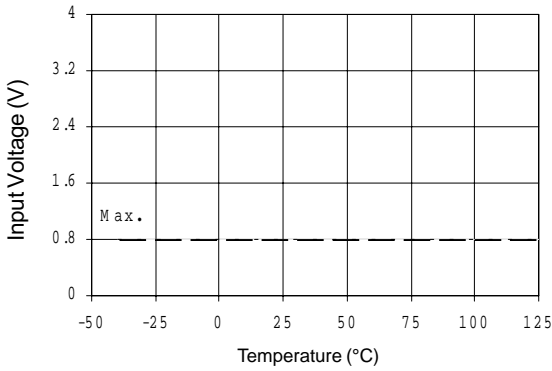


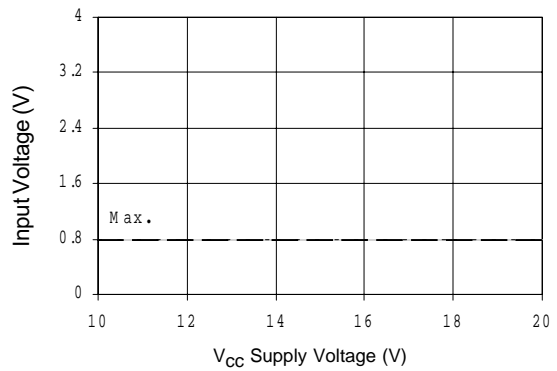
Figure 12B. Logic "1" Input Voltage vs. Voltage



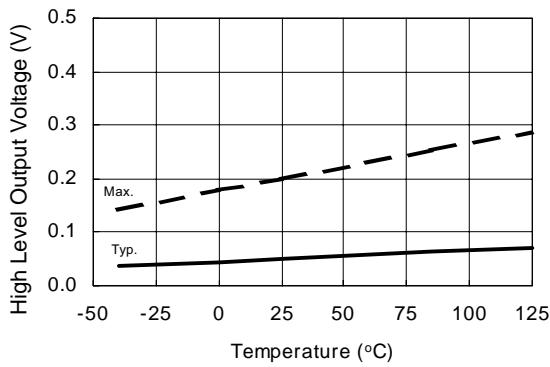
# IRS2001(S)PbF



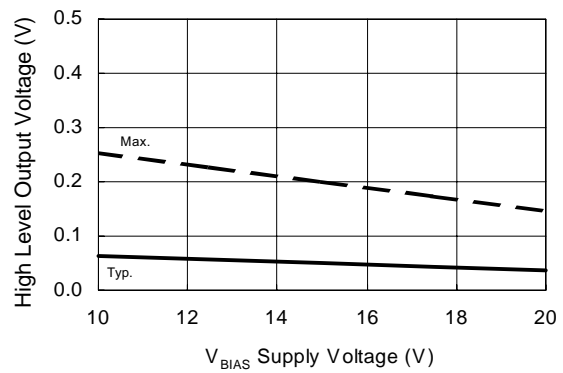
**Figure 13A. Logic "0" Input Voltage vs. Temperature**



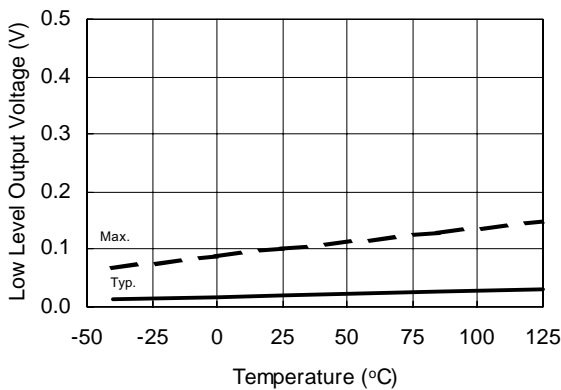
**Figure 13B. Logic "0" Input Voltage vs. Supply Voltage**



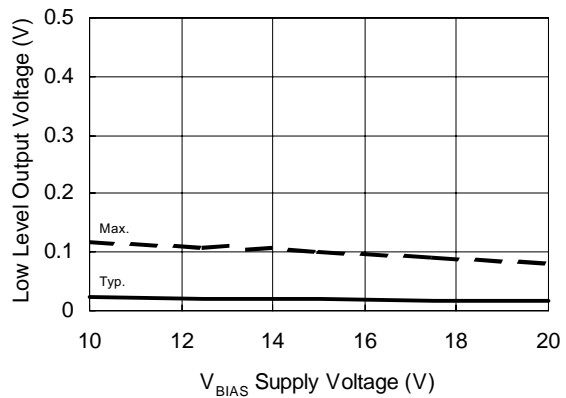
**Figure 14A. High Level Output Voltage vs. Temperature**



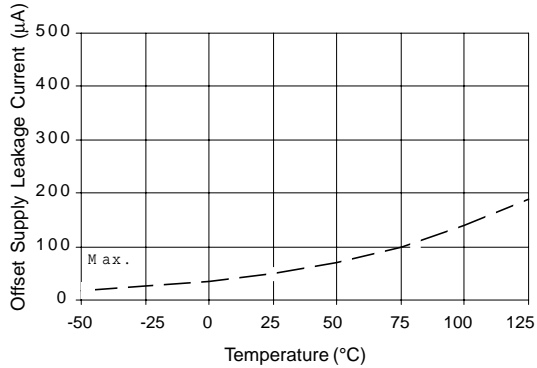
**Figure 14B. High Level Output vs. Supply Voltage**



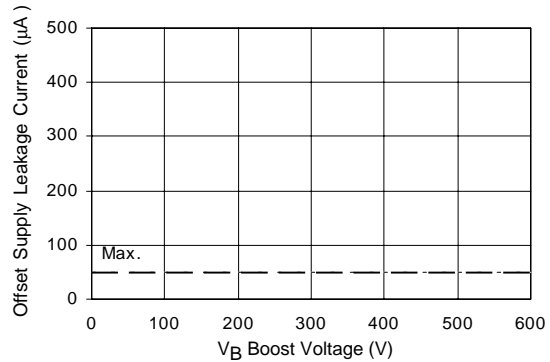
**Figure 15A. Low Level Output Voltage vs. Temperature**



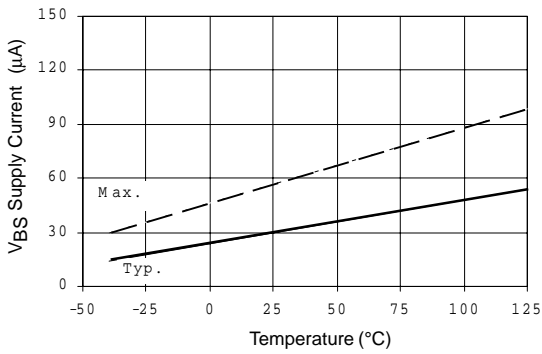
**Figure 15B. Low level Output vs. Supply Voltage**



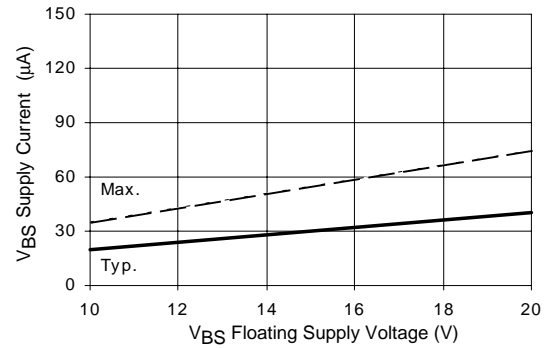
**Figure 16A. Offset Supply Current vs. Temperature**



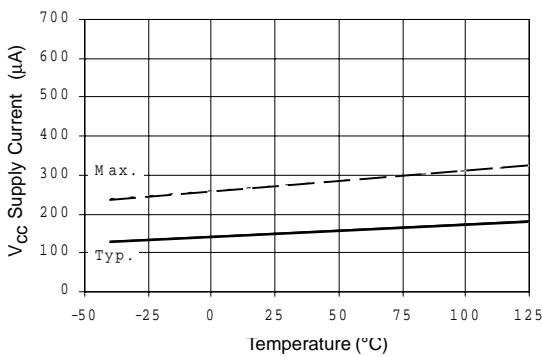
**Figure 16B. Offset Supply Current vs. Voltage**



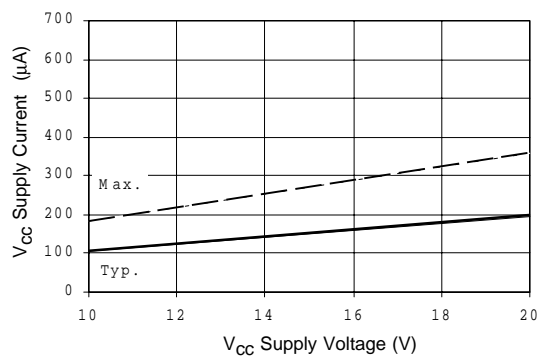
**Figure 17A. V<sub>BS</sub> Supply Current vs. Temperature**



**Figure 17B. V<sub>BS</sub> Supply Current vs. Voltage**

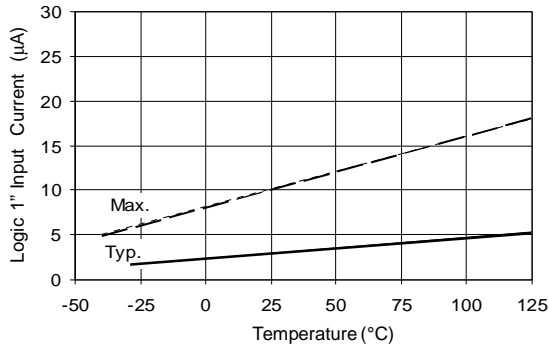


**Figure 18A. V<sub>CC</sub> Supply Current vs. Temperature**

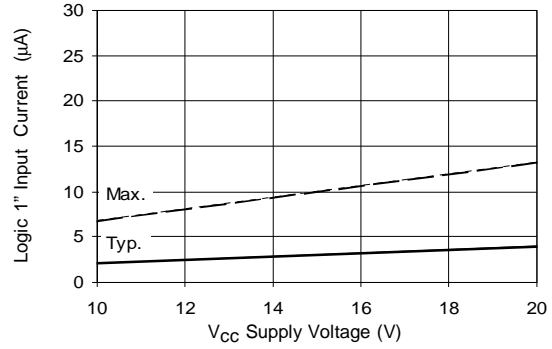


**Figure 18B. V<sub>CC</sub> Supply Current vs. Voltage**

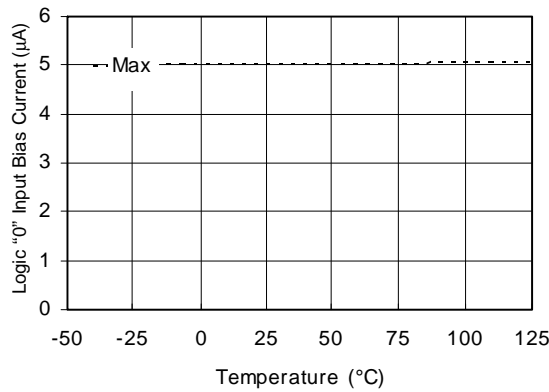
# IRS2001(S)PbF



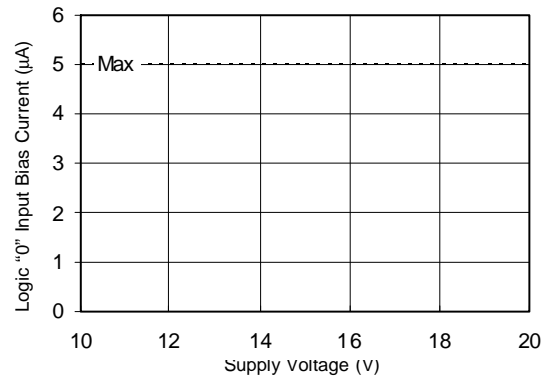
**Figure 19A. Logic "1" Input Current vs. Temperature**



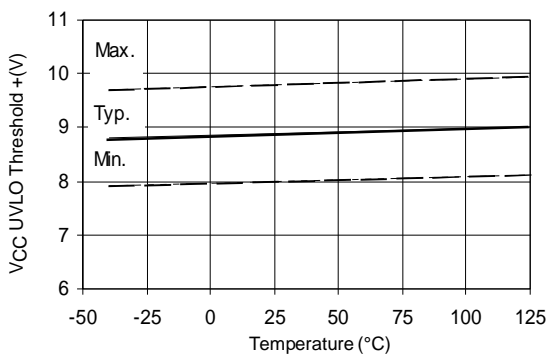
**Figure 19B. Logic "1" Input Current vs. Voltage**



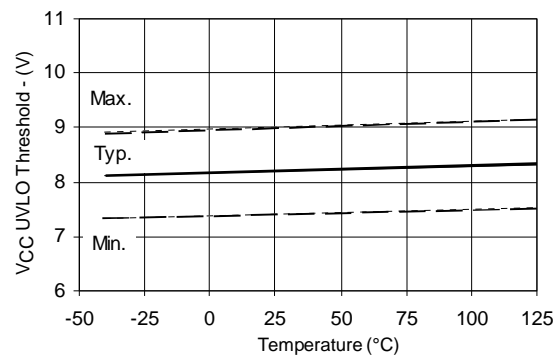
**Figure 20A. Logic "0" Input Bias Current vs. Temperature**



**Figure 20B. Logic "0" Input Bias Current vs. Voltage**

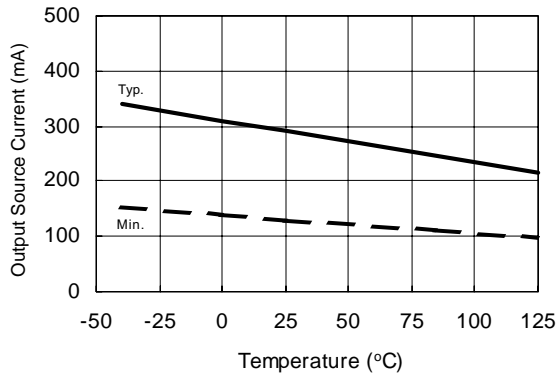


**Figure 21A. V<sub>CC</sub> Undervoltage Threshold(+) vs. Temperature**

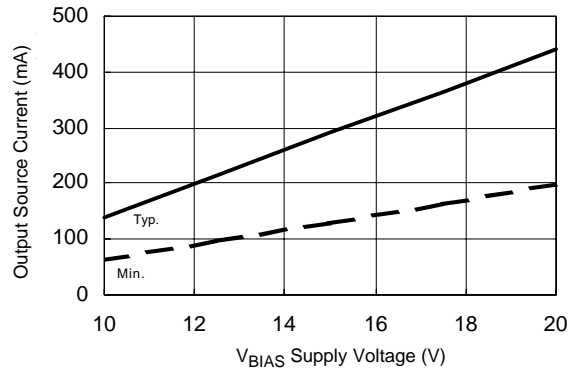


**Figure 21B. V<sub>CC</sub> Undervoltage Threshold(-) vs. Temperature**

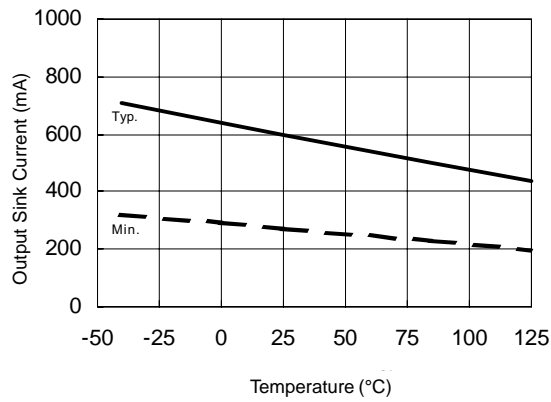
# IRS2001(S)PbF



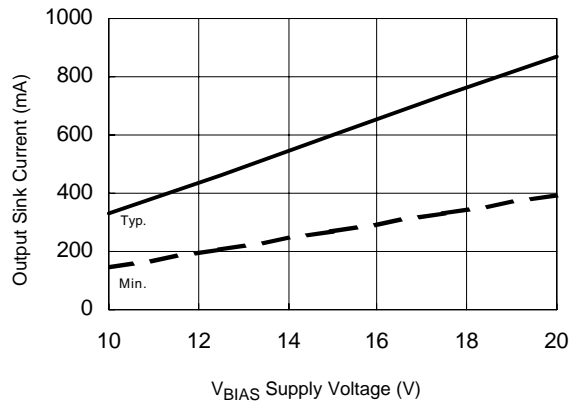
**Figure 22A. Output Source Current vs. Temperature**



**Figure 22B. Output Source Current vs. Supply Voltage**

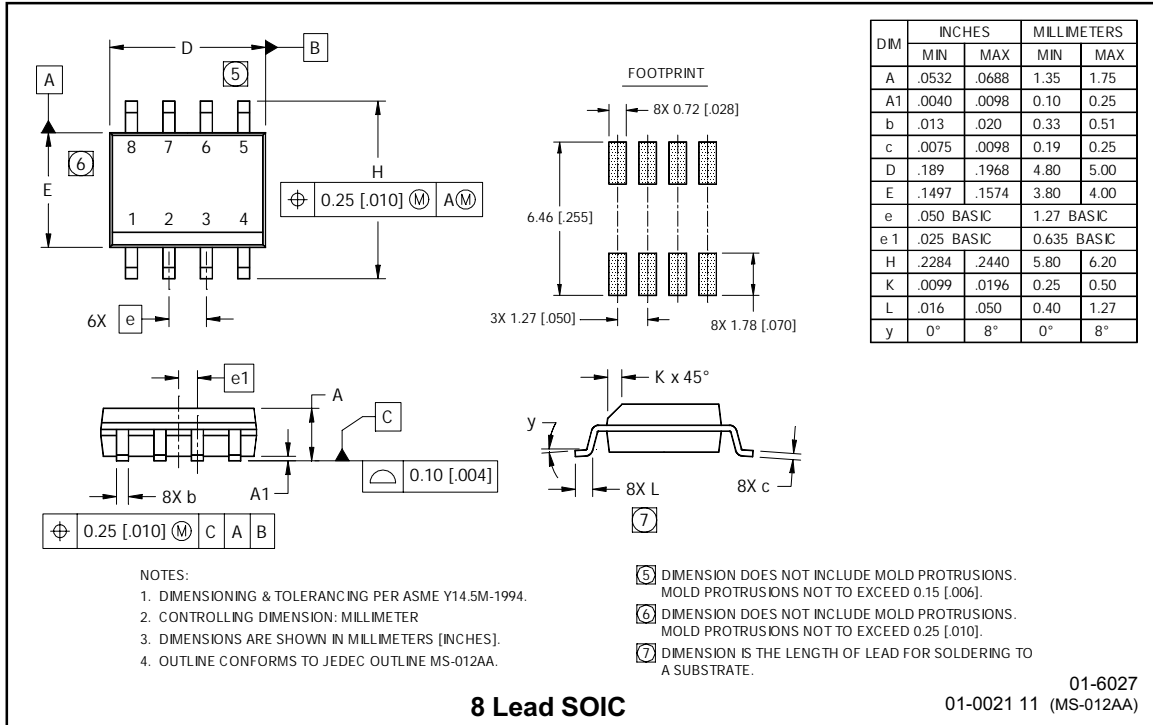
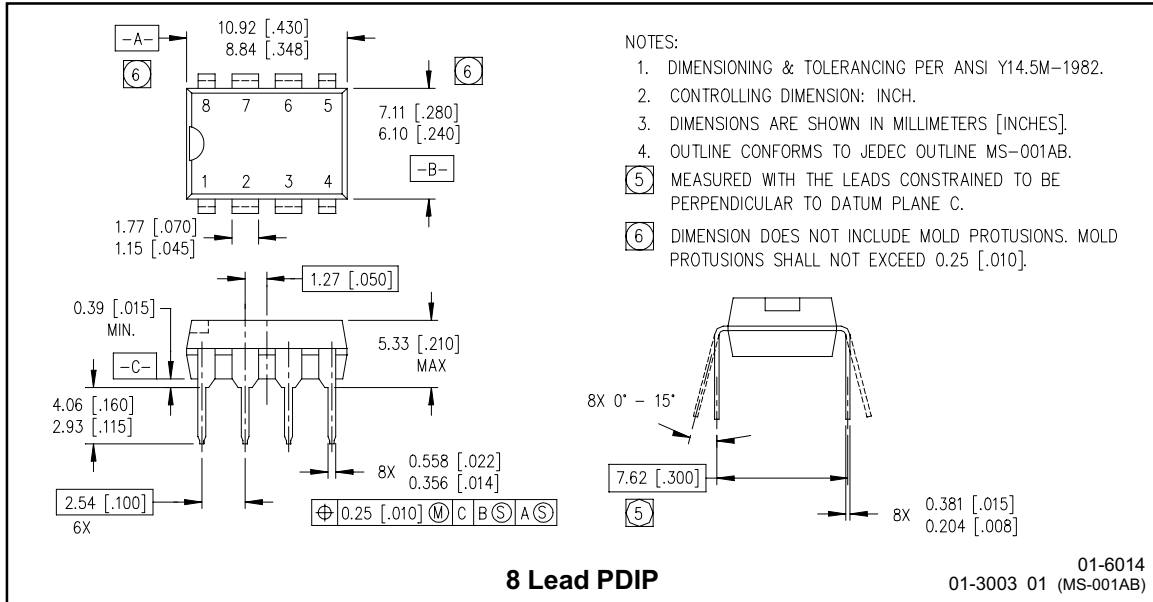


**Figure 23A. Output Sink Current vs. Temperature**



**Figure 23B. Output Sink Current vs. Supply Voltage**

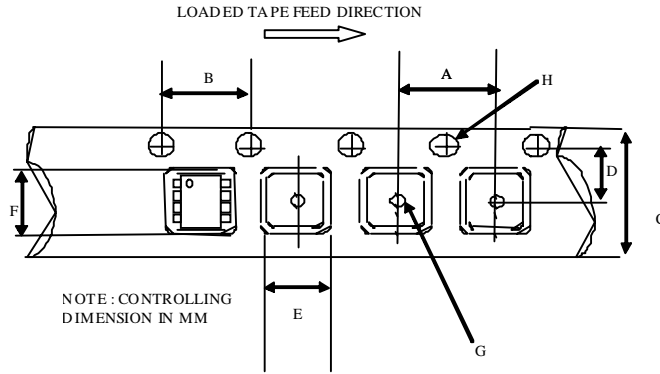
## Case Outlines



International  
**IR** Rectifier

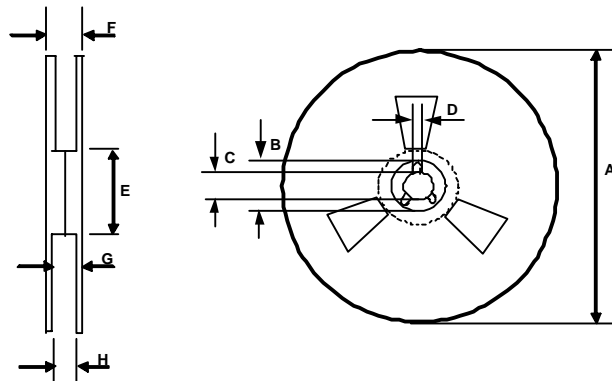
# IRS2001(S)PbF

**Tape & Reel**  
**8-lead SOIC**



CARRIER TAPE DIMENSION FOR 8SOICN

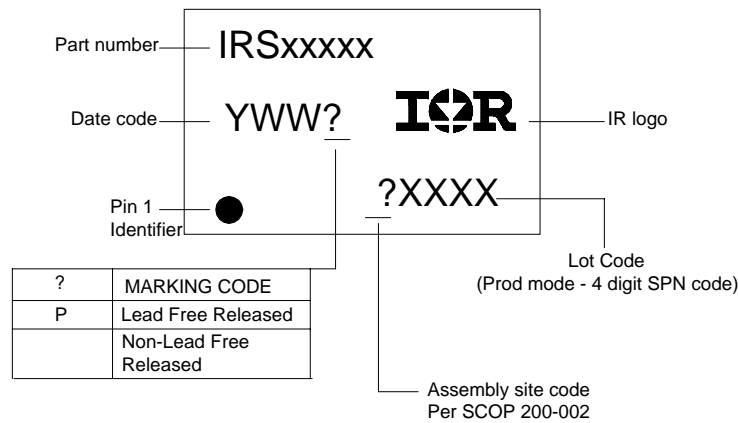
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

## LEADFREE PART MARKING INFORMATION



## ORDER INFORMATION

- 8-Lead PDIP IRS2001PbF
- 8-Lead SOIC IRS2001SPbF
- 8-Lead SOIC Tape & Reel IRS2001STRPbF

单击下面可查看定价，库存，交付和生命周期等信息

[>>Infineon Technologies\(英飞凌\)](#)