

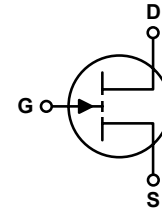
INN100W032A

1. General description

GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in Solder Bar WLCSP with 3.5 mm x 2.13 mm package size.

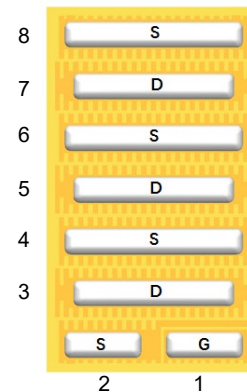
2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small package size
- Zero reverse recovery charge



3. Applications

- Synchronous rectification
- Class-D audio
- High frequency DC-DC converter
- Communication base station
- Motor driver



Bottom View

4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max} @ V_{GS} = 5\text{ V}$	3.2	$m\Omega$
$Q_{G,typ} @ V_{DS} = 50\text{ V}$	9.2	nC
$I_{DS,Pulse}$	230	A
$Q_{OSS} @ V_{DS} = 50\text{ V}$	50	nC

5. Pin information

Table 2 Pin information

PIN	Pin Description	Pin Function
2,4,6,8	Source	Power Source
3,5,7	Drain	Power Drain
1	Gate	Driver Gate

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100W032A	WLCSP 3.5x2.13	J16

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6. Maximum ratings

at $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
I_D	Continuous current	60	A
	Pulsed ($25\text{ }^\circ\text{C}$, $T_{PULSE} = 300\text{ }\mu\text{s}$)	230	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	$^\circ\text{C}$

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	1.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ¹	33	°C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{DSS}	Drain-to-Source Voltage	100	-	-	V	$V_{GS} = 0\text{ V}, I_D = 400\text{ }\mu\text{A}$
I_{DSS}	Drain Source Leakage	-	4	28	μA	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$
I_{GSS}	Gate-to-Source Forward Leakage(25°C)	-	1.2	23	μA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Forward Leakage(125°C)	-	0.1	2	mA	$V_{GS} = 5\text{ V}$
	Gate-to-Source Reverse Leakage	-	0.1	0.5	μA	$V_{GS} = -4\text{ V}$
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	$V_{DS} = V_{GS}, I_D = 9\text{ mA}$
$R_{DS(on)}$	Drain-Source On-state Resistance	-	2.5	3.2	m Ω	$V_{GS} = 5\text{ V}, I_D = 25\text{ A}$
V_{SD}	Source-Drain Forward Voltage	-	1.5	-	V	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{ISS}	Input Capacitance	-	1000	-	pF	V _{GS} = 0 V, V _{DS} = 50 V
C _{OSS}	Output Capacitance	-	460	-		V _{GS} = 0 V, V _{DS} = 50 V
C _{RSS}	Reverse Transfer Capacitance	-	8.2	-		V _{GS} = 0 V, V _{DS} = 50 V
C _{OSS(ER)}	Energy Related C _{OSS}	-	700	-		V _{GS} = 0 V, V _{DS} = 0 V to 50 V
C _{OSS(TR)}	Time Related C _{OSS}	-	1020	-		V _{GS} = 0 V, V _{DS} = 0 V to 50 V
R _G	Gate resistance	-	2.2	-	Ω	f = 5 MHz, open drain
Q _G	Total Gate Charge ¹	-	9.2	12	nC	V _{GS} = 5 V, V _{DS} = 50 V, I _D = 25 A
Q _{GS}	Gate to Source Charge	-	1.9	-		V _{DS} = 0 V to 50 V, I _D = 25 A
Q _{GD}	Gate to Drain Charge	-	1.7	-		V _{DS} = 0 V to 50 V, I _D = 25 A
Q _{G(TH)}	Gate Charge at Threshold	-	1.1	-		V _{DS} = 0 V to 50 V, I _D = 25 A
Q _{OSS}	Output Charge	-	50	-		V _{GS} = 0 V, V _{DS} = 0 V to 50 V

Note 1: Guarantee by design.

9. Electric characteristics diagrams

at $T_J = 25^\circ\text{C}$ unless otherwise specified.

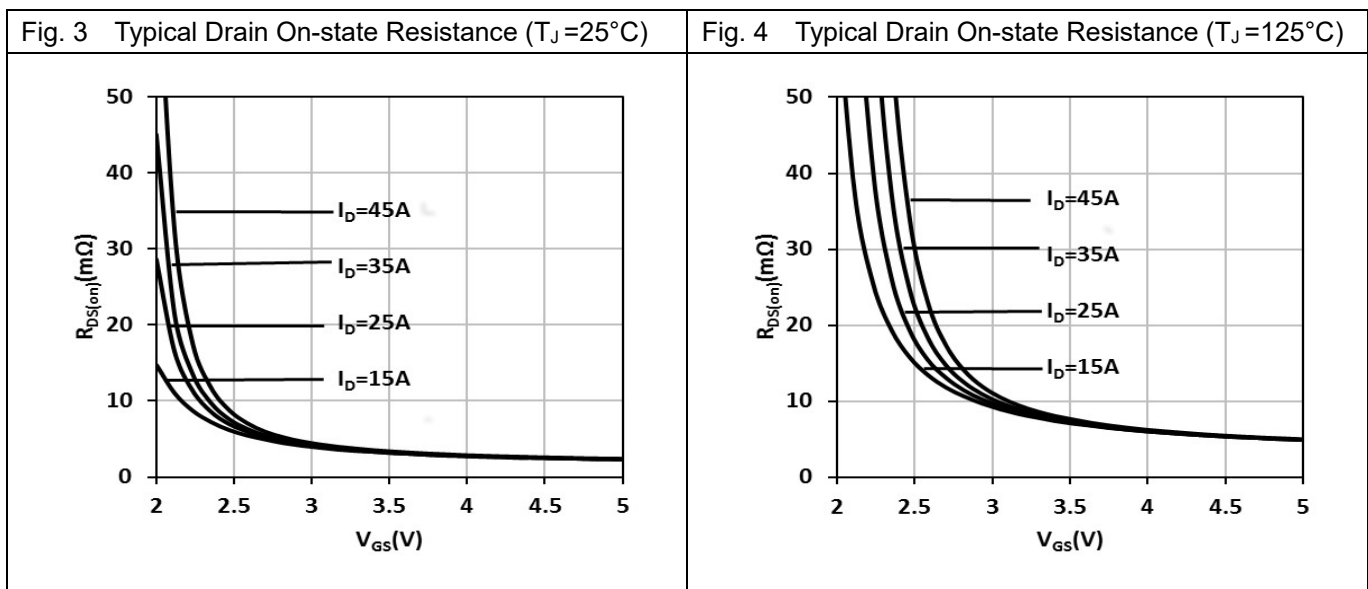
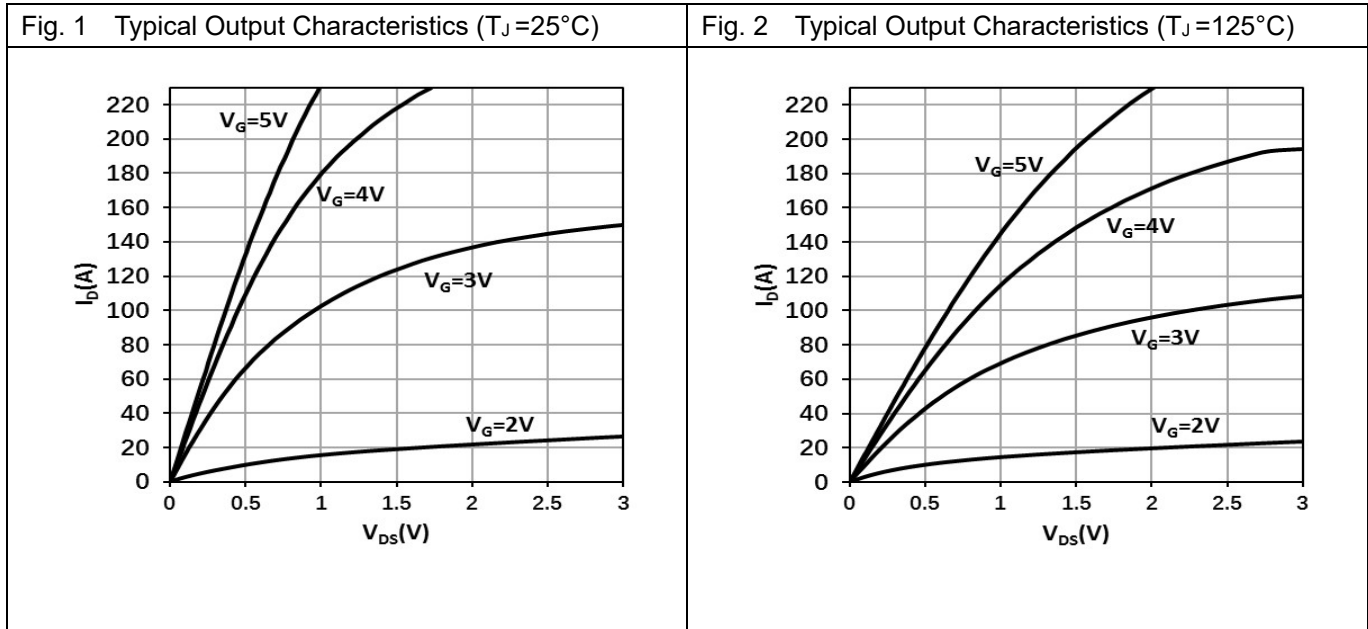


Fig. 5 Normalized On-State Resistance vs. Temp.

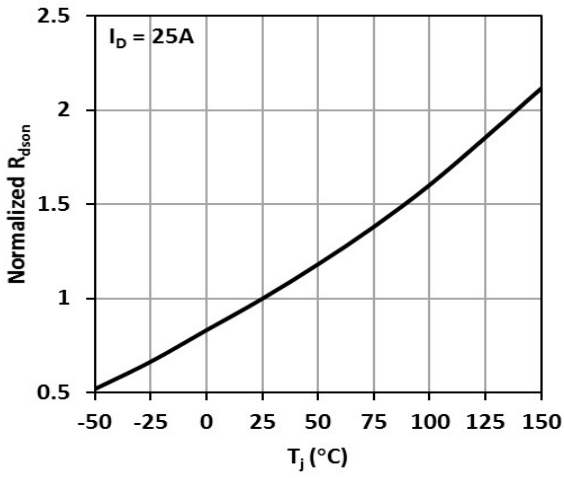


Fig. 6 Typical Transfer Characteristics

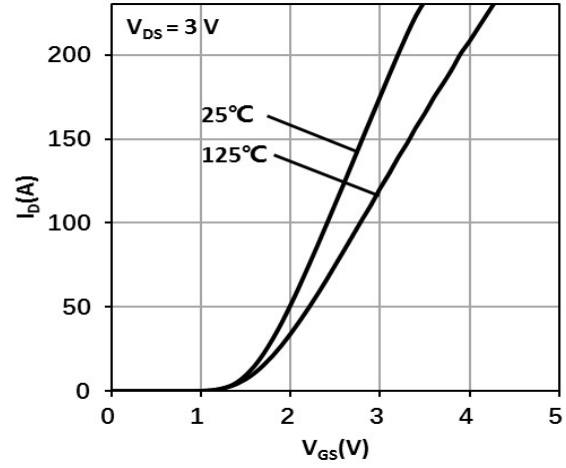


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0, T_J = 25^\circ C$)

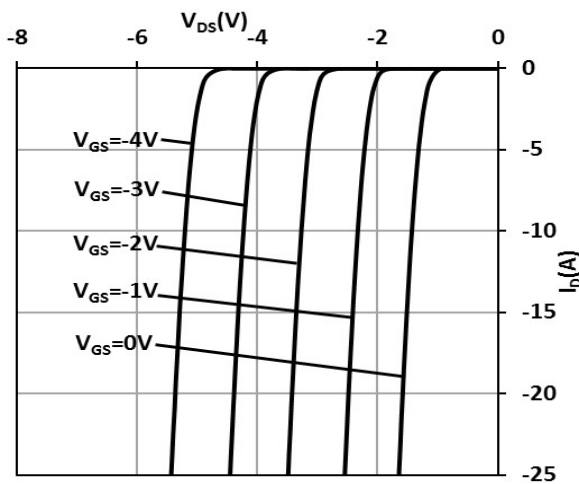


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0, T_J = 25^\circ C$)

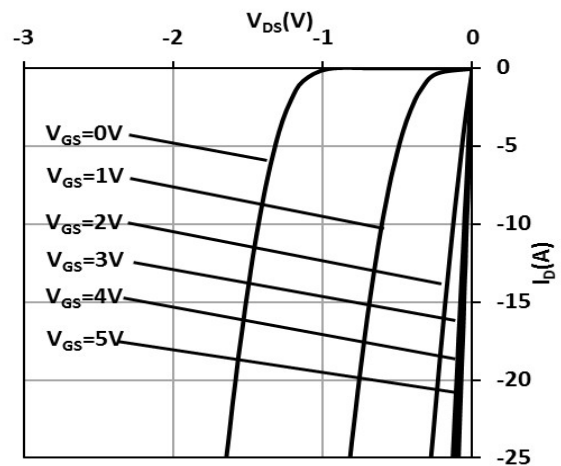


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS} \leq 0$, $T_J = 125^\circ\text{C}$)

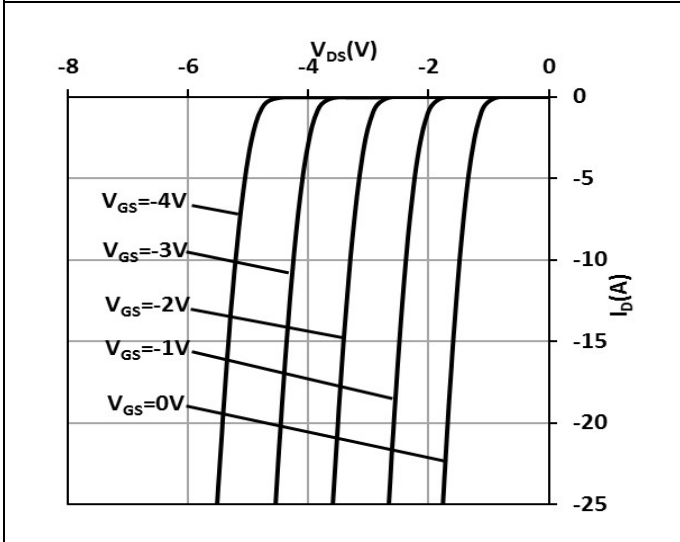


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS} \geq 0$, $T_J = 125^\circ\text{C}$)

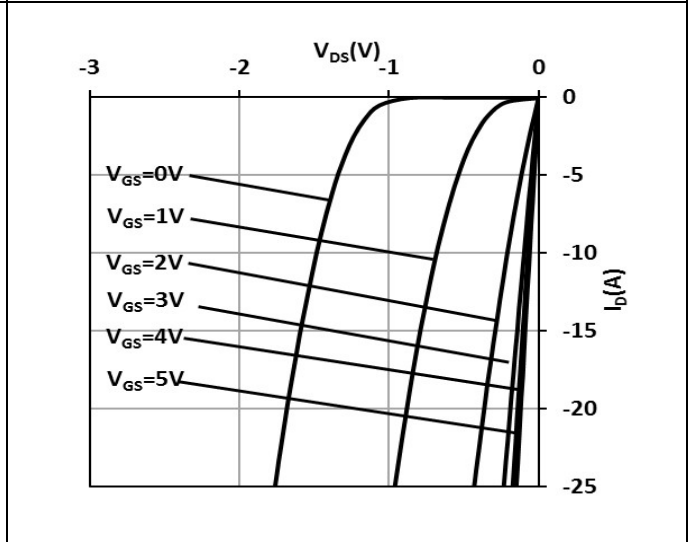


Fig. 11 Typ. Capacitances Characteristics

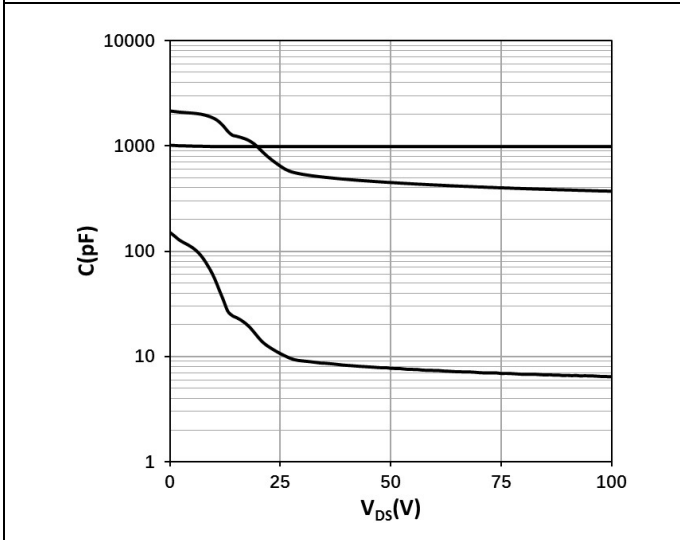


Fig. 12 Typ. Gate Charge

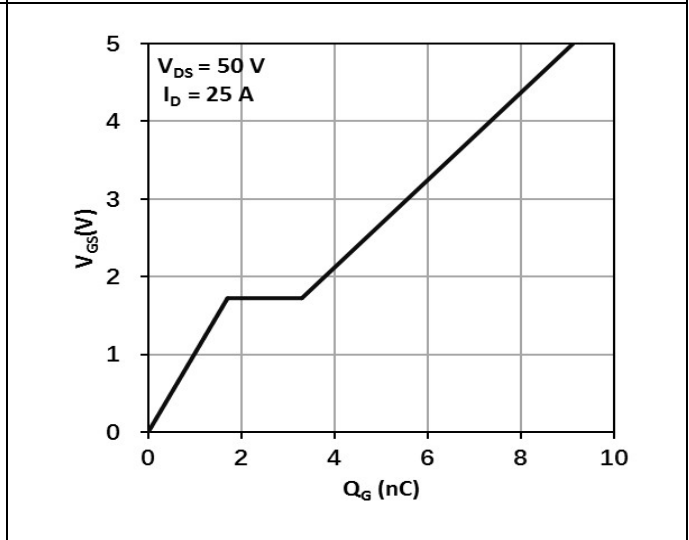


Fig. 13 Normalized Threshold Voltage vs. Temp.

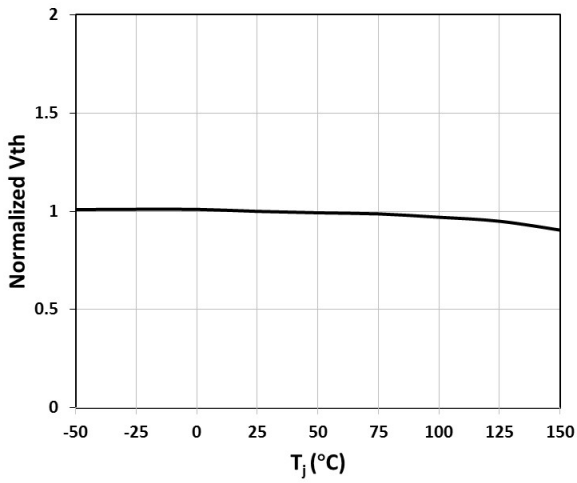


Fig. 14 Output Charge

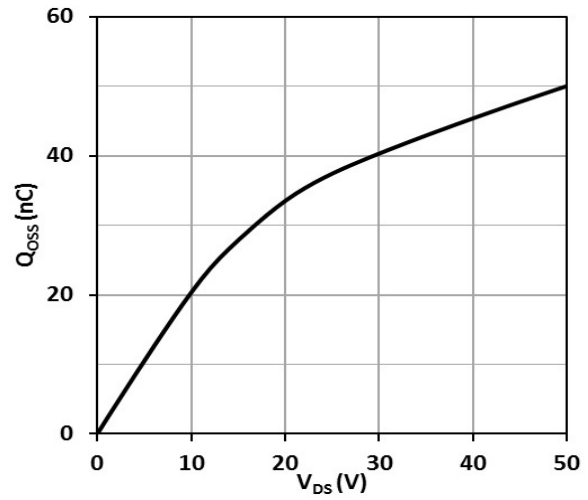


Fig. 15 Output Capacitance Stored Energy

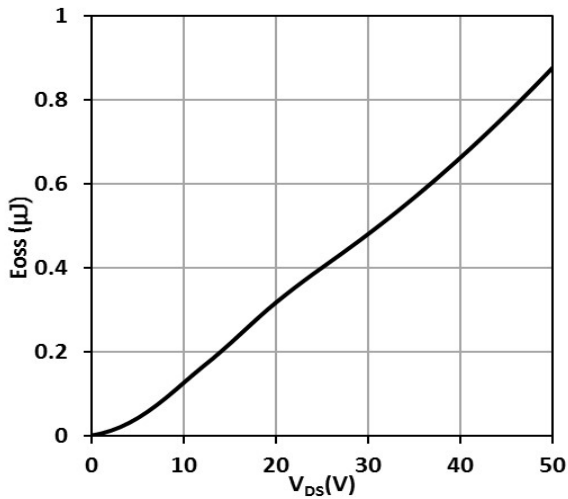


Fig. 16 Power Dissipation

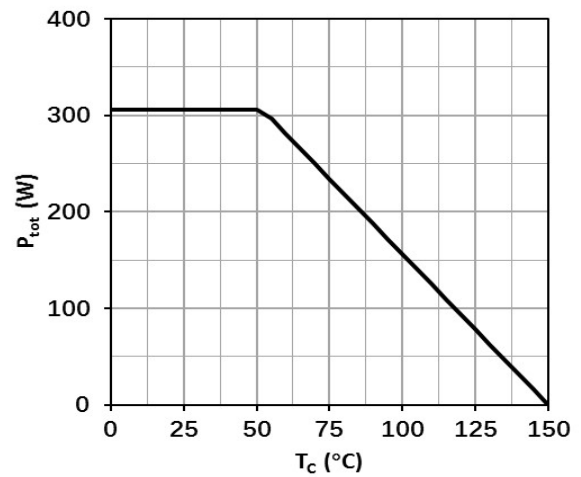


Fig. 17 Safe Operating Area

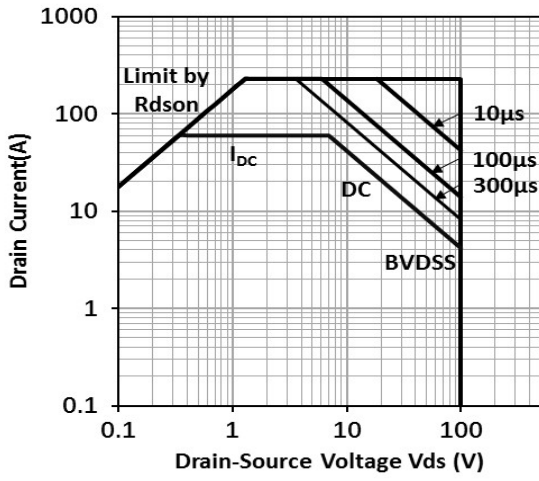
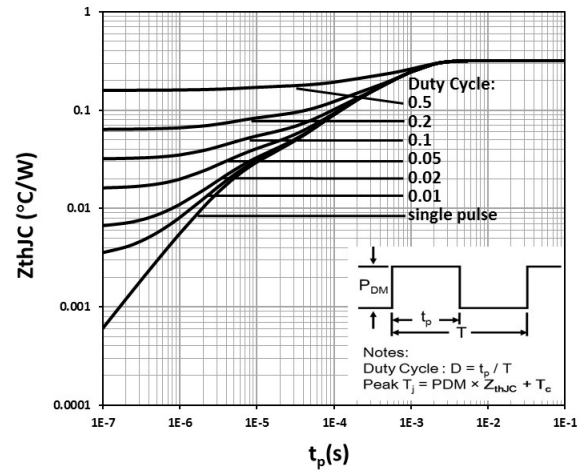
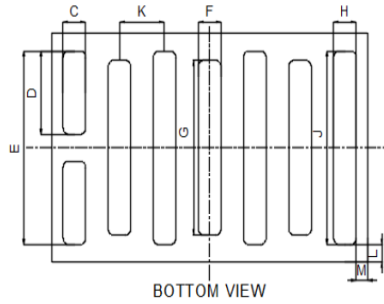
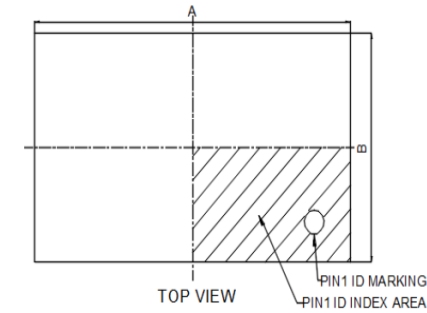


Fig. 18 Max. Transient Thermal Impedance

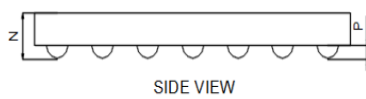


10. Package outlines

Package Reference



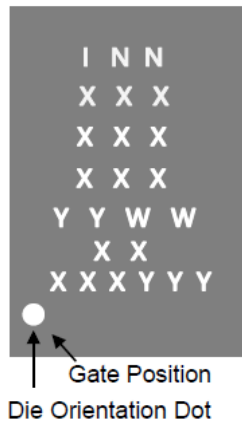
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
A	3.475	3.5	3.525	
B	2.105	2.13	2.155	
C	0.23	0.25	0.27	2X
D	0.755	0.775	0.795	2X
E	1.78	1.8	1.82	
F	0.23	0.25	0.27	3X
G	1.605	1.625	1.645	3X
H	0.23	0.25	0.27	3X
J	1.78	1.8	1.82	3X
K	0.5 BASIC			7X
L	0.165 REF			
M	0.125 REF			
N	0.394	0.429	0.464	
P	0.1	0.12	0.14	



NOTE:

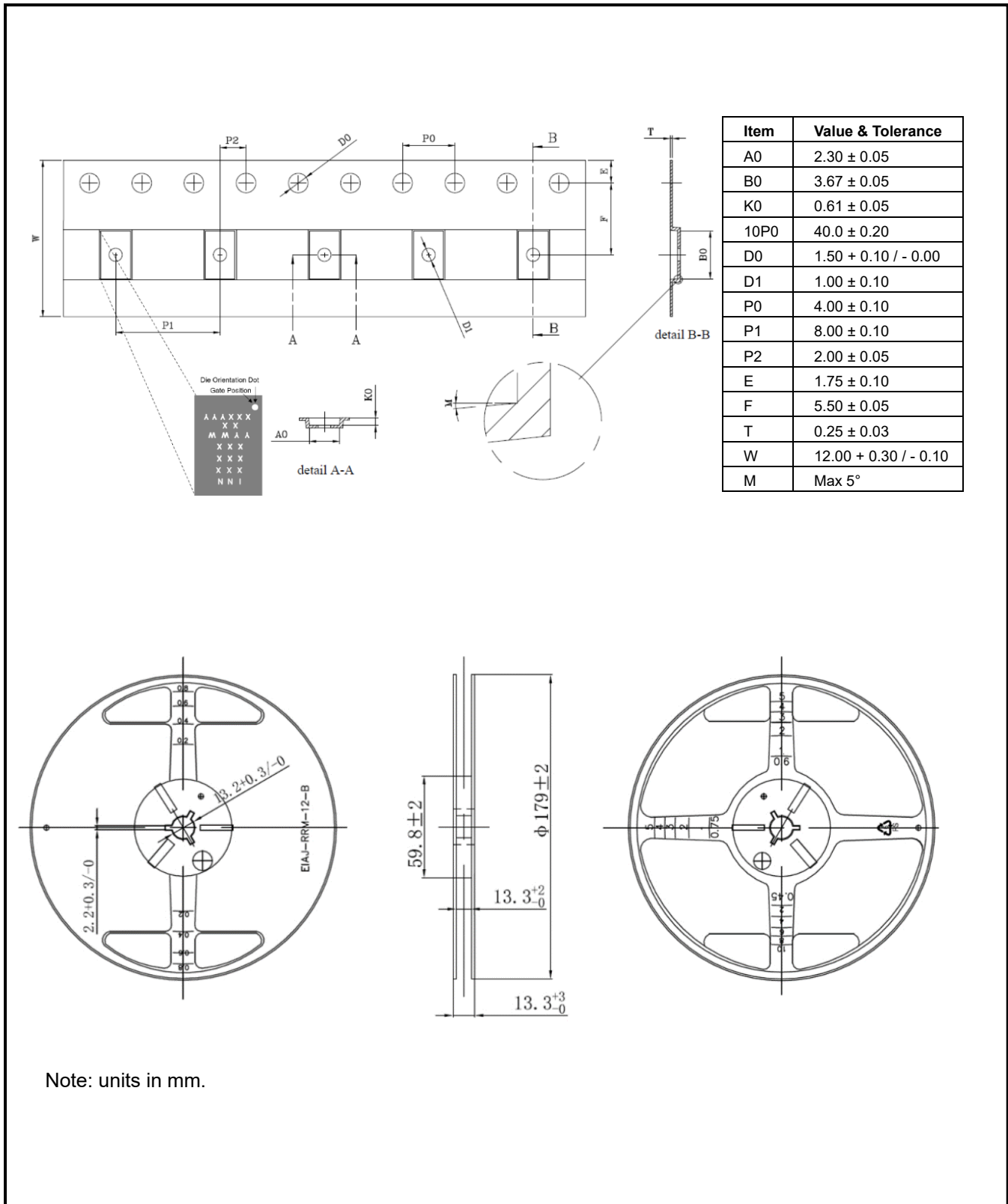
- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) BOTTOM VIEW IS SOLDER BAR VIEW.
- 3) COMPLIES WITH JEDEC MO-211.
- 4) DRAWING IS NOT TO SCALE.
- 5) A, B IS PACKAGE SIZE
- 6) BAR COPLANARITY SHALL BE 0.05 MILLIMETERS MAX

Marking Reference:



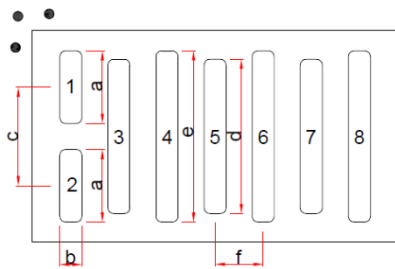
Row	Description	Example
Row1	Company name	INN
Row2	Product code	XXX
Row3	Lot Code	XXX
Row4		XXX
Row5	Date code	YYWW
Row6	Wafer ID	XX
Row7	Location ID	XXXYYY

11. Reel information



12. Land Pattern

Recommended Land Pattern
Top View

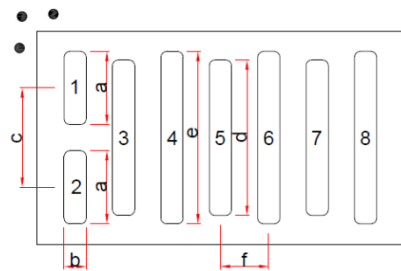


Land pattern is solder mask defined
Solder mask opening is 0.23mm
It is recommended to have on-Cu trace PCB vias

DIM	Millimeter
a	0.775
b	0.250
c	1.025
d	1.605
e	1.780
f	0.500

Pad 1 is Gate;
Pads 2 ,4, 6, 8 are Source;
Pads 3, 5, 7 are Drain;

Recommended Stencil Drawing
Top View



DIM	Millimeter
a	0.775
b	0.230
c	1.025
d	1.605
e	1.780
f	0.500

Pad 1 is Gate;
Pads 2 ,4, 6, 8 are Source;
Pads 3, 5, 7 are Drain;

13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-08-09	1.0 Version Setup
1.1	2023-03-14	1.1 Update Product Code & R _G Test Condition

Important Notice

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