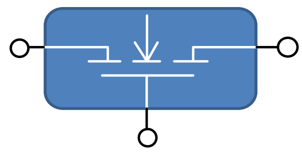
INN040W048A

1. General description

Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) based on advanced low voltage BiGaN Technology with ultra-low on resistance.

2. Features

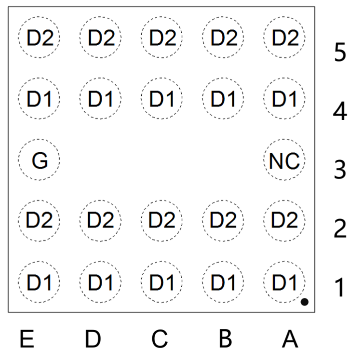


- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on Resistance

3. Applications

- High side load switch
- OVP protection in smart phone USB port
- Switch circuits in multiple power suppliers system

Top view



4. Key performance parameters

Table 1 Key performance parameters at T_j = 25 °C

Parameter	Value	Unit
$V_{DD, max}$	40	V
$R_{DD(on),max}$ @ V_G = 5 V	4.8	mΩ
$Q_{G, typ}$ @ V_{DD} = 20 V	15.8	nC
$I_{D, DC}$	20	A

5. Pin information

Table 2 Pin information

Pin	Pin description	Pin function
A~E1, A~E4	Drain1	Power Drain1
A~E2, A~E5	Drain2	Power Drain2
E3	Gate	Driver Gate
A3	Not Connected	Dummy Pin

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN040W048A	WLCSP 2.1x2.1	D12

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6. Maximum ratings

at T_j = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DD}	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	40	V
V_{DG}	Drain-to-Gate Voltage	40	V
V_{GD}	Gate-to-Drain Voltage	6	V
I_D	Continuous Drain current	20	A
I_{DM}	Pulsed Drain Current (25°C, T_{Pulse} = 300 µs)	100	A
T_J	Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-40 to 150	°C

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction to Case	12.6	˚C/W
$R_{\theta JB}$	Thermal Resistance, Junction to Board	7.3	˚C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [1]	59.3	˚C/W

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

8. Electric characteristics

at T_j = 25 °C, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{D1D2S}	Drain1-to-Drain2 Breakdown Voltage	40			V	V_{D2} = V_G = 0 V, I_{D1D2} = 500 µA
BV_{D2D1S}	Drain2-to-Drain1 Breakdown Voltage	40			V	V_{D1} = V_G = 0 V, I_{D2D1} = 500 µA
I_{D1D2S}	Zero Gate Voltage Drain Current			20	µA	V_{D2} = V_G = 0 V, V_{D1} = 40 V
I_{D2D1S}	Zero Gate Voltage Drain Current			20	µA	V_{D1} = V_G = 0 V, V_{D2} = 40 V
I_{GDS} (T_J=85°C)	Gate-to-Drain Leakage		0.5	3	µA	V_{D1} = V_{D2} = 0 V, V_G = 5 V
	Gate-to-Drain Leakage	-30			µA	V_{D1} = V_{D2} = 0 V, V_G = -5 V
I_{GDS} (T_J=85°C)	Gate-to-Drain Leakage		5	30	µA	V_{D1} = V_{D2} = 0 V, V_G = 6 V
	Gate-to-Drain Leakage	-40			µA	V_{D1} = V_{D2} = 0 V, V_G = -6 V
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8		2.4	V	V_{D1} = 0 V, V_{D2} = V_G, I_{D2D1} = 1 mA
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8		2.4	V	V_{D2} = 0 V, V_{D1} = V_G, I_{D1D2} = 1 mA
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance		4	4.8	mΩ	V_{D2} = 0 V, V_{GD} = 5 V, I_{D1D2} = 10 A
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance		4	4.8	mΩ	V_{D1} = 0 V, V_{GD} = 5 V, I_{D2D1} = 10 A

Table 7 Dynamic characteristics

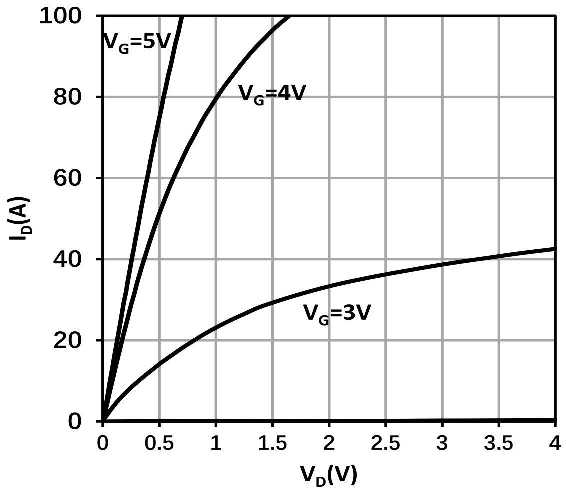
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance		886.5		pF	V_G = 0 V, V_D = 20 V
C_{OSS}	Output Capacitance		381.2			
C_{RSS}	Reverse Transfer Capacitance		226.4			
R_G	Gate Resistance		4.1		Ω	f = 1 MHz
Q_G	Total Gate Charge		15.8		nC	V_D = 20 V, V_G = 5 V, I_D = 10 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D2D1}=20V)		1.9			V_{D1} = 0, V_{D2} = 20 V, I_{D2D1} = 10 A
Q_{GD1}	Gate-to-Drain1 Charge (V_{D1D2}=20V)		8.6			V_{D2} = 0, V_{D1} = 20 V, I_{D1D2} = 10 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D1D2}=20V)		1.9			V_{D2} = 0, V_{D1} = 20 V, I_{D1D2} = 10 A
Q_{GD2}	Gate-to-Drain2 Charge (V_{D2D1}=20V)		8.6			V_{D1} = 0, V_{D2} = 20 V, I_{D2D1} = 10 A
Q_{OSS}	Output Charge		12.2			V_G = 0 V, V_D = 20 V

9. Electric characteristics diagrams

at T_j = 25 °C, unless specified otherwise

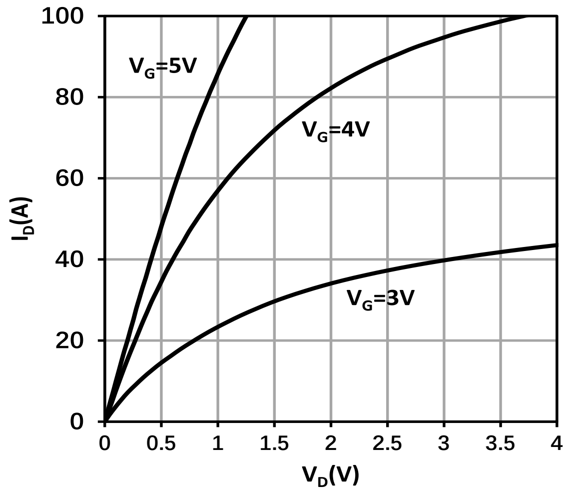
Note: The device characteristics with D1 as drain and D2 as source is the same with D2 as drain and D1 as source.

Figure 1 Typical Output Characteristics



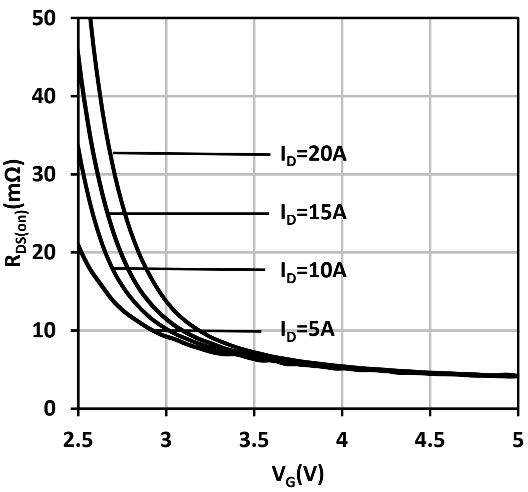
$I_D = f(V_D, V_G)$; T_J = 25 °C

Figure 2 Typical Output Characteristics



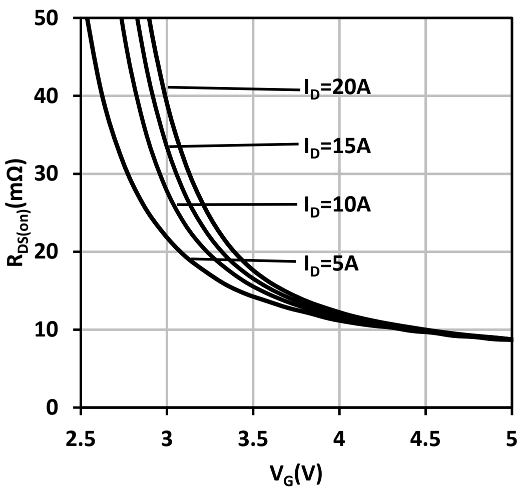
$I_D = f(V_D, V_G)$; T_J = 125 °C

Figure 3 Typical Drain On-state Resistance



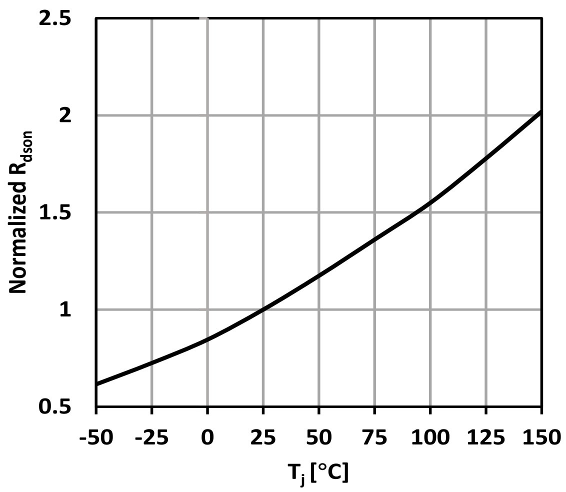
$R_{D(on)} = f(V_G, I_D)$; T_J = 25 °C

Figure 4 Typical Drain On-state Resistance



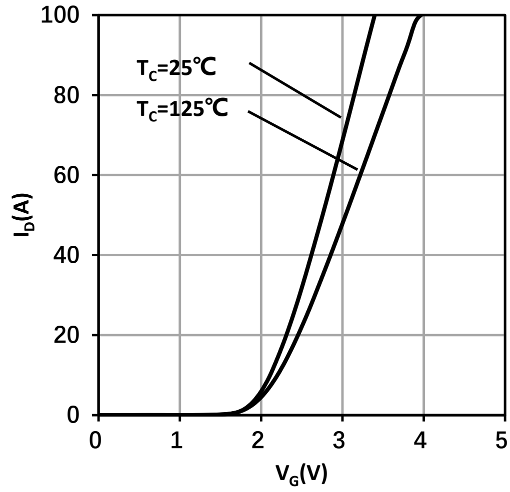
$R_{D(on)} = f(V_G, I_D)$; T_J = 125 °C

Figure 5 Typical On Resistance vs. Temperature



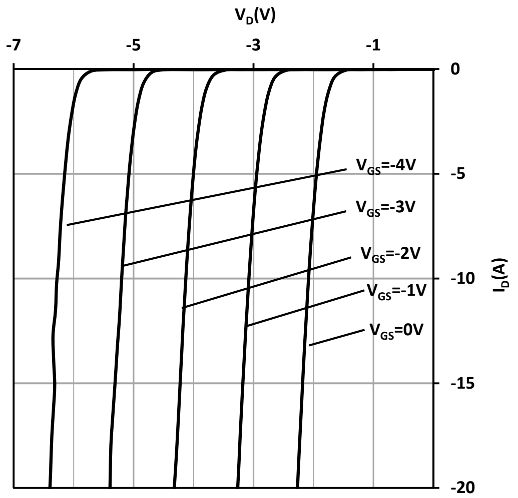
Normalized $R_{D(on)} = f(T_J)$; I_D = 10 A

Figure 6 Typical Transfer Characteristics



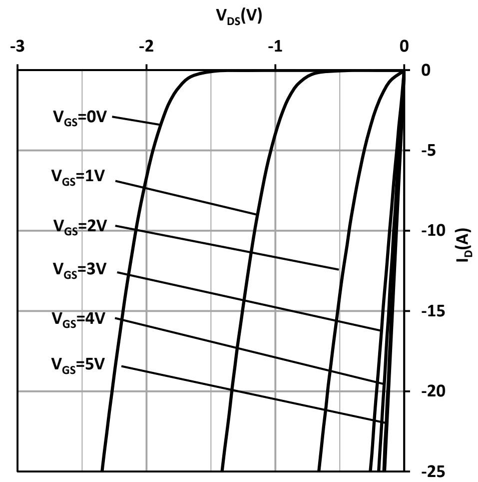
$I_D = f(V_G)$; V_D = 3 V

Fig. 7 Typ. Reverse Drain-Source Characteristics



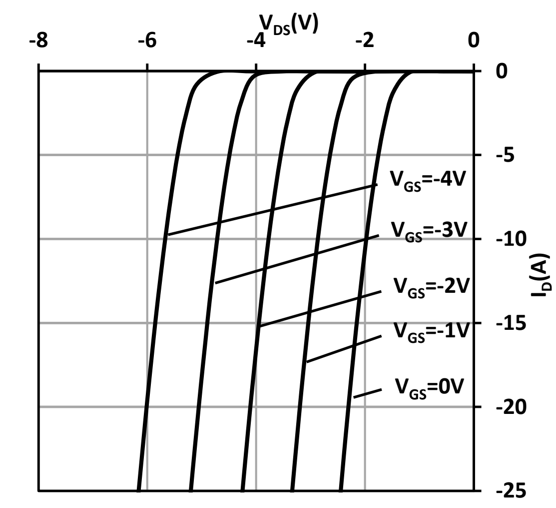
$I_D = f(V_D, V_G)$; T_J = 25 °C

Fig. 8 Typ. Reverse Drain-Source Characteristics



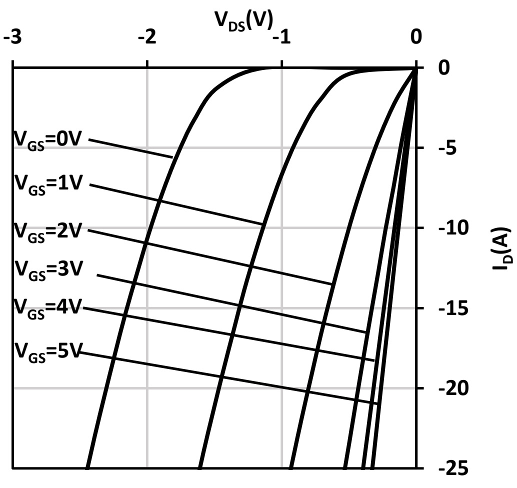
$I_D = f(V_D, V_G)$; T_J = 25 °C

Fig. 9 Typ. Reverse Drain-Source Characteristics



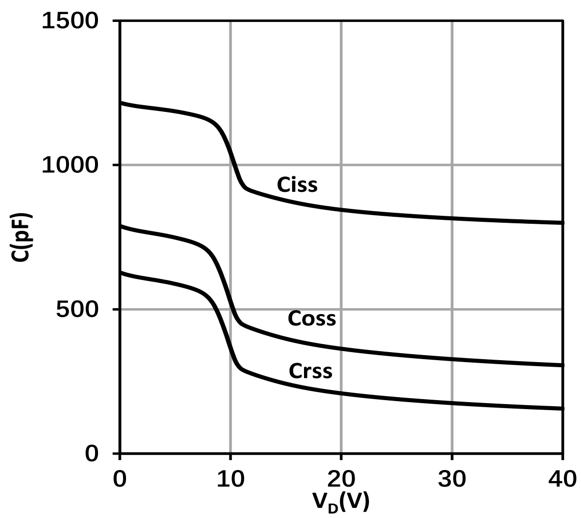
$I_D = f(V_D, V_G)$; T_J = 125 °C

Fig. 10 Typ. Reverse Drain-Source Characteristics



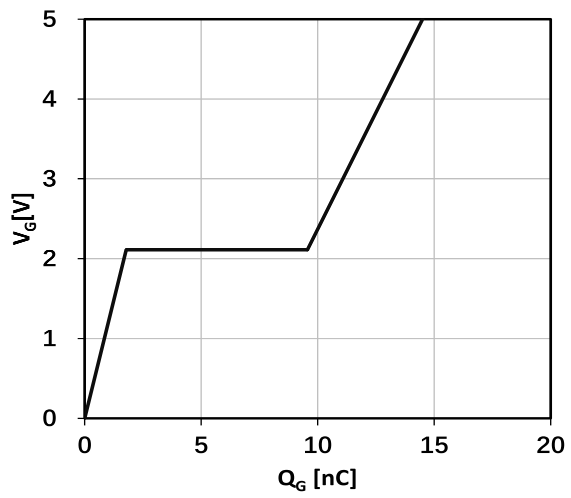
$I_D = f(V_D, V_G)$; T_J = 125 °C

Fig. 11 Typ. Capacitances Characteristics



$C_{XSS} = f(V_D)$; f = 1 MHz

Fig. 12 Typ. Gate Charge



$V_G = f(Q_G)$; V_D = 20 V; I_D = 10 A

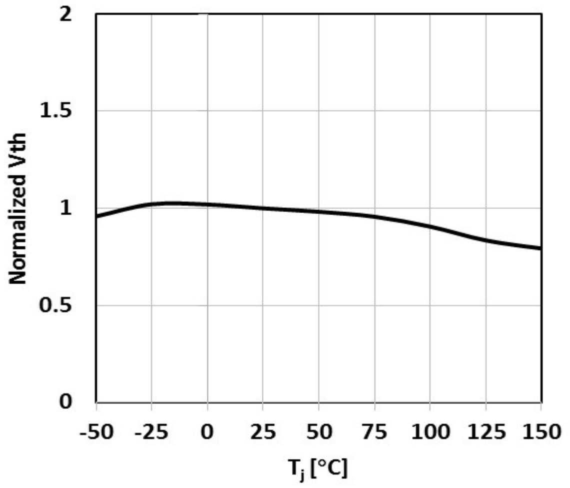
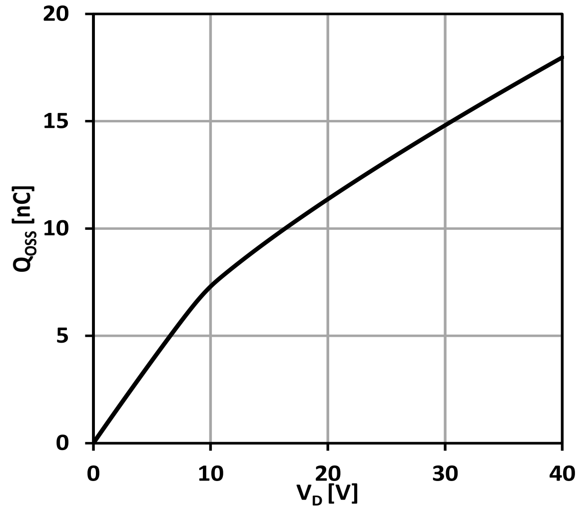
Fig. 13 Normalized Threshold Voltage vs. Temp.	Fig. 14 Output Charge
	
Normalized $V_{TH} = f(T_J)$; $V_G = V_D$; I_D = 1 mA	$Q_{oss} = f(V_D)$

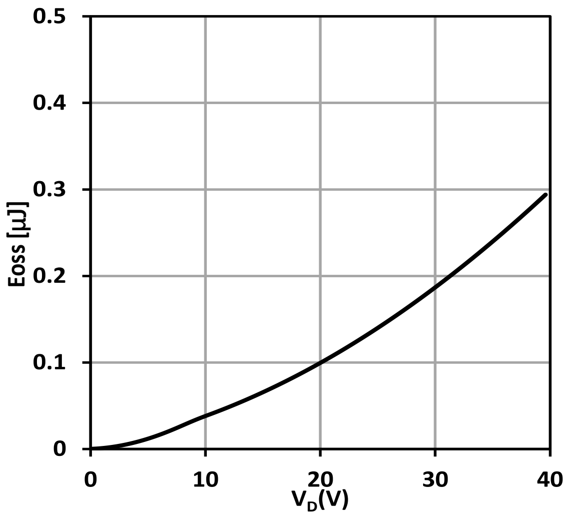
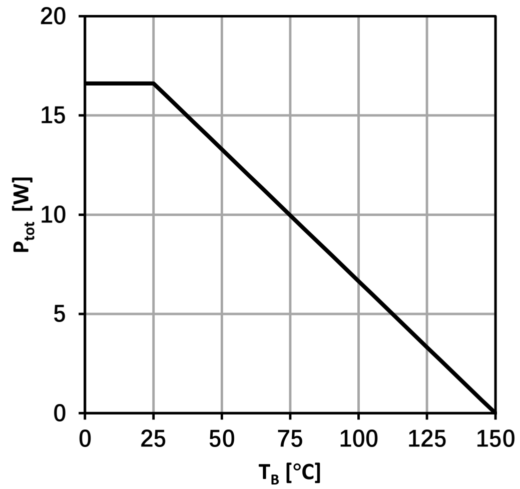
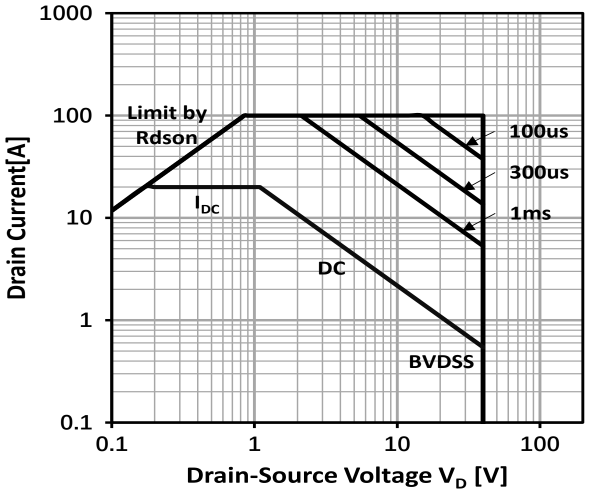
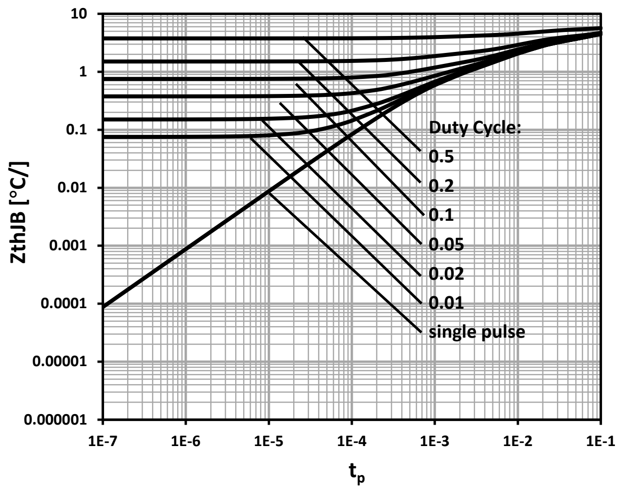
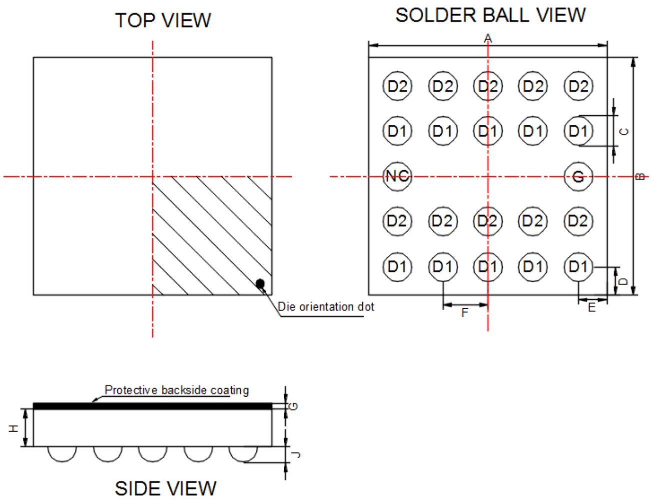
Fig. 15 Output Capacitance Stored Energy	Fig. 16 Power Dissipation
	
$E_{oss} = f(V_D)$	$P_{tot} = f(T_B)$

Fig. 17 Safe Operating Area	Fig. 18 Max. Transient Thermal Impedance
	
$I_D = f(V_D)$; $T_C = 25$ ˚C; Single Pulse	$Z_{\theta JB} = f(t_p)$; parameter: $D = t_p / T$

10. Package outlines

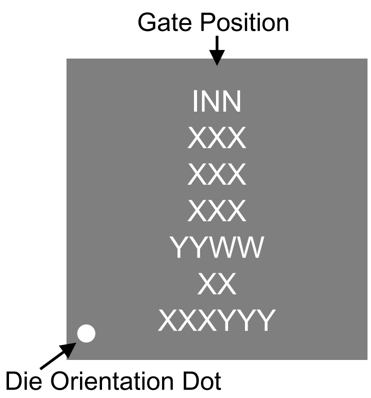
Package Reference



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.075	2.1	2.125
B	2.075	2.1	2.125
C	0.241	0.268	0.295
D	0.25 REF		
E	0.25 REF		
F	0.4 BASIC		
G	0.022	0.025	0.028
H	0.330	0.344	0.358
J	0.165	0.195	0.225

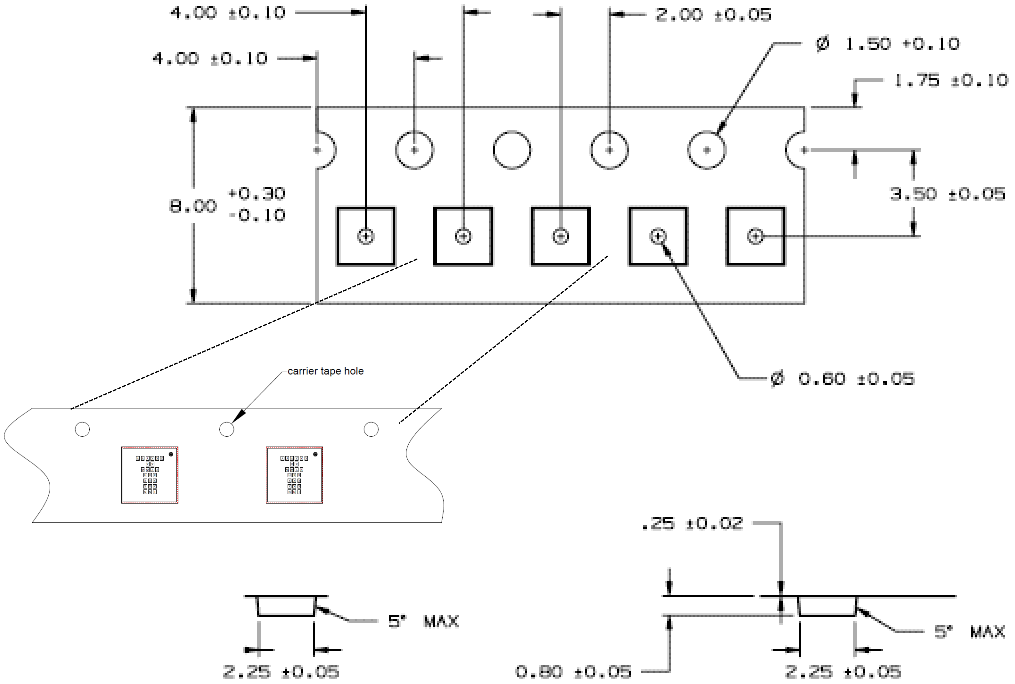
NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BALL COPLANARITY SHALL BE 0.01 MILLIMETERS MAX.
3)COMPLIES WITH JEDEC MO-211.
4)DRAWING IS NOT TO SCALE.

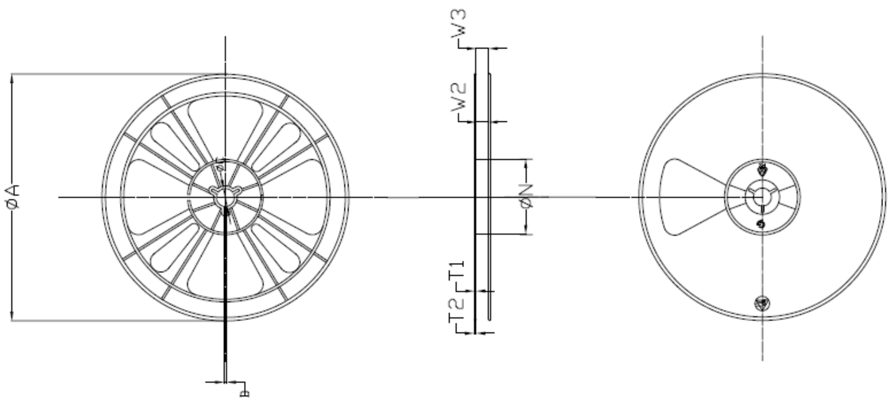
Marking Reference:



Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Lot code	XXX
Row 4		XXX
Row 5	Date code	YYWW
Row 6	Wafer ID	XX
Row 7	Location ID	XXXYYY

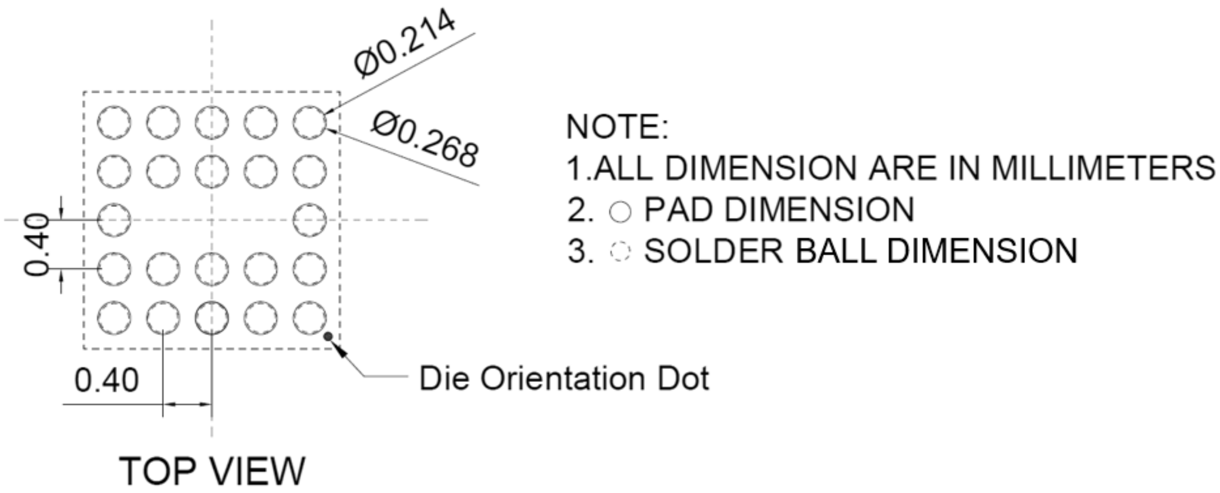
11. Reel information





Item	Value&Tolerance
A	179±1.0
B	2.0±0.2
C	13.5±0.2
N	54.8±0.2
W2	9.0±0.2
W3	9.2+1.0
T1	1.2±0.2
T2	1.5±0.2

12. Land pattern



13. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-04-28	1.0 version release
1.1	2022-06-30	Update land pattern information

Important Notice

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