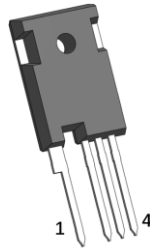


IV3Q12013T4Z- Gen3 1200V 13.5mΩ Automotive SiC MOSFET

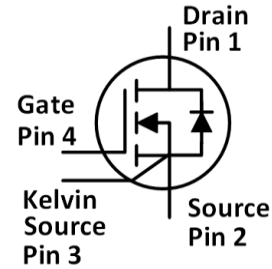
Features

- 3rd Generation SiC MOSFET Technology with +15~+18V gate drive
- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- High operating junction temperature capability
- Very fast, robust and soft-recovery intrinsic body diode
- Kelvin gate input easing driver circuit design
- AEC-Q101 qualified

Outline:



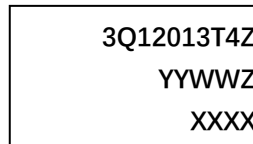
TO247-4



Applications

- EV Motor drivers
- Solar MPPT and inverters
- High voltage DC/DC converters
- Switch mode power supplies

Marking Diagram:



3Q12013T4Z= Specific Device Code
 YY = Year
 WW = Work Week
 Z = Assembly Location
 XXXX = Lot Traceability

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DS}	Drain-Source voltage	1200	V	$V_{GS}=0V, I_D=100\mu A$	
$V_{GSmax}(DC)$	Maximum DC voltage	-5 to 20	V	Static (DC)	
V_{GSmax} (Transient)	Maximum transient voltage	-10 to 23	V	Duty cycle<1%, and pulse width<200ns	
V_{GSon}	Recommended turn-on voltage	15 to 18	V		
V_{GSoff}	Recommended turn-off voltage	-3.5 to -2	V		
I_D	Drain current (continuous)	147	A	$V_{GS}=18V, T_c=25^\circ\text{C}$	Fig. 23
		106	A	$V_{GS}=18V, T_c=100^\circ\text{C}$	
I_{DM}	Drain current (pulsed)	367	A	Pulse width limited by SOA	Fig. 26
I_{SM}	Body diode current (pulsed)	367	A	Pulse width limited by SOA and dynamic $R_{\theta(j-c)}$	Fig. 25 26
P_{TOT}	Total power dissipation	553	W	$T_c=25^\circ\text{C}$	Fig. 24
T_{stg}	Storage temperature range	-55 to 175	$^\circ\text{C}$		
T_j	Operating junction temperature	-55 to 175	$^\circ\text{C}$		
T_L	Solder Temperature	260	$^\circ\text{C}$	wave soldering only allowed at leads, 1.6mm from case for 10 s	

Thermal Data

Symbol	Parameter	Value	Unit	Note
$R_{\theta(j-c)}$	Thermal Resistance from Junction to Case	0.27	$^\circ\text{C}/\text{W}$	Fig. 25

Electrical Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
I_{DSS}	Zero gate voltage drain current		5	100	μA	$V_{DS}=1200\text{V}, V_{GS}=0\text{V}$	
I_{GSS}	Gate leakage current			± 100	nA	$V_{DS}=0\text{V}, V_{GS}=-5\sim 20\text{V}$	
V_{TH}	Gate threshold voltage	2.0	2.8	4.0	V	$V_{GS}=V_{DS}, I_D=20\text{mA}$	Fig. 8, 9
			2.0		V	$V_{GS}=V_{DS}, I_D=20\text{mA}$ @ $T_J=175^\circ\text{C}$	
R_{ON}	Static drain-source on-resistance		13.5	17	$\text{m}\Omega$	$V_{GS}=18\text{V}, I_D=60\text{A}$ @ $T_J=25^\circ\text{C}$	Fig. 4, 5, 6, 7
			22.5		$\text{m}\Omega$	$V_{GS}=18\text{V}, I_D=60\text{A}$ @ $T_J=175^\circ\text{C}$	
			17		$\text{m}\Omega$	$V_{GS}=15\text{V}, I_D=60\text{A}$ @ $T_J=25^\circ\text{C}$	
			24.5		$\text{m}\Omega$	$V_{GS}=15\text{V}, I_D=60\text{A}$ @ $T_J=175^\circ\text{C}$	
C_{iss}	Input capacitance		4774		pF	$V_{DS}=800\text{V}, V_{GS}=0\text{V},$ $f=100\text{kHz},$ $V_{AC}=25\text{mV}$	Fig. 16
C_{oss}	Output capacitance		211		pF		
C_{rss}	Reverse transfer capacitance		8.1		pF		
E_{oss}	C_{oss} stored energy		88		μJ		Fig. 17
Q_g	Total gate charge		187		nC	$V_{DS}=800\text{V}, I_D=100\text{A},$ $V_{GS}=-3\text{ to }18\text{V}$	Fig. 18
Q_{gs}	Gate-source charge		66		nC		
Q_{gd}	Gate-drain charge		68		nC		
R_g	Gate input resistance		2.3		Ω	$f=1\text{MHz}$	
E_{ON}	Turn-on switching energy		1480		μJ	$V_{DS}=800\text{V}, I_D=100\text{A},$ $V_{GS}=-3.5\text{ to }18\text{V},$ $R_{G(\text{ext})}=2.0\Omega,$ $L=200\mu\text{H}$ $T_J=25^\circ\text{C}$	Fig. 19, 20
E_{OFF}	Turn-off switching energy		430		μJ		
$t_{d(\text{on})}$	Turn-on delay time		22		ns		
t_r	Rise time		33				
$t_{d(\text{off})}$	Turn-off delay time		32				
t_f	Fall time		9.5				

Reverse Diode Characteristics ($T_c=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
V_{SD}	Diode forward voltage		3.3		V	$I_{SD}=30\text{A}, V_{GS}=0\text{V}$	Fig. 10, 11, 12
			3.0		V	$I_{SD}=30\text{A}, V_{GS}=0\text{V}, T_J=175^\circ\text{C}$	
I_S	Diode forward current (continuous)			104	A	$V_{GS}=-2\text{V}, T_c=25^\circ\text{C}$	
				62	A	$V_{GS}=-2\text{V}, T_c=100^\circ\text{C}$	
t_{rr}	Reverse recovery time		48		ns	$V_{GS}=-3.5\text{V}/+18\text{V}, I_{SD}=100\text{A}, V_R=800\text{V}, R_{G(\text{ext})}=10\Omega, L=200\mu\text{H}, di/dt=3000\text{A}/\mu\text{s}$	
Q_{rr}	Reverse recovery charge		289		nC		
I_{RRM}	Peak reverse recovery current		29		A		

Typical Performance (curves)

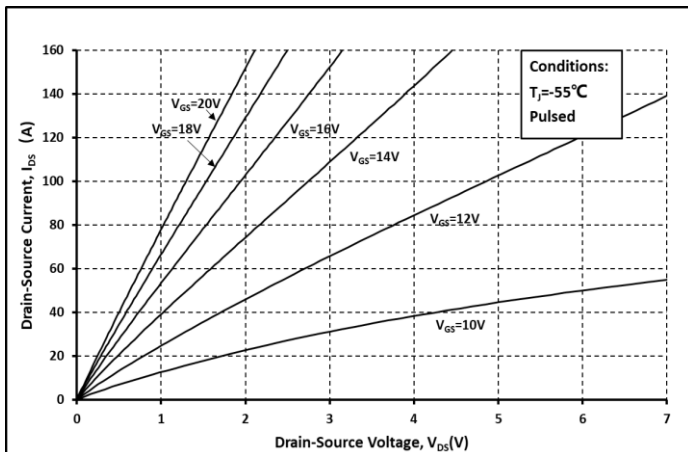


Fig. 1 Output Curve @ $T_j=-55^\circ\text{C}$

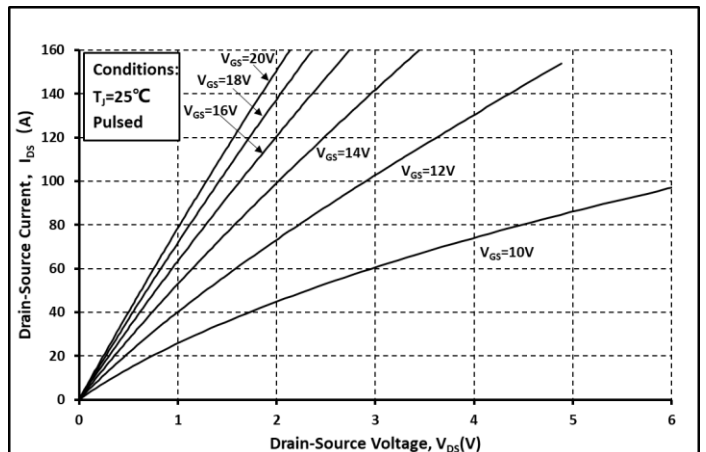


Fig. 2 Output Curve @ $T_j=25^\circ\text{C}$

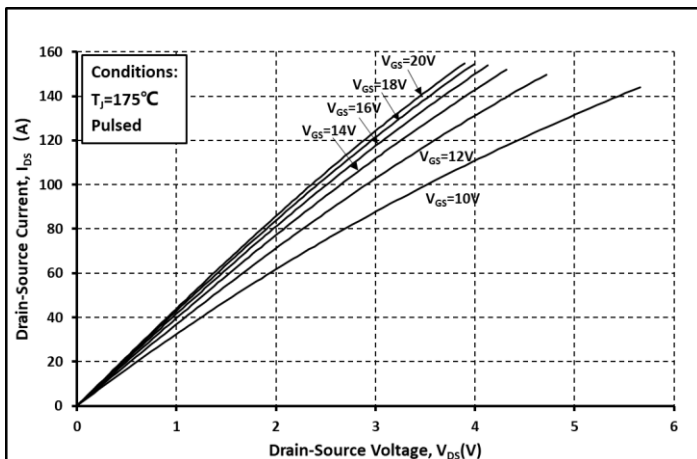


Fig. 3 Output Curve @ $T_j=175^\circ\text{C}$

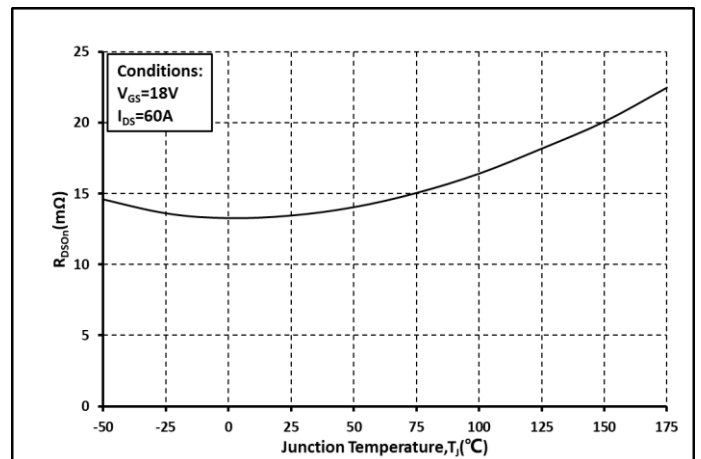


Fig. 4 R_{on} vs. Temperature

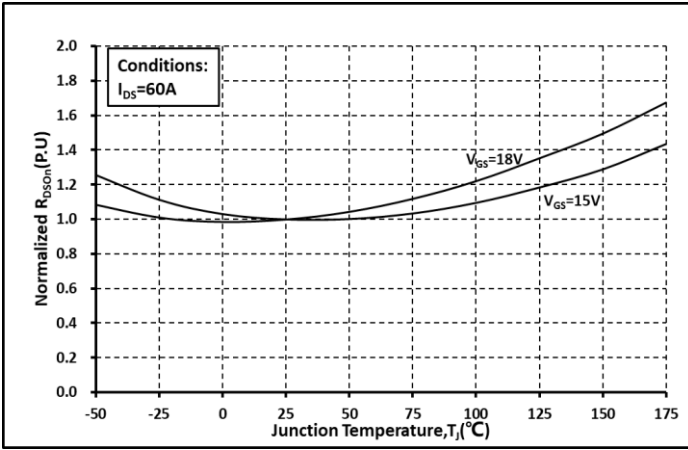


Fig. 5 Normalized Ron vs. Temperature

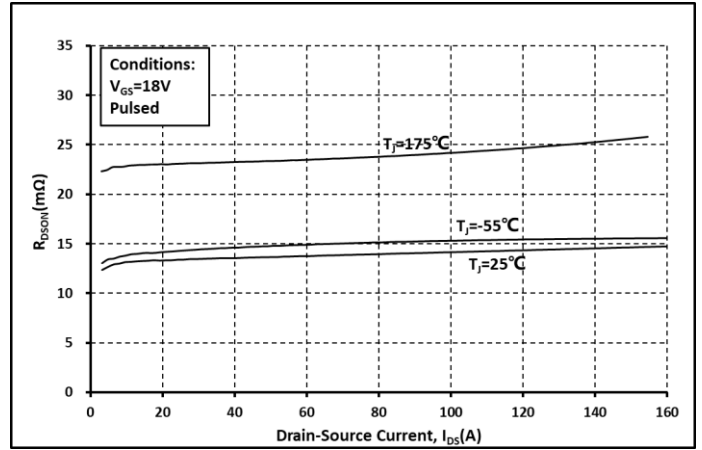


Fig. 6 Ron vs. Ids @ Various Temperature

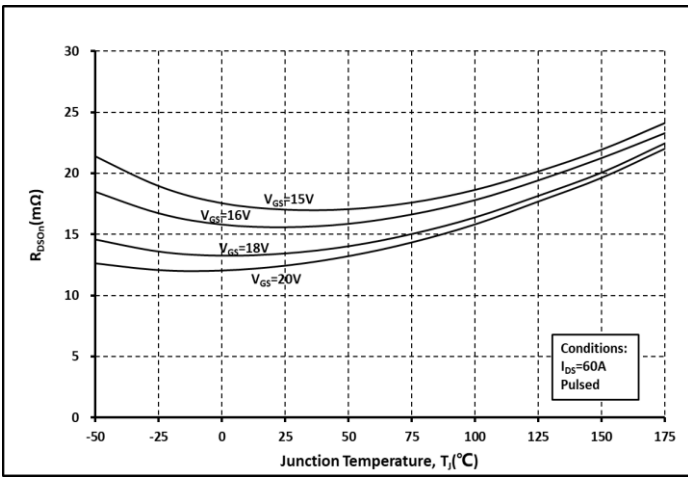


Fig. 7 Ron vs. Temperature @ Various Vgs

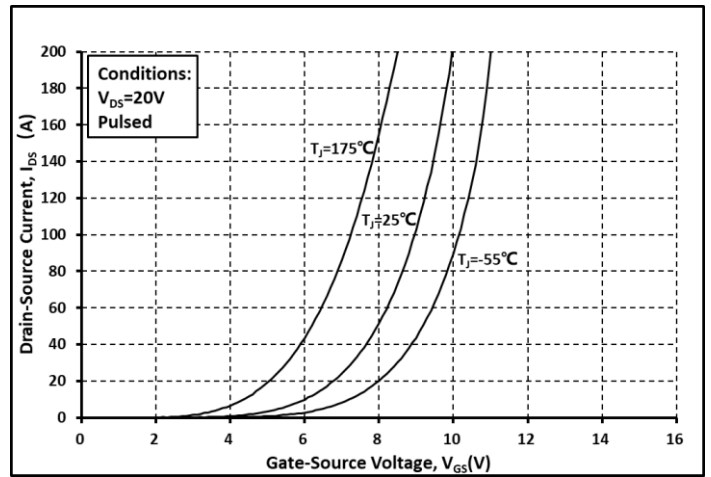


Fig. 8 Transfer Curves @ Various Temperature

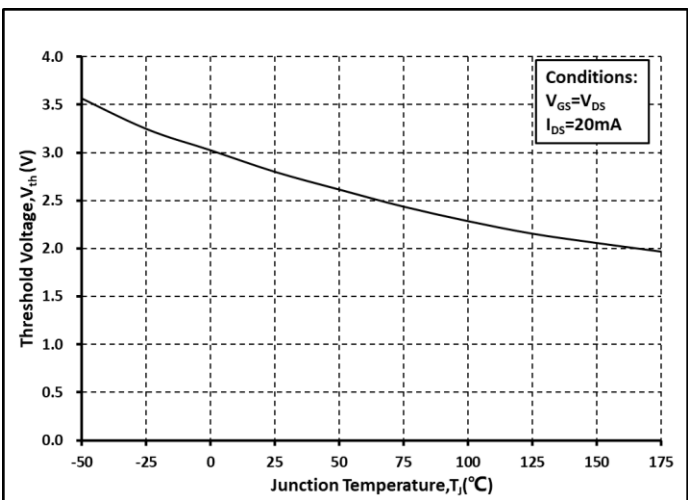


Fig. 9 Threshold Voltage vs. Temperature

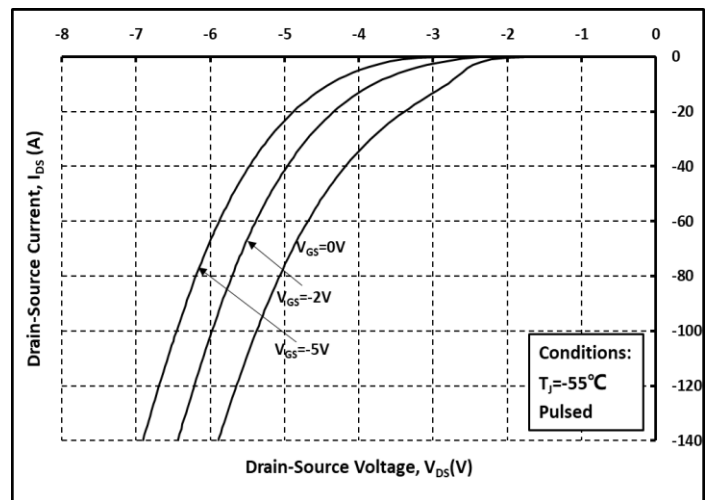


Fig. 10 Body Diode curves @ Tj = -55°C

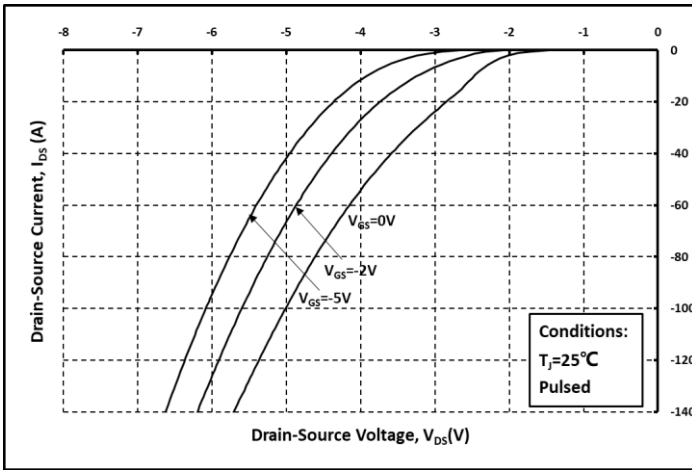


Fig. 11 Body Diode curves @ $T_j=25^\circ\text{C}$

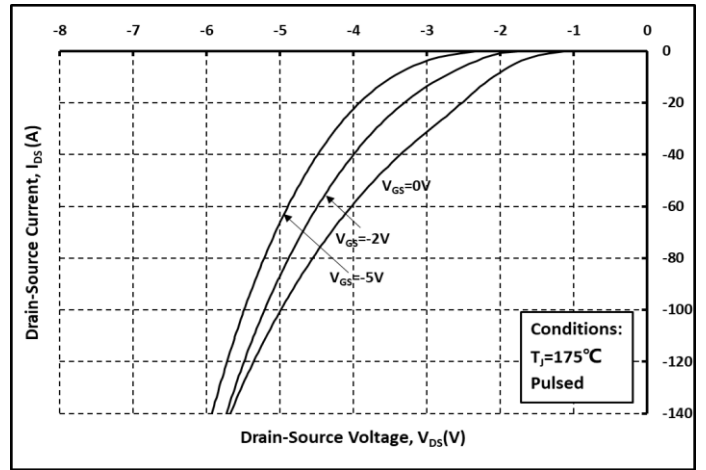


Fig. 12 Body Diode curves @ $T_j=175^\circ\text{C}$

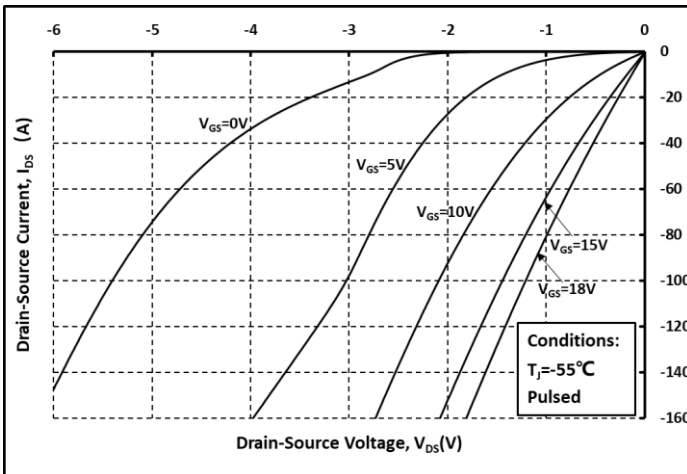


Fig. 13 3rd Quadrant curves @ $T_j=-55^\circ\text{C}$

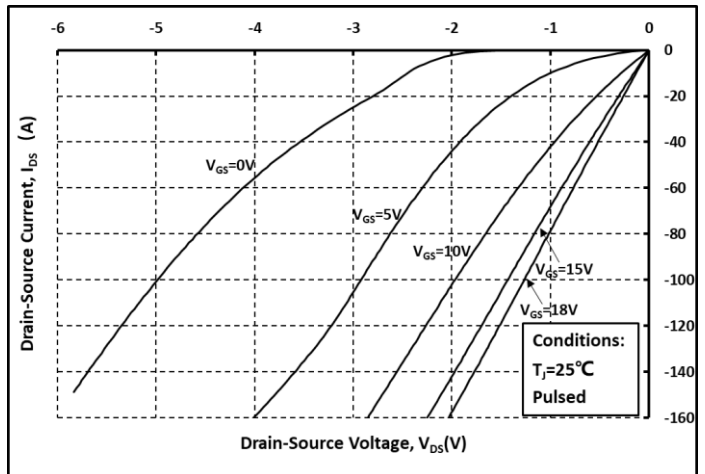


Fig. 14 3rd Quadrant curves @ $T_j=25^\circ\text{C}$

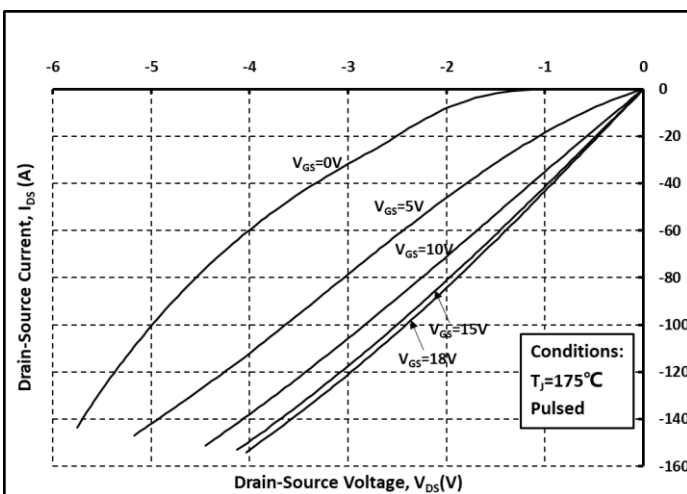


Fig. 15 3rd Quadrant curves @ $T_j=175^\circ\text{C}$

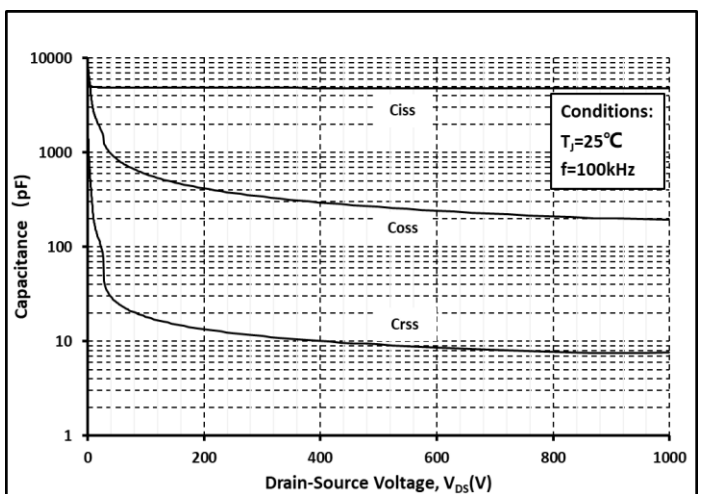


Fig. 16 Capacitance vs. V_{DS}

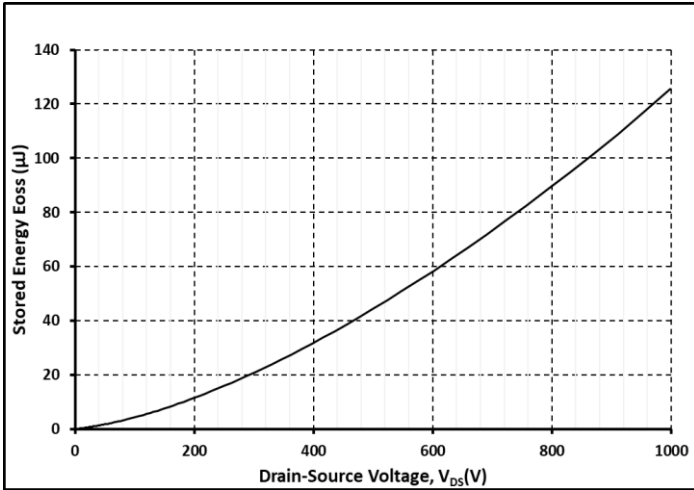


Fig. 17 Output Capacitor Stored Energy

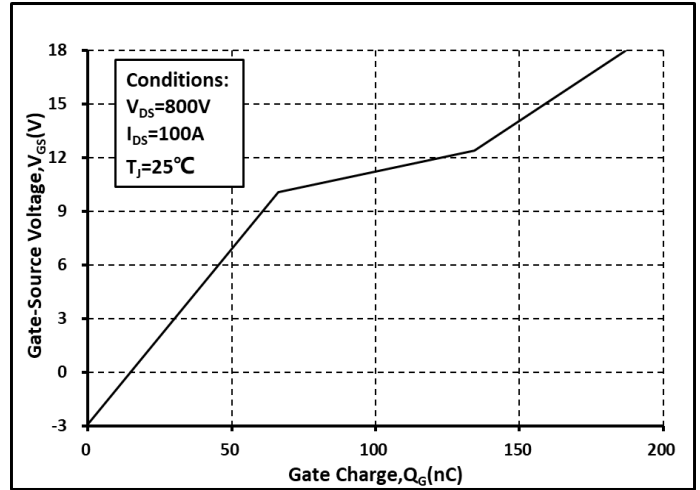


Fig. 18 Gate Charge Characteristics

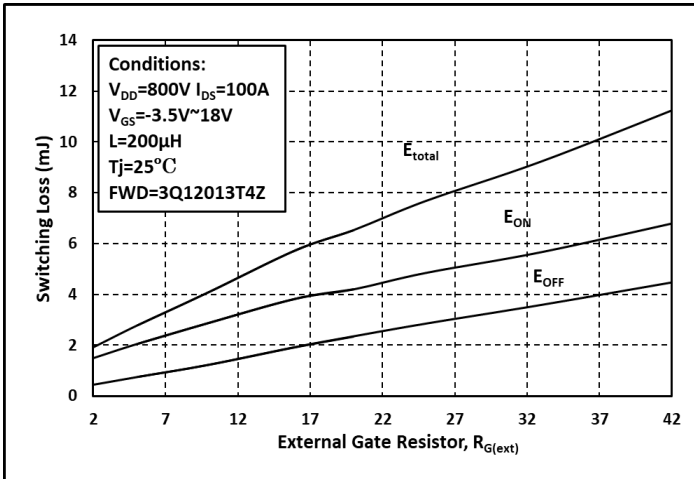


Fig. 19 Switching Energy vs. $R_{G(ext)}$

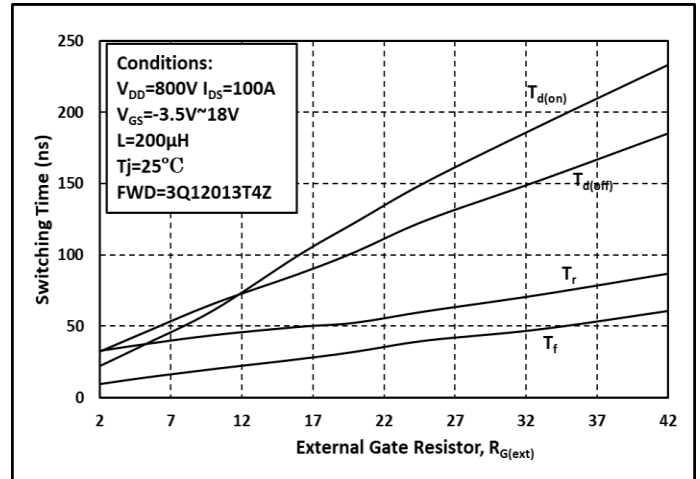


Fig. 20 Switching Times vs. $R_{G(ext)}$

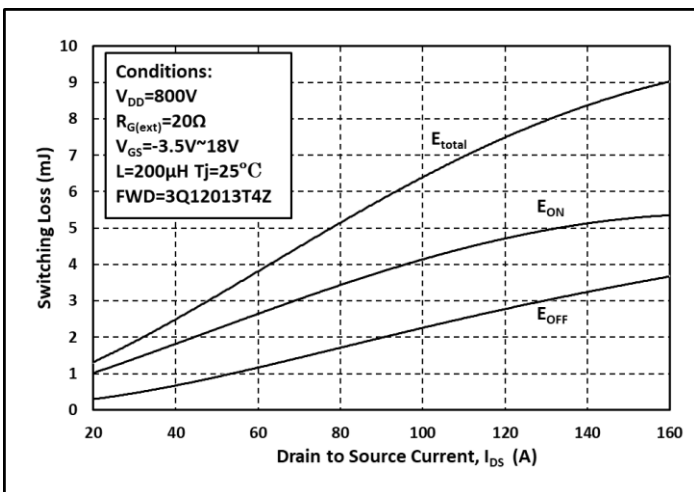


Fig. 21 Switching Energy vs. I_{DS}

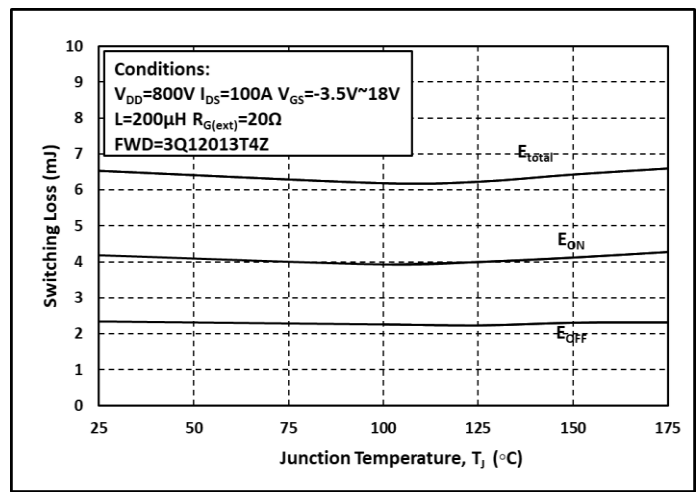


Fig. 22 Switching Energy vs. Temperature

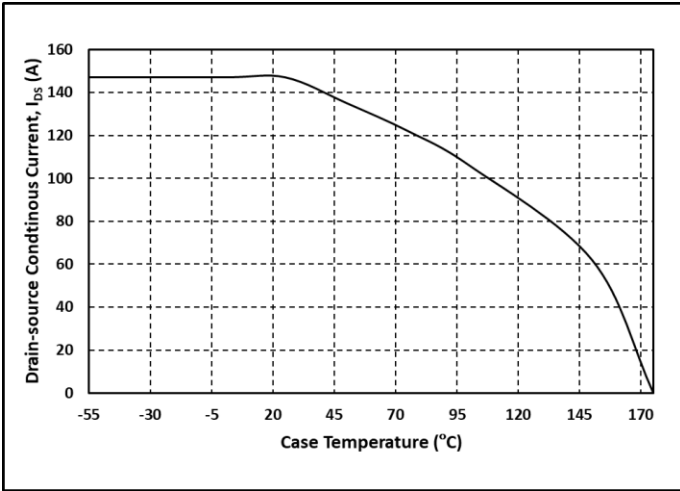


Fig. 23 Continuous Drain Current vs. Case Temperature

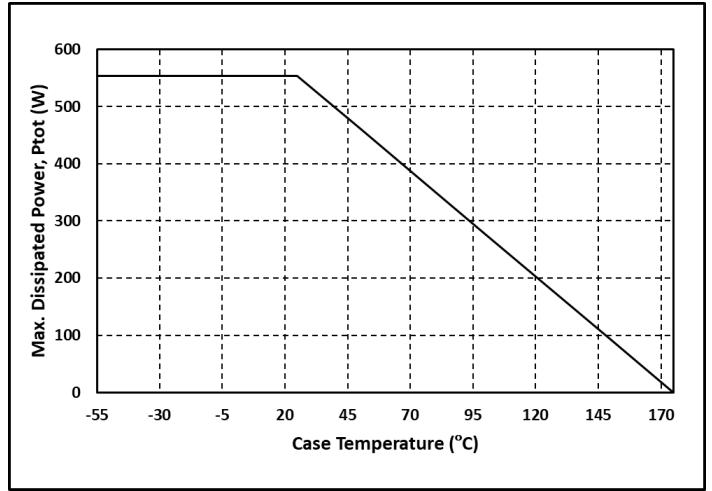


Fig. 24 Max. Power Dissipation Derating vs. Case Temperature

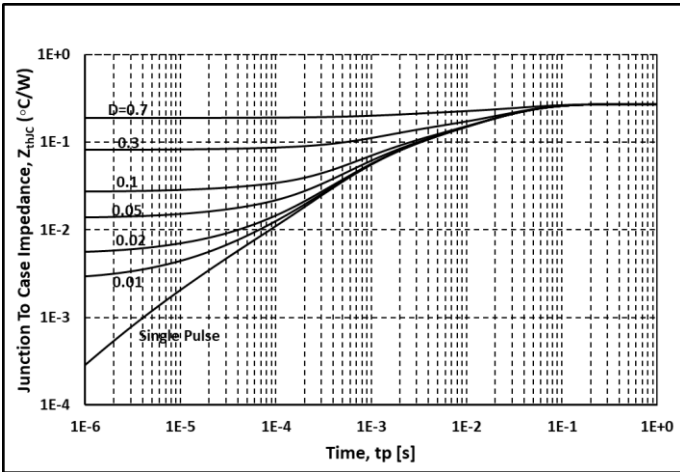


Fig. 25 Thermal impedance

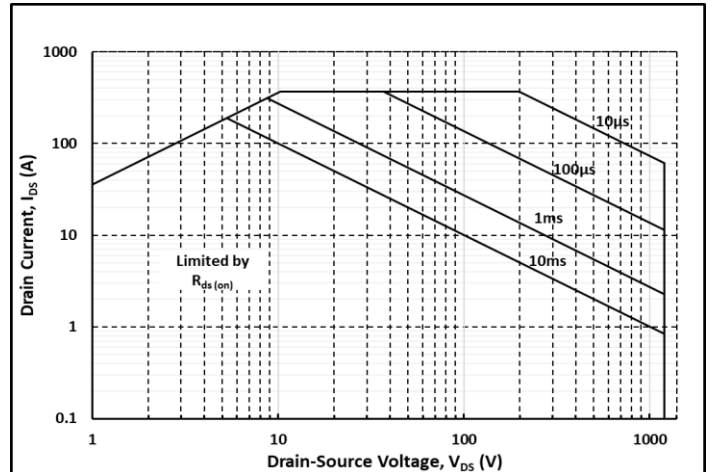
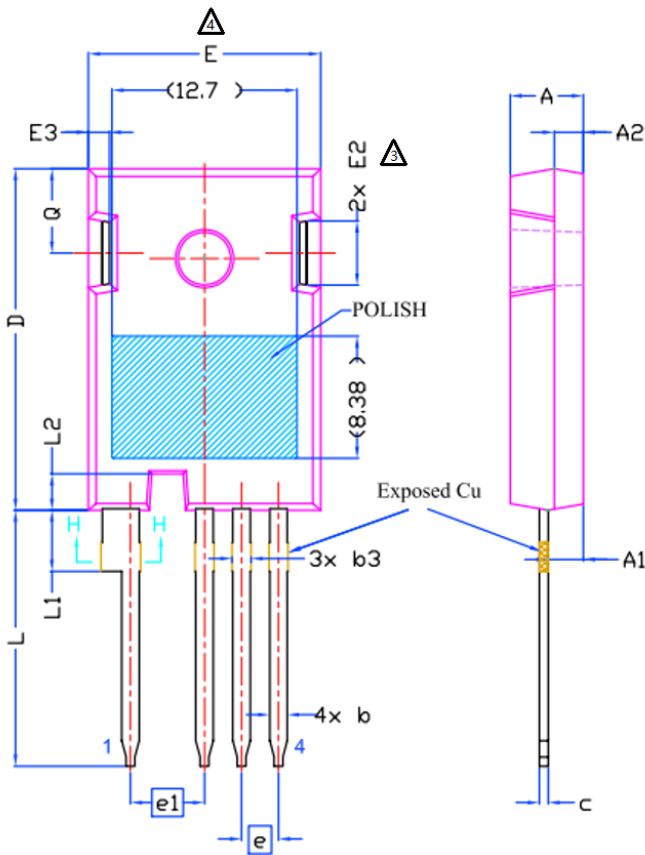
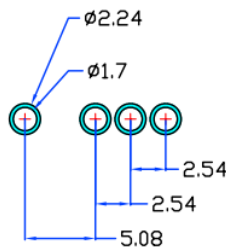
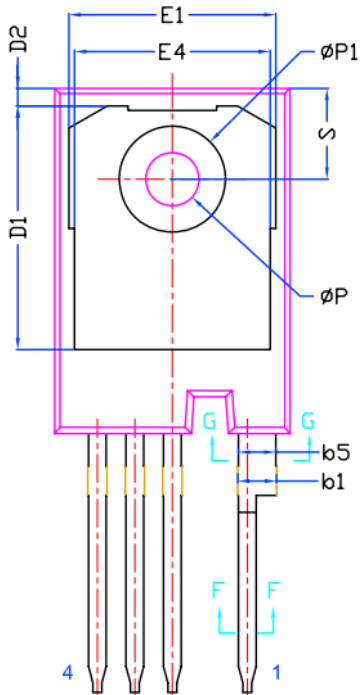


Fig. 26 Safe Operating Area

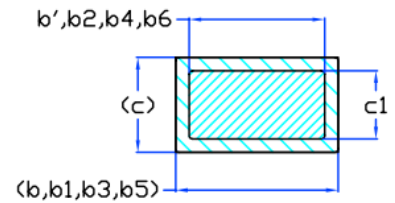
Package Dimensions



Dimensions In Millimeters		
SYMBOL	MIN.	MAX.
A	4.83	5.21
A1	2.29	2.54
A2	1.91	2.16
b	1.07	1.33
b'	1.07	1.28
b1	2.39	2.94
b2	2.39	2.84
b3	1.07	1.60
b4	1.07	1.50
b5	2.39	2.69
b6	2.39	2.64
c	0.55	0.68
c1	0.55	0.65
D	23.30	23.60
D1	16.25	17.65
D2	0.95	1.25
E	15.75	16.13
E1	13.10	14.15
E2	3.68	5.10
E3	1.00	1.90
E4	12.38	13.43
e	2.54 BSC	
e1	5.08 BSC	
L	17.31	17.82
L1	3.97	4.37
L2	2.35	2.65
N	4	
φP	3.51	3.65
φP1	7.18 REF.	
Q	5.49	6
S	6.04	6.3



Recommended Solder Pad Layout



Section F--F, G--G, H--H

Note:

1. Package Reference: JEDEC TO247, Variation AD
2. All Dimensions are in mm
3. Slot Required, Notch May Be Rounded
4. Dimension D&E Do Not Include Mold Flash
5. Subject to Change Without Notice

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