IV2Q20045BD – 2000V 45mΩ Gen2 SiC MOSFET chip

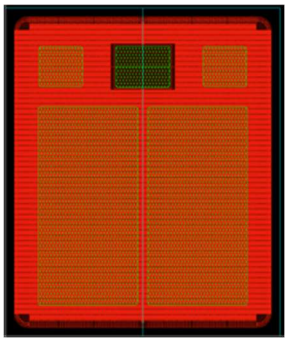
Features

- 2nd Generation SiC MOSFET Technology with +15~+18V gate drive
- High blocking voltage with low on-resistance
- High speed switching with low capacitance
- 175℃ operating junction temperature capability
- Very fast and robust intrinsic body diode
- Kelvin gate input easing driver circuit design

Applications

- Solar boosters
- UPS power supplies
- Motor drivers
- Switch mode power supplies

Chip Outline:



Part Number	Die Size
IV2Q20045BD	Please contact your sales representative to get the detailed die information

Absolute Maximum Ratings (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
V_{DS}	Drain-Source voltage	2000	V	V_{GS}=0V, I_D=100μA	
V_{GSmax} (Transient)	Maximum transient voltage	-10 to 23	V	Duty cycle<1%, and pulse width<200ns	
V_{GSon}	Recommended turn-on voltage	15 to 18	V		
V_{GSoff}	Recommended turn-off voltage	-5 to -2	V	Typical -3.5V	
I_D	Drain current (continuous)	62	A	V_{GS}=18V, T_C=25°C	Fig. 23
I_D	Drain current (continuous)	46	A	V_{GS}=18V, T_C=100°C	Fig. 23
I_{DM}	Drain current (pulsed)	155	A	Pulse width limited by SOA and dynamic $R_{\theta(J-C)}$	Fig. 25, 26
I_{SM}	Body diode current (pulsed)	155	A	Pulse width limited by SOA and dynamic $R_{\theta(J-C)}$	Fig. 25,26
P_{TOT}	Total power dissipation	500	W	T_C=25°C	Fig. 24
T_{stg}	Storage temperature range	-55 to 175	°C		
T_J	Operating junction temperature	-55 to 175	°C		
T_L	Solder Temperature	260	°C	wave soldering only allowed at leads, 1.6mm from case for 10 s	

Note1: Assumes $R_{\theta(J-C)}$< 0.3°C/W.

Note2: All the electrical data and curve data please refer to datasheet for packaged device which part number is IV2Q20045T4.

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
I_{DSS}	Zero gate voltage drain current		1	10	μA	V_{DS}=2000V, V_{GS}=0V	
I_{GSS}	Gate leakage current			±100	nA	V_{DS}=0V, V_{GS}=-5~20V	
V_{TH}	Gate threshold voltage	1.8	2.8	4.5	V	V_{GS}=V_{DS}, I_D=10mA	Fig. 8, 9
			2.2			V_{GS}=V_{DS}, I_D=10mA @ T_J=175°C	
R_{ON}	Static drain-source on-resistance		43	56	mΩ	V_{GS}=18V, I_D=20A @T_J=25°C	Fig. 4, 5, 6, 7
			105		mΩ	V_{GS}=18V, I_D=20A @T_J=175°C	
			48		mΩ	V_{GS}=15V, I_D=20A @T_J=25°C	
			110		mΩ	V_{GS}=15V, I_D=20A @T_J=175°C	
C_{iss}	Input capacitance		3950		pF	V_{DS}=1500V, V_{GS}=0V, f=1MHz, V_{AC}=25mV	Fig. 16
C_{oss}	Output capacitance		110		pF		
C_{rss}	Reverse transfer capacitance		13		pF		
E_{oss}	C_{oss} stored energy		145		μJ		Fig. 17
Q_g	Total gate charge		175		nC	V_{DS}=1500V, I_D=20A, V_{GS}=-3 to 18V	Fig. 18
Q_{gs}	Gate-source charge		43		nC		
Q_{gd}	Gate-drain charge		63		nC		
R_g	Gate input resistance		1.5		Ω	f=1MHz	
E_{ON}	Turn-on switching energy		870		μJ	V_{DS}=1200V, I_D=20A, V_{GS}=-3.5 to 18V, $R_{G(ext)}$=3.3Ω, L=400μH, T_J=25°C	Fig. 19, 20
E_{OFF}	Turn-off switching energy		150		μJ		
$t_{d(on)}$	Turn-on delay time		25		ns		
t_r	Rise time		24				
$t_{d(off)}$	Turn-off delay time		40				
t_f	Fall time		23				

Reverse Diode Characteristics (T_C=25°C unless otherwise specified)

Symbol	Parameter	Value			Unit	Test Conditions	Note
		Min.	Typ.	Max.			
V_{SD}	Diode forward voltage		3.5		V	I_{SD}=20A, V_{GS}=0V	Fig. 10, 11, 12
			3.4		V	I_{SD}=20A, V_{GS}=0V, T_J=175°C	
t_{rr}	Reverse recovery time		46		ns	V_{GS}=-3.5V/+18V, I_{SD}=20A, V_R=1200V, $R_{G(ext)}$=5.1Ω, di/dt=3000A/μs	
Q_{rr}	Reverse recovery charge		550		nC		
I_{RRM}	Peak reverse recovery current		23		A		

Typical Performance (curves)

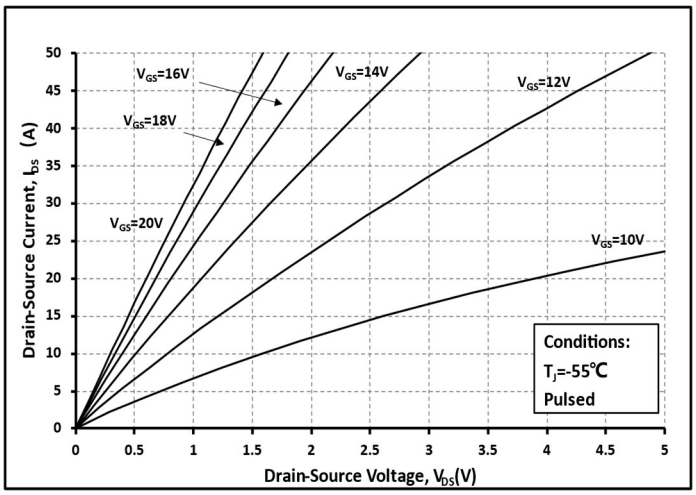


Fig. 1 Output Curve @ T_J=-55℃

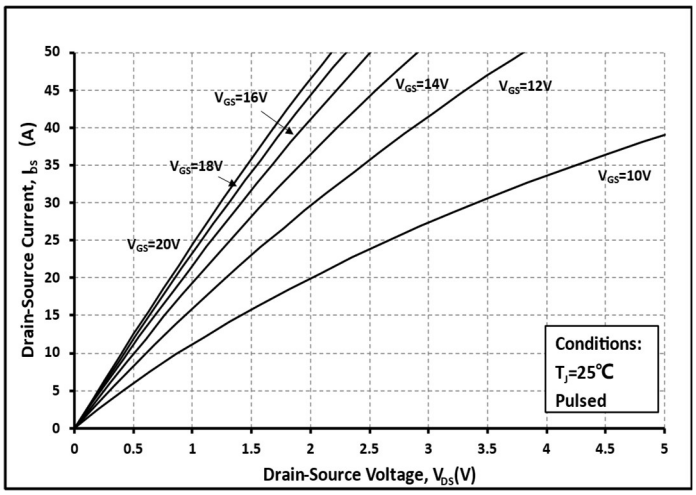


Fig. 2 Output Curve @ T_J=25℃

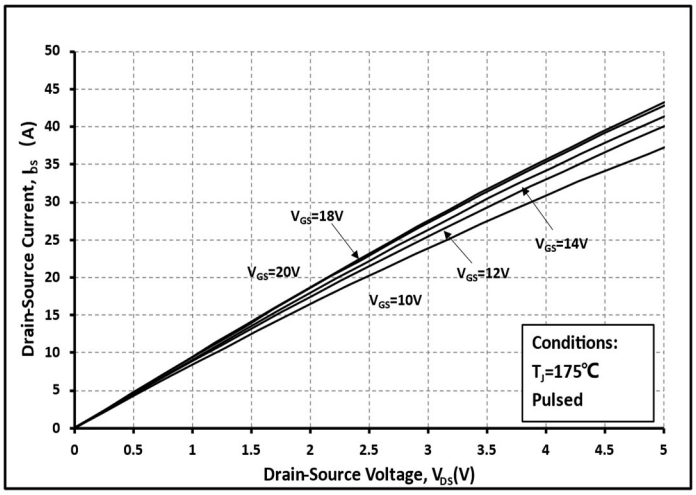


Fig. 3 Output Curve @ T_J=175℃

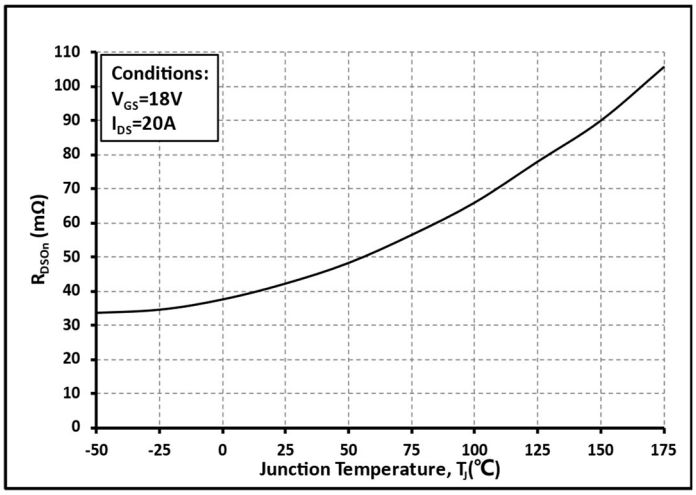


Fig. 4 Ron vs. Temperature

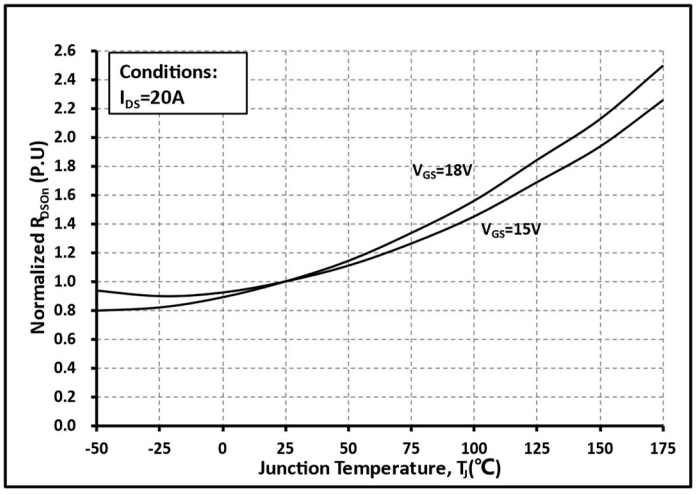


Fig. 5 Normalized Ron vs. Temperature

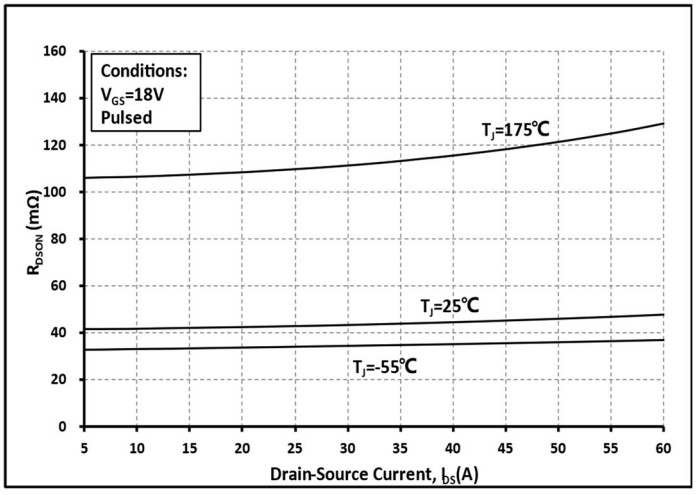


Fig. 6 Ron vs. I_{DS} @ Various Temperature

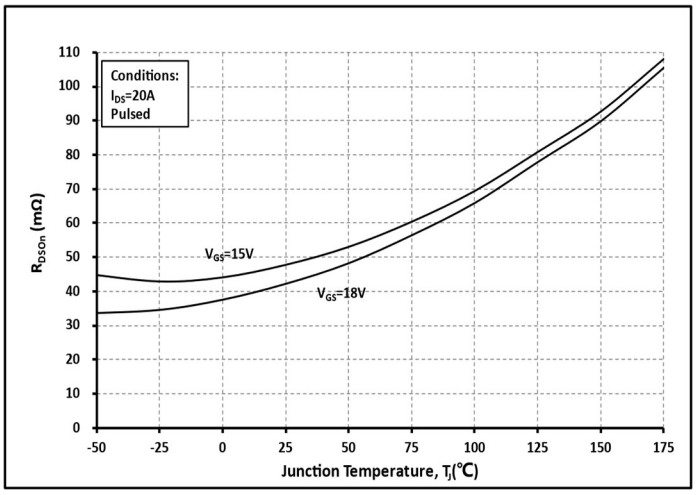


Fig. 7 Ron vs. Temperature @ Various V_{GS}

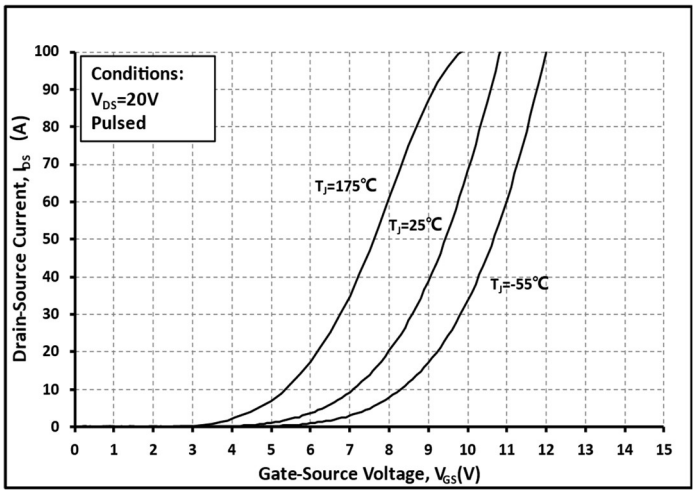


Fig. 8 Transfer Curves @ Various Temperature

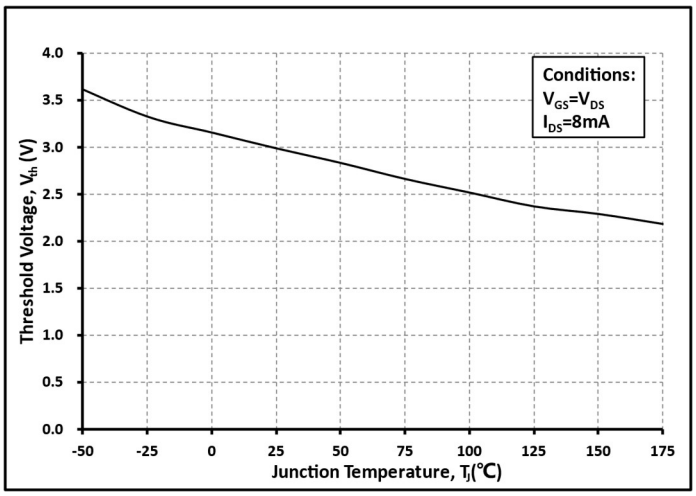


Fig. 9 Threshold Voltage vs. Temperature

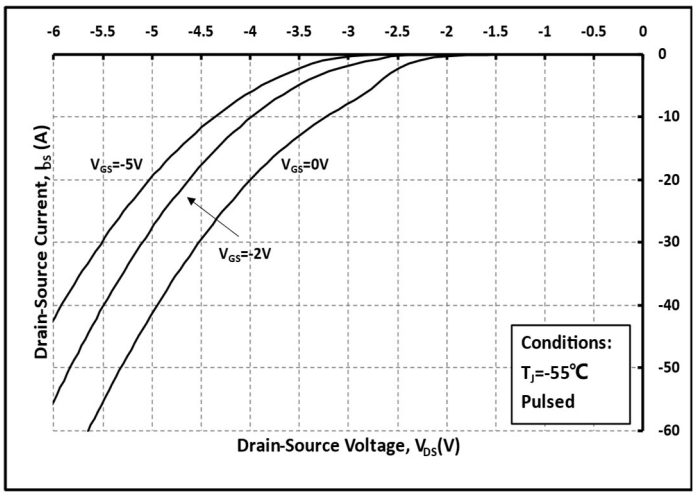


Fig. 10 Body Diode curves @ T_J=-55°C

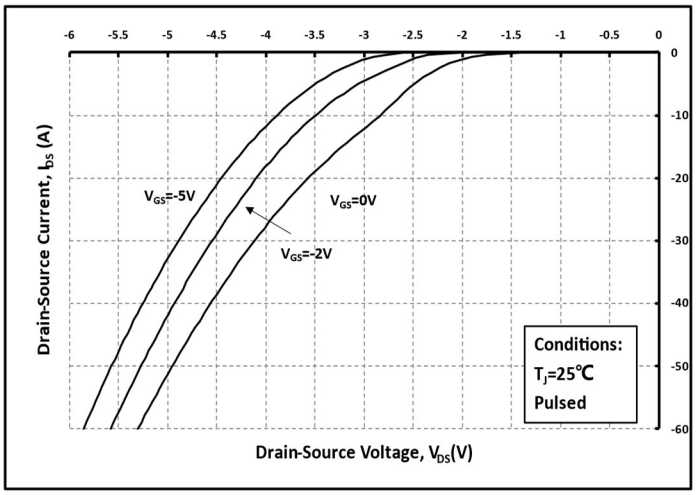


Fig. 11 Body Diode curves @ T_J=25°C

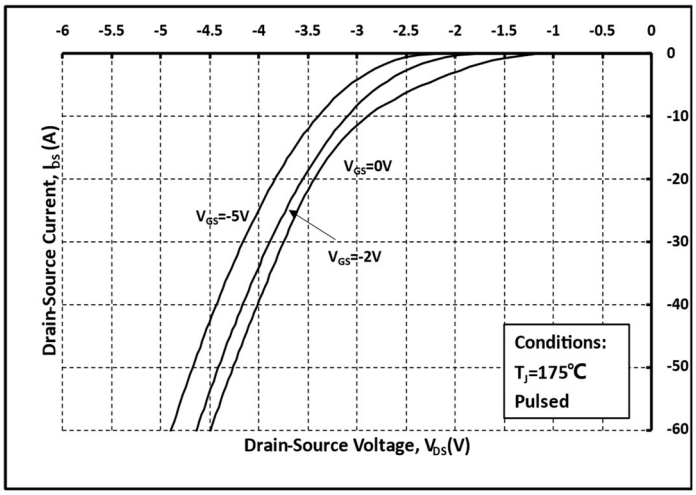


Fig. 12 Body Diode curves @ T_J=175°C

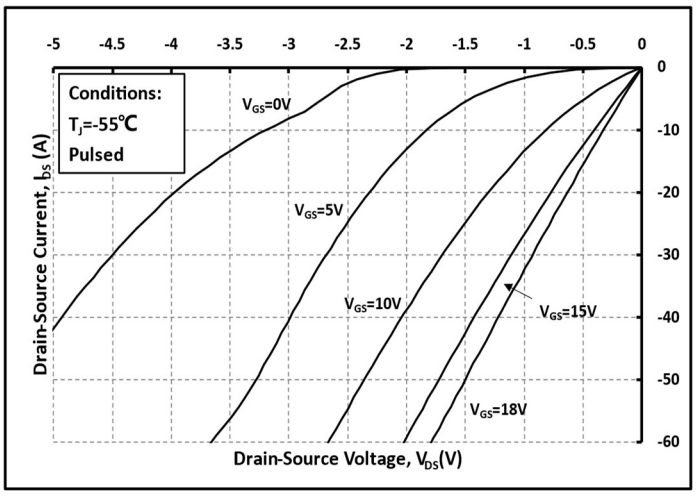


Fig. 13 3rd Quadrant curves @ T_J=-55°C

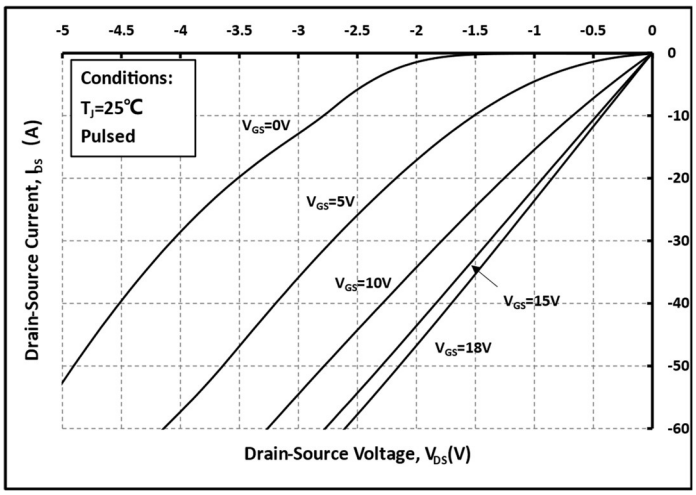


Fig. 14 3rd Quadrant curves @ T_J=25°C

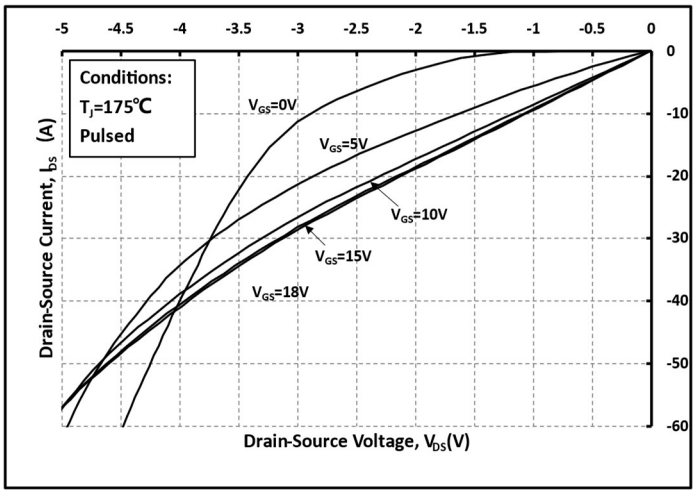


Fig. 15 3rd Quadrant curves @ T_J=175°C

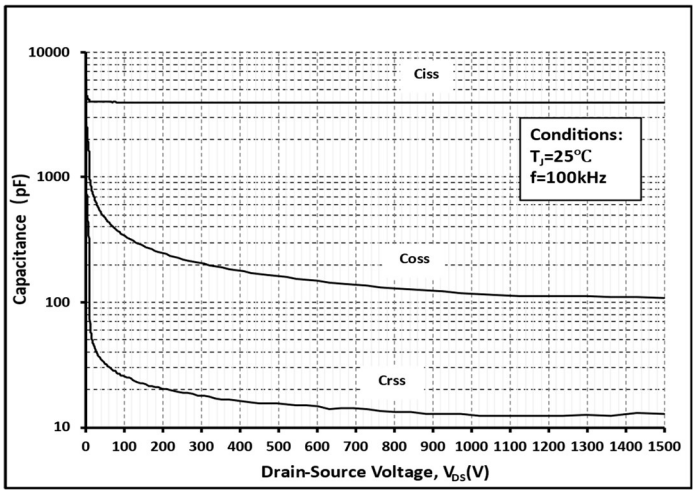


Fig. 16 Capacitance vs. V_{DS}

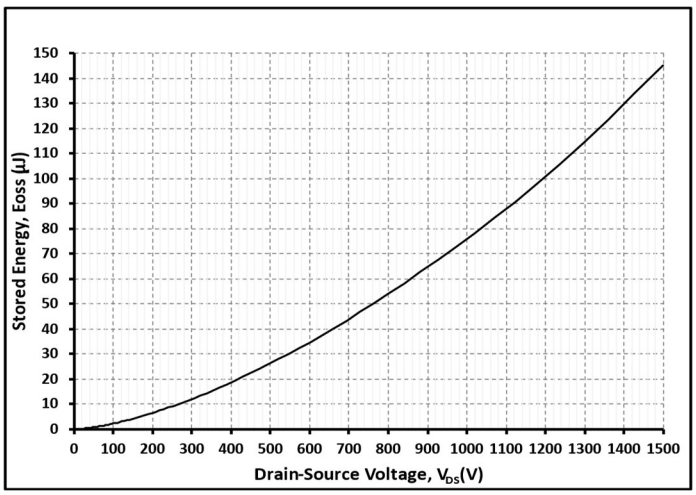


Fig. 17 Output Capacitor Stored Energy

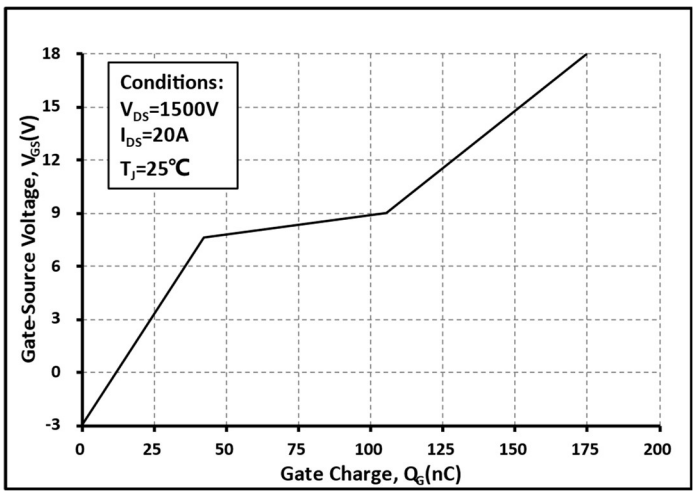


Fig. 18 Gate Charge Characteristics

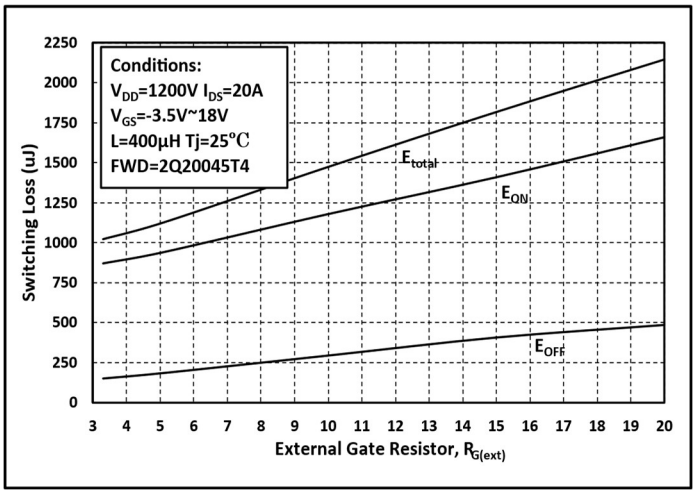


Fig. 19 Switching Energy vs. $R_{G(ext)}$

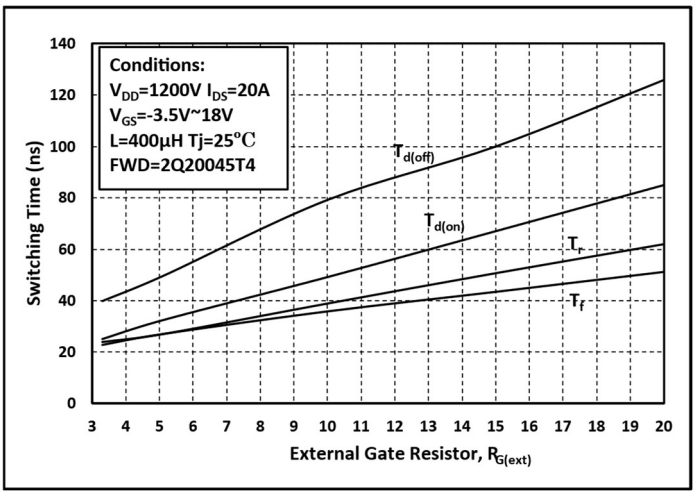


Fig. 20 Switching Times vs. $R_{G(ext)}$

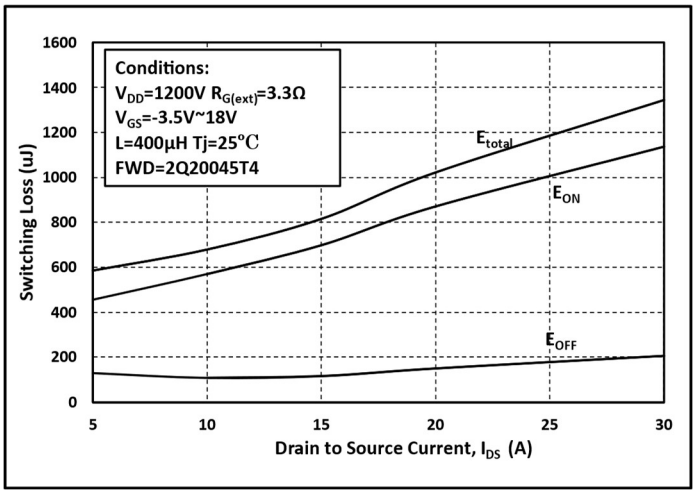


Fig. 21 Switching Energy vs. I_{DS}

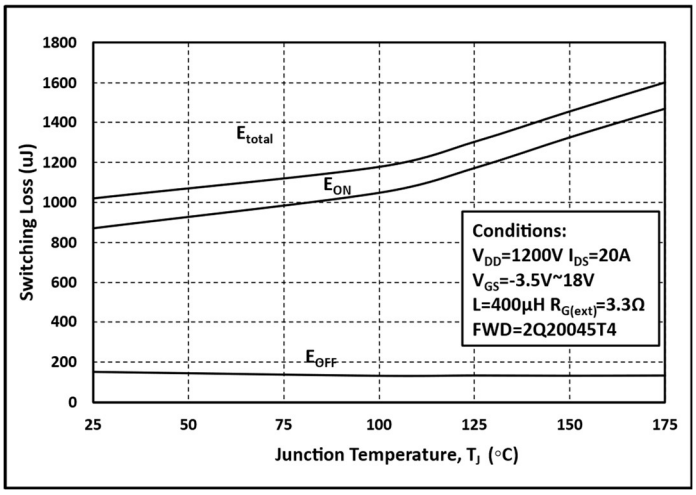


Fig. 22 Switching Energy vs. Temperature

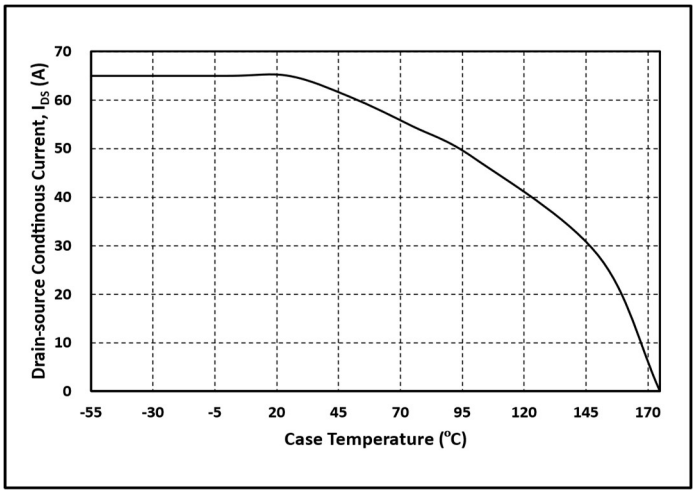


Fig. 23 Continuous Drain Current vs. Case Temperature

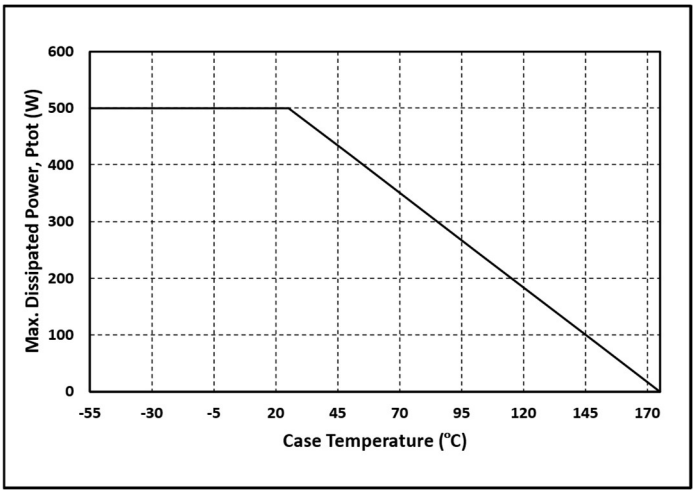


Fig. 24 Max. Power Dissipation Derating vs. Case Temperature

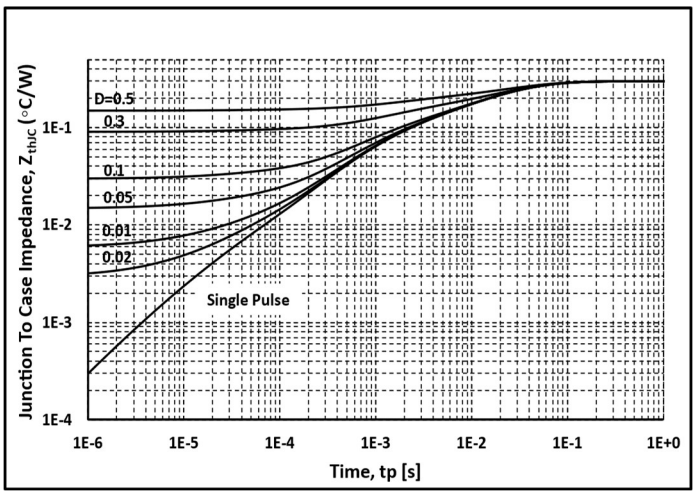


Fig. 25 Thermal impedance

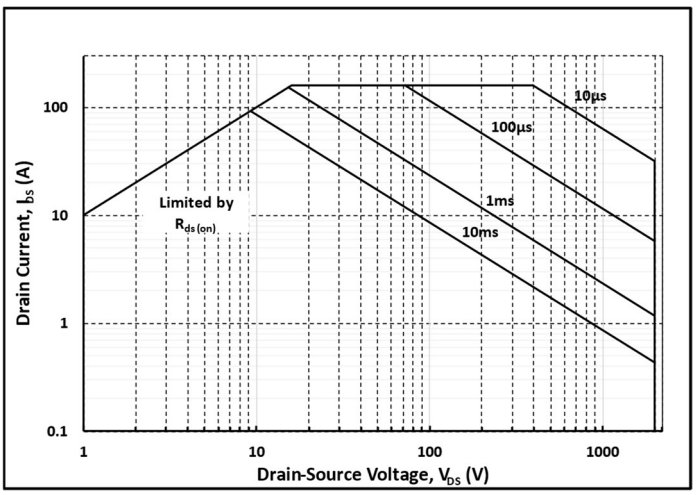


Fig. 26 Safe Operating Area

Notes

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