IVCO1411/2 4A Isolated Single Channel Gate Drivers

1. Features

- Multiple options:
  - Short Circuit Protection (IVCO1411)
  - Negative Bias Drive Output (IVCO1412)
- Industry standard SOIC(W)-8 pinout supports 5.7kVrms isolation voltage
- 4A peak source and sink drive current
- Wide driver VCC2 range up to 25V
- 13.5V VCC2 UVLO protection
- 100V/ns minimum CMTI
- 50ns typical propagation delay
- Outputs held low when floating inputs
- Safety and regulatory certifications:
  - UL (pending)
  - VDE (pending)
  - CQC (pending)
- Operating temperature range -40°C to 125°C
- AEC-Q100 qualified

2. Applications

- Emerging Wide Band-Gap Power Devices
- Motor Drivers
- EV/HEV inverters and DC/DC converters
- PV boosters and inverters
- AC/DC and DC/DC converters
- Server and Telecom rectifiers
- UPS

3. Description

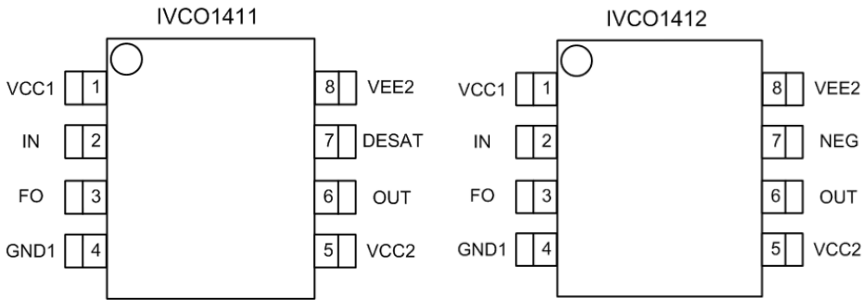
The IVCO1411/2 is a family of 4A single-channel isolated gate drivers with 5.7kVrms isolation. It is capable of effectively and safely driving SiC/Si MOSFETs and Si IGBTs. With integrated over current protection or drive negative bias, it greatly simplifies the driver circuit design.

Wide output VDD operating range from 15V to 25V enables effective driving with Si or SiC MOSFET and IGBT power switches. Integrated UVLO protection ensures outputs held at low under abnormal conditions. The input VDD operates from 2.5V to 5.5V, which supports most digital controllers.

Device Information

PART NUMBER	PACKAGE	PACKING
IVCO1411FDWQR	SOIC(W)-8	Tape and Reel
IVCO1412FDWQR	SOIC(W)-8	Tape and Reel
IVCO1411HDWQR	SOIC(W)-8	Tape and Reel

Pin Configurations



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4. Pin Configuration and Functions

PIN	PART NUMBER	NAME	I/O	DESCRIPTION
1	IVCO1411/2	VCC1	P	Input Power Supply
2		IN	I	Input
3		FO	O	Fault Output
4		GND1	G	Input Ground
5		VCC2	P	Output Power Supply
6		OUT	O	Output
8		VEE2	G	Output Ground
7	IVCO1411	DESAT	I	Desaturation Input, MOSFET/IGBT Drain/Collector
7	IVCO1412	NEG	O	Negative Voltage Output

Truth Table

VCC1	IN	VCC2	OUT
X	X	below UVLO	L
below UVLO	X	X	L
above UVLO	L or floating	above UVLO	L
above UVLO	H	above UVLO	H

5. Specifications

5.1. Absolute Maximum Ratings

Over free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC1}	Input supply voltage (reference to GND1)	-0.3	6	V
IN	Signal input voltage	-0.3	V_{cc1}+0.3	V
V_{CC2}	Output supply voltage (reference to VEE2)	-0.3	32	V
FO	Fault Output	-0.3	V_{cc1}+0.3	V
OUT	Gate driver output voltage	-0.3	V_{cc2}+0.3	V
DESAT	Desaturation input voltage (IVCO1411)	-0.3	V_{cc2}+0.3	V
NEG	Negative output voltage (IVCO1412)	-5.5	V_{cc2}+0.3	V
T_J	Junction temperature	-40	150	°C
T_{STG}	Storage temperature	-65	150	°C

(1) Operating beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended period may affect device reliability.

5.2. ESD Rating

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	+/-2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	+/-750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3. Recommended Operation Conditions

		MIN	MAX	UNIT
V_{CC1}	Input supply voltage	2.5	5.5	V
V_{IN}	Input voltage	0	V_{CC1}	V
V_{CC2}	Output supply voltage	15	25	V
V_{CC2}	Output supply voltage of IVCO1411H	18	25	V
T_A	Ambient temperature	-40	125	°C

5.4. Thermal Information

		VALUE	UNIT
$R_{\theta JA}$	Junction-to-Ambient	103	°C/W
$R_{\theta JB}$	Junction-to-PCB	65	°C/W

5.5. Electrical Specifications

Unless otherwise noted, V_{CC1} = 3.3 V, V_{CC2} = 15 V, V_{CC2} (IVCO1411H)= 18 V ,T_A = –40°C to 125°C
Currents are positive into and negative out of the specified terminal. Typical condition specifications are at 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS CURRENT						
I_{CC1q}	V_{CC1} quiescent supply current	output logic LOW		1.3	3	mA
I_{CC2q}	V_{CC2} quiescent supply current	output logic LOW		4.0	8	mA
UVLO (V_{CC1})						
V_{ON}	V_{CC1} Under voltage lockout thresholds	Rising threshold	1.95	2.2	2.375	V
V_{OFF}		Falling threshold	1.88	2.07	2.325	V
UVLO (V_{CC2})						
V_{ON}	V_{CC2} Under voltage lockout thresholds	Rising threshold	12.5	13.5	14.5	V
V_{OFF}		Falling threshold	11.6	12.7	13.6	V
UVLO (V_{CC2}) (IVCO1411H)						
V_{ON}	V_{CC2} Under voltage lockout thresholds	Rising threshold	15.5	16.7	17.9	V
V_{OFF}		Falling threshold	14.3	15.4	16.5	V
INPUT						
V_{INH}	Input rising threshold			1.77	2	V
V_{INL}	Input falling threshold		0.8	1.32		V
FAULT OUTPUT						
T_{FO}	Fault pulse width			13		us
V_{OH}	Output high voltage	I_{FO} = -2mA	V_{CC1}-0.2	V_{CC1}-0.1		V
V_{OL}	Output low voltage	I_{FO} = 2mA		0.1	0.2	V
OUTPUTS						
I_{PK}	Peak sink/source current	C_{LOAD} =0.22uF, with external current limiting, 1kHz switching frequency		4		A
V_{OH}	Output high voltage	I_{OUTH} = -20mA	V_{CC2}-0.05	V_{CC2}-0.03		V
V_{OL}	Output low voltage	I_{OUTL} = 20mA		0.01	0.03	V
R_{OH}	Output pull-up resistance			1.5	2.5	Ω
R_{OL}	Output pull-down resistance			0.6	1.5	Ω
DESAT (IVCO1411)						
I_{DESATL}	DESAT sink current			44		mA
I_{DESATL}	DESAT source current			1		mA
V_{DESAT}	DESAT threshold voltage		8.8	9.8	10.7	V
V_{DESAT} (1411H)	DESAT threshold voltage of IVCO1411H		11.7	13	14.3	V
T_{BLK}	DESAT blanking time		190	223	280	ns
NEG (IVCO1412)						
V_{NEG}	NEG negative voltage	IN=0V	-3.6	-3	-2.6	V
TIMING						
TD_r	Output rising delay	C_{LOAD} = 1.8nF	40	53	70	ns
TD_f	Output falling delay	C_{LOAD} = 1.8nF	30	50	70	ns
T_r	Rise time	C_{LOAD} = 1.8nF	5	13	18	ns
T_f	Fall time	C_{LOAD} = 1.8nF	3	8	12	ns
CMTI (*)			100			V/ns
TIMING (IVCO1411H)						
TD_r	Output rising delay	C_{LOAD} = 1.8nF	40	55	70	ns
TD_f	Output falling delay	C_{LOAD} = 1.8nF	30	50	70	ns

T_r	Rise time	C_{LOAD} = 1.8nF	5	16	18	ns
T_f	Fall time	C_{LOAD} = 1.8nF	3	9	12	ns
CMTI (*)			100			V/ns

(*) Guaranteed by design

5.6 Insulation and Safety Related Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
	Rated Dielectric Insulation Voltage	1-minute duration	5700	V_{RMS}
CLR	External Clearance	Measured from input terminals to output terminals, shortest distance through air	≥8	mm
CPG	External Creepage	Measured from input terminals to output terminals, shortest distance alone body	≥8	mm
DTI	Internal Clearance	Insulation distance through insulation	≥27	μm
CTI	Comparative Tracking Index	DIN EN 60112 (VDE 0303-11)	>600	V
	Material Group	IEC 60664-1	I	
R_{IO}-R_S	Isolation Resistance (Input to Output)		10^{12}	Ω
C_{IO}	Barrier Capacitance (Input to Output)	Freq = 1 MHz	0.5	pF
	Installation Classification per DIN VDE 0110	For rated mains voltage < 300 VRMS	I – IV	
		For rated mains voltage < 400 VRMS	I – IV	
		For rated mains voltage < 600 VRMS	I – III	
	Climatic Classification		40/125/21	
	Pollution Degree per DIN VDE 0110, Table 1		2	
V_{IORM}	Maximum Working Insulation Voltage		2121	V_{PK}
V_{IOTM}	Maximum Transient Isolation Voltage		8000	V_{PK}
V_{IOSM}	Maximum Surge Isolation Voltage	IEC60065, 1.2/50 μs combination wave V_{TEST} = 1.6 x V_{IOSM}	8000	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method B1	V_{IORM} x 1.875 = $V_{pd(m)}$, 100% production test, t_{ini} = t_m = 1 s, partial discharge < 5 pC	3976	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method A: After Environmental Tests Subgroup 1	V_{IORM} x 1.6 = $V_{pd(m)}$, 100% production test, t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	3393	V_{PK}
$V_{pd(m)}$	Input to Output Test Voltage, Method A: After Input and/or Safety Test Subgroup 2 and Subgroup 3	V_{IORM} x 1.2 = $V_{pd(m)}$, 100% production test, t_{ini} = 60 s, t_m = 10 s, partial discharge < 5 pC	2545	V_{PK}
T_S	Maximum Safety Temperature		150	°C
R_S	Isolation Resistance at T_S	V_{IO} = 500 V, Ta = 25℃	> 10^{12}	Ω
		V_{IO} = 500 V, 100℃ ≤Ta ≤ 25℃	> 10^{11}	Ω
		V_{IO} = 500 V, Ta = 150℃	> 10^9	Ω

5.7 Regulatory Information

Regulatory	
UL	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 5700V_{RMS} Isolation Voltage (pending)
VDE	DIN EN IEC 060747-17(VDE 0884-17):2021-10[2] Basic insulation, V_{IORM} = 2121V_{PK}, V_{IOSM} = 8000V_{PK} (pending)
CQC	Certified under GB4943.1-2022 Basic insulation at 3000V_{RMS} (4242V_{PK}) (pending)

(1) In accordance with UL 1577, each IVCO1411/2 is proof tested by applying an insulation test voltage ⩾ 6840 V rms for 1 sec.

(2) In accordance with VDE 0884-17, each IVCO1411/2 is proof tested by applying an insulation test voltage ⩾ 3976V rms for 1 sec (partial discharge limit = 5pC).

6. Typical Characteristics

VCC1= 3.3V, 0.1uF capacitor from VCC1 to GND1, VCC2 = 15V, 1uF capacitor from VCC2 to VEE2, CLOAD =1nF. TA = –40°C to 125°C (Unless otherwise noted).

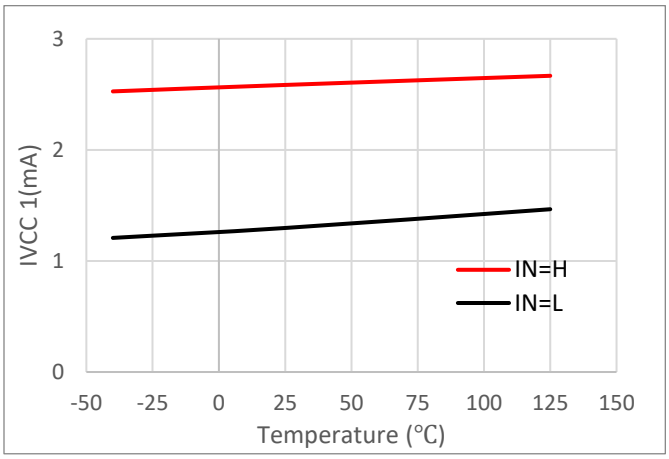


Figure 1. I_{VCC1} Supply Current vs Temperature

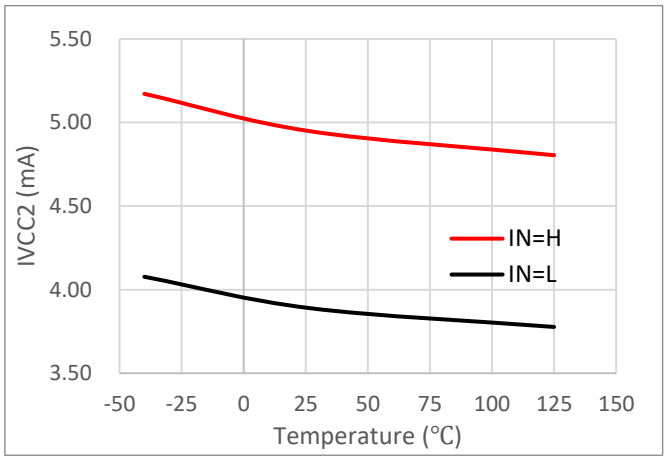


Figure 2. I_{VCC2} Supply Current vs Temperature

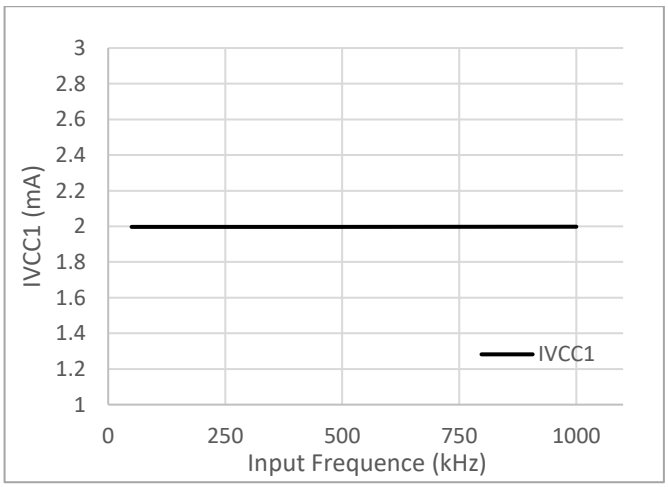


Figure 3. I_{VCC1} Supply Current vs Input Frequency

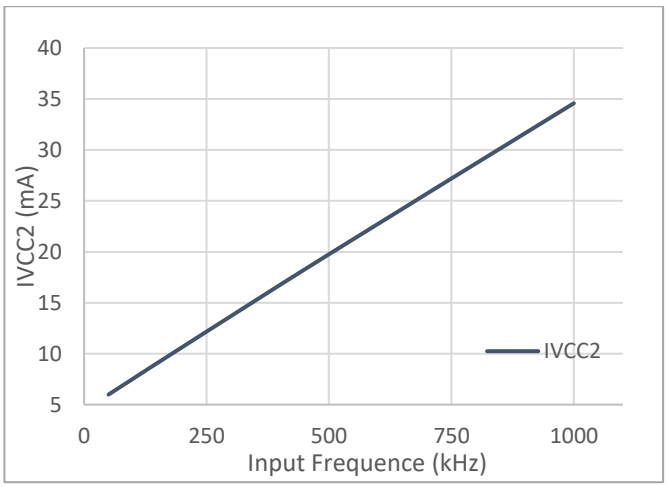


Figure 4. I_{VCC2} Supply Current vs Input Frequency

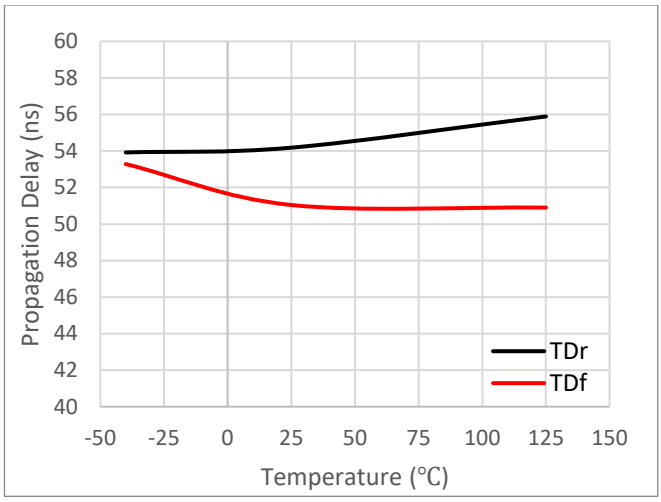


Figure 5. Propagation Delay vs Temperature

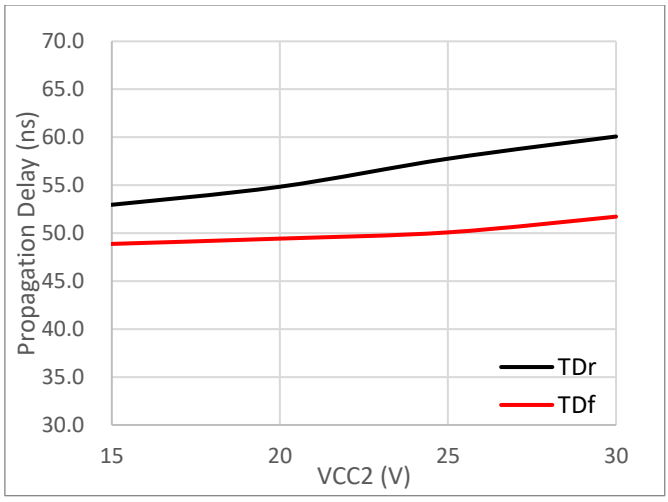


Figure 6. Propagation Delay vs VCC2

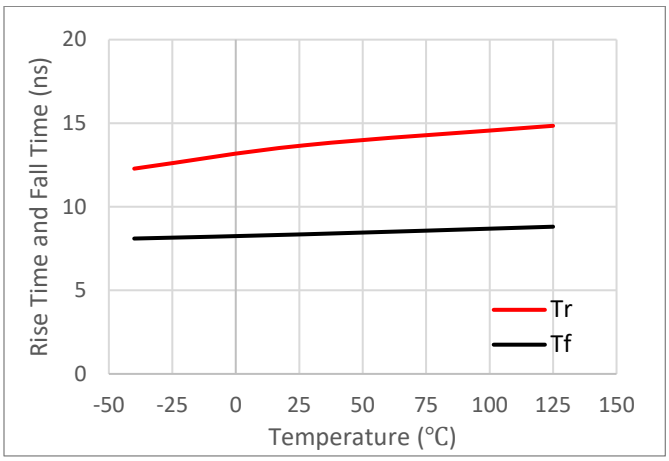


Figure 7. Rise Time and Fall Time vs Temperature

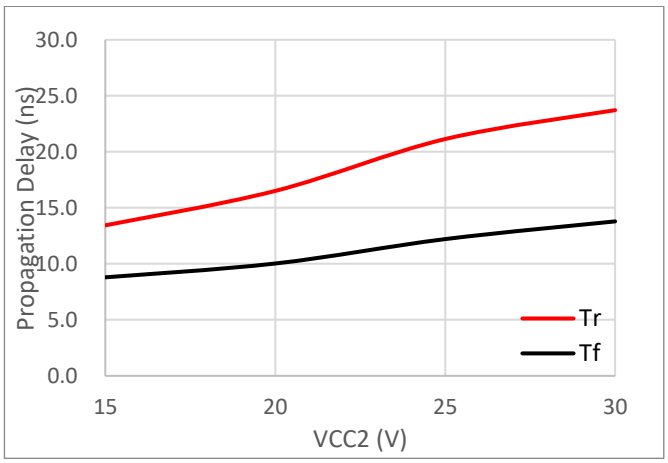


Figure 8. Rise Time and Fall Time vs VCC2

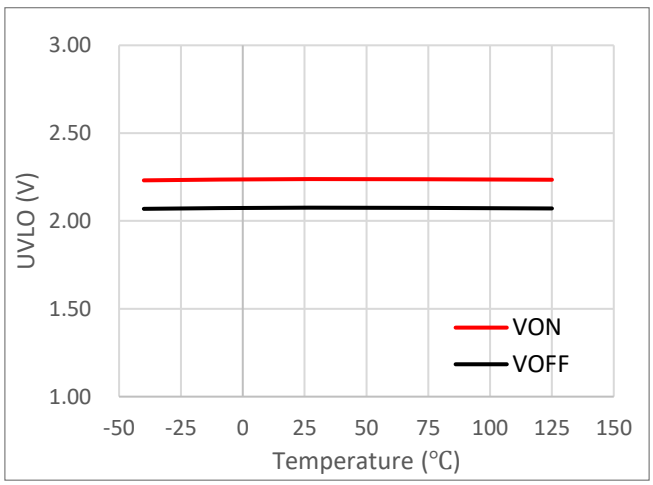


Figure 9. UVLO of VCC1 vs Temperature

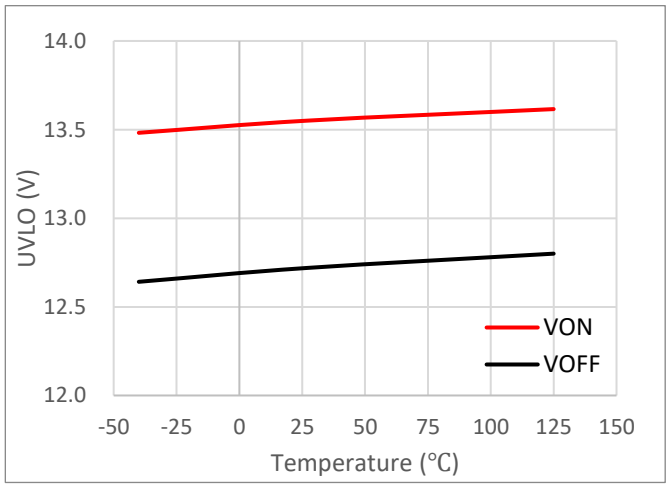


Figure 10. UVLO of VCC2 vs Temperature

7. Detail Descriptions

IVCO141x driver is a family of single-channel isolated gate drivers with 5.7kVrms insulation voltage. IVCO1411 features desaturation/short-circuit protection and UVLO. IVCO1412 features negative voltage generation and UVLO.

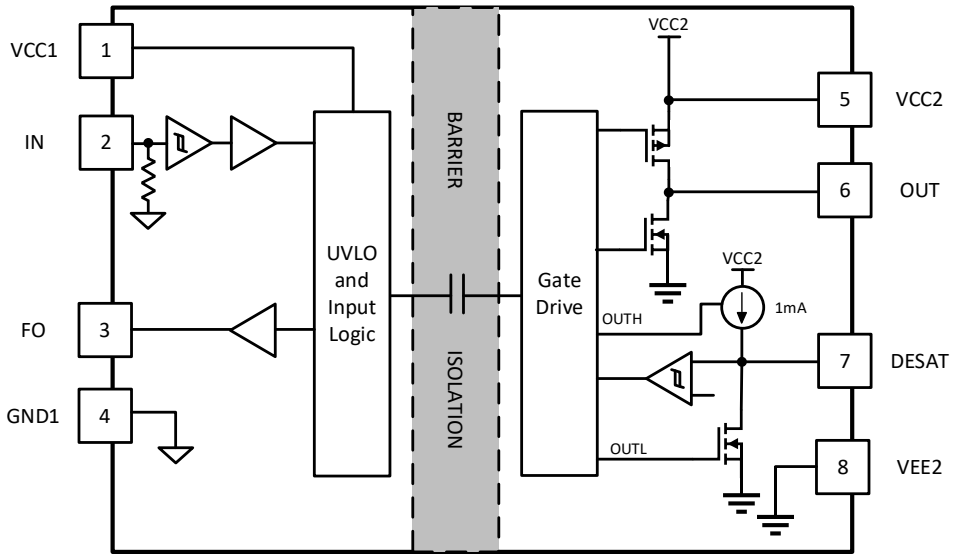


Figure 11. IVCO1411 Function Block Diagram

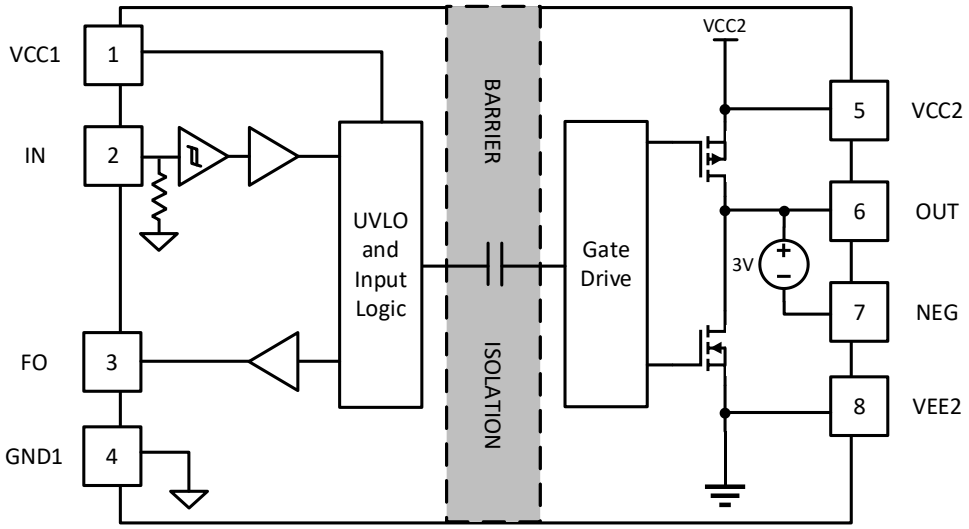


Figure 12. IVCO1412 Function Block Diagram

7.1 Input Signals

IN is a non-inverting logic gate driver input. The pin has a weak pulldown. When IN floating, output is pulled to VEE2. The input is a TTL and CMOS logic level with maximum 6V input tolerance.

7.2 Output Signals

IVCO141x features a 4A totem-pole output stage. The output voltage swings between VCC2 and VEE2 providing rail-to-rail operation. The presence of the MOSFET body diodes also offers voltage clamping paths to limit overshoot and undershoot. That means that in many cases, external Schottky diode clamps may not be necessary.

7.3 Negative Voltage Generation

At startup, NEG output is pulled to VEE2 and provides a high current path for a current source to charge the external negative-voltage capacitor CN (1uF typical) through OUT pin. The capacitor can be charged to above 1.8V in less than 100us. Before the capacitor voltage, V_{CN}, is charged up, FO stays low, disregarding IN's logic level. After the negative bias is ready, both NEG pin and FO pin are released and OUT starts to follow input signal IN. The gate drive signal, NEG, then switches between V_{CC2} - 3V and -3V.

7.4 VCC and Under Voltage Protection

IVCO141x maximum VCC1 voltage rating is 6V. The VCC1 internal under voltage lockout (UVLO) protection threshold voltage is 2.2V typical, which enables the input stage working with 2.5V, 3.3V or 5V supply voltages. When VCC1 level is below UVLO (VCC1) threshold, this device holds the output LOW, regardless of the status of the inputs.

IVCO141x maximum VCC2 voltage rating is 32V. It is suitable for Si MOSFET, IGBT and SiC MOSFET gate drive. The output stage has VCC2 internal under voltage lockout (UVLO) protection feature. When VCC2 level is below UVLO (VCC2) threshold, this circuit holds the output LOW, regardless of the status of the inputs.

7.5 Isolation and CMTI

IVCO141x provides insulation withstand voltage 5.7kVrms with SOIC(W)-8 package. This device is designed with capacitive isolation technique. The common-mode transient immunity (CMTI) 100V/ns ensures error-free operation when high dv/dt is present.

7.6 CMTI Measurement

Common mode transient immunity (CMTI), which can be distinguished between static and dynamic CMTI, is defined as the maximum tolerable rate of rise and fall of the common mode voltage applied between two isolated circuits. The measurement principle of the CMTI test is shown in figure 13.

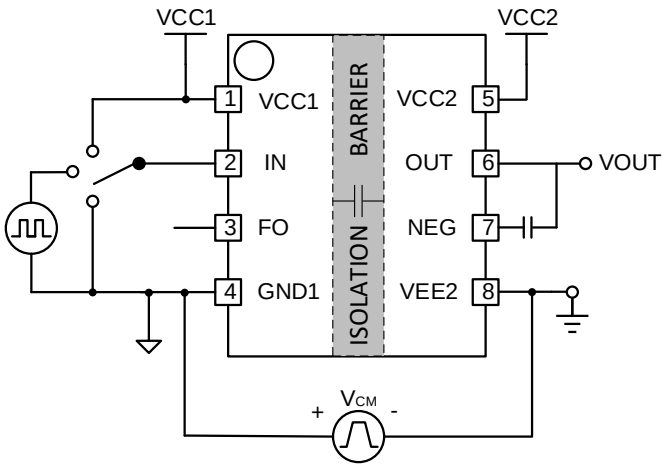


Figure 13. Common-mode transient immunity (CMTI) measurement

7.7 Desaturation Detection

When short circuit or over current happens, the power device's (SiC MOSFET or IGBT) drain or collector current can increase to such a high value that the devices get out of saturation state, and Vds/Vce of the devices will rise to a substantially high value. DESAT pin with a blanking capacitor Cblk, normally clamped to Id x Rds_on, now is able to charge up much higher by an internal 1mA constant current source. When the voltage reaches typical 9.8V threshold, OUT and FO are both pulled low. A 220ns blank time is inserted at OUT rising edge to prevent DESAT protect circuit from being triggered prematurely due to Coss discharge. To minimize the loss of internal constant current source, the current source is turned off when the main switch is at off state. By selecting a different capacitance, turn-off delay time (external blanking time) can be programmed. The blanking time can be calculated with,

$$T_{eblk} = C_{blk} \cdot V_{th} / I_{DESAT}$$

For example, if C_{blk} is 47pF, T_{eblk} = 47pF ·9.8V / 1mA = 461ns.

Note T_{eblk} includes internal T_{blk} 220ns blanking time already.

For current limit setting, the following equation can be used,

$$I_{limit} = (V_{th} – R1* I_{DESAT} – V_{F\_D1})/ R_{ds\_on}$$

where R1 is a programming resistor connecting between the blanking capacitor and the high voltage diode, V_{F_D1} is the high voltage diode forward voltage, R_{ds_on} is SiC MOSFET turn-on resistance at estimated junction temperature, such as 175℃.

A different power system usually requires a different turn-off time. An optimized turn-off time can maximize the system short circuit capability while limiting Vds and bus voltage ringing.

7.8 FO

IVCO1411: When desaturation or under voltages are detected, the FO pin and OUT are both pulled low. The FO signal will stay at low for 13us when the fault condition is detected. After 13us, when IN becomes low, FO returns to high.

IVCO1412: When under voltages are detected, the FO and OUT will be pulled low.

7.9 NEG

The external negative bias capacitor is quickly charged up at power up. After power up, the charging current is reduced. During the charging time, the negative bias capacitor voltage V_{CN} is measured. As soon as the voltage is beyond about 1.8V, NEG becomes high-impedance and OUT takes over gate drive control.

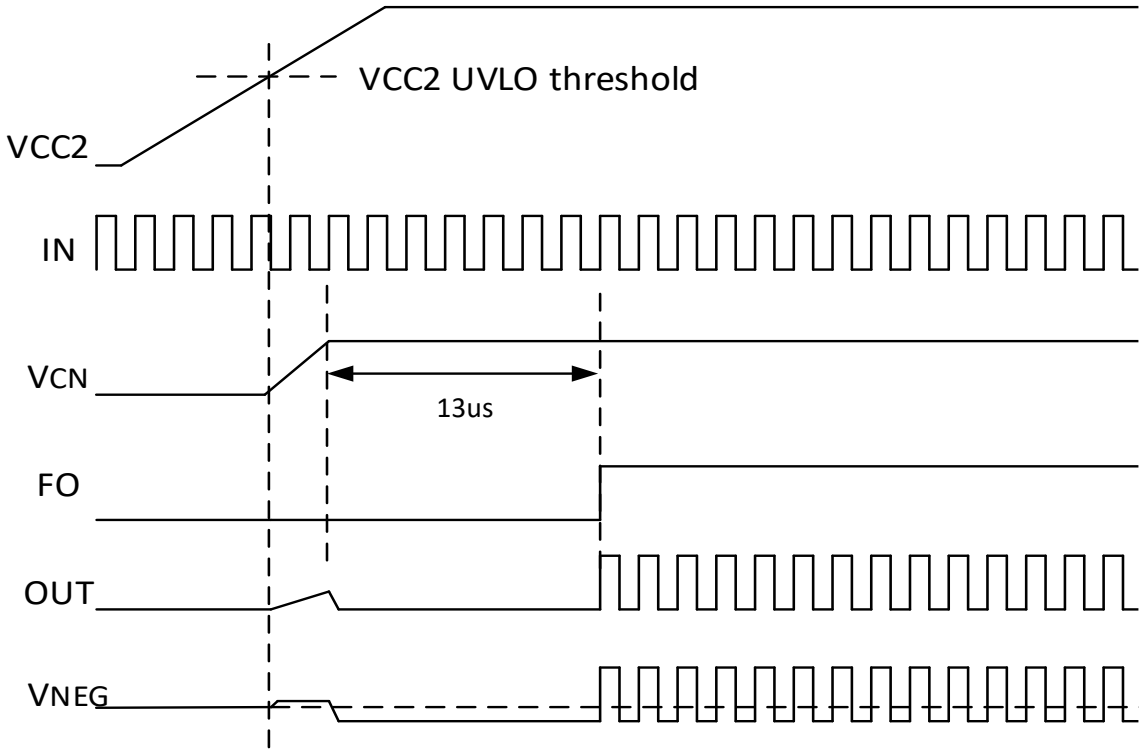


Figure 14. Power Up Sequence for IVCO1412

8. Application Implementation

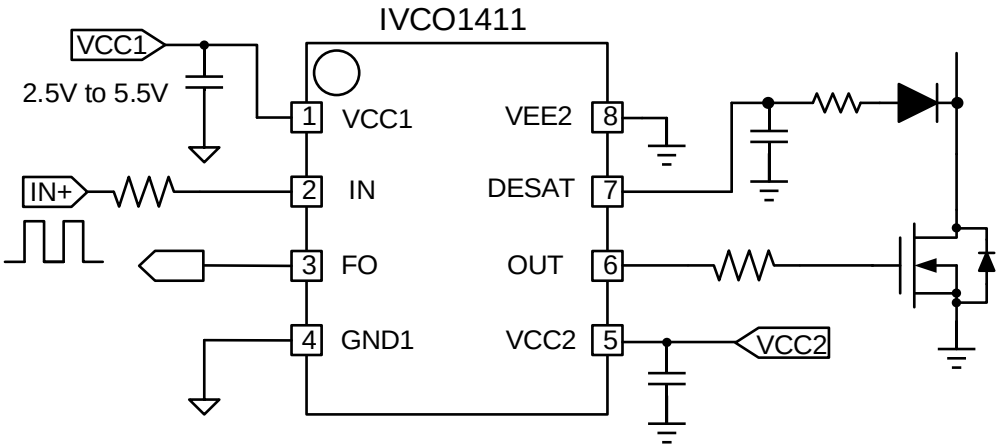


Figure 15. IVCO1411 Typical Application Circuit

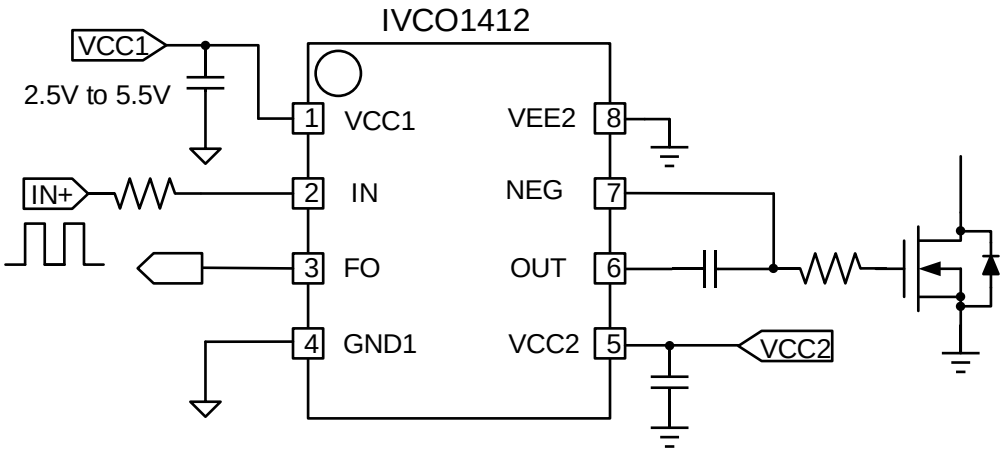


Figure 16. IVCO1412 Typical Application Circuit

9. Layout

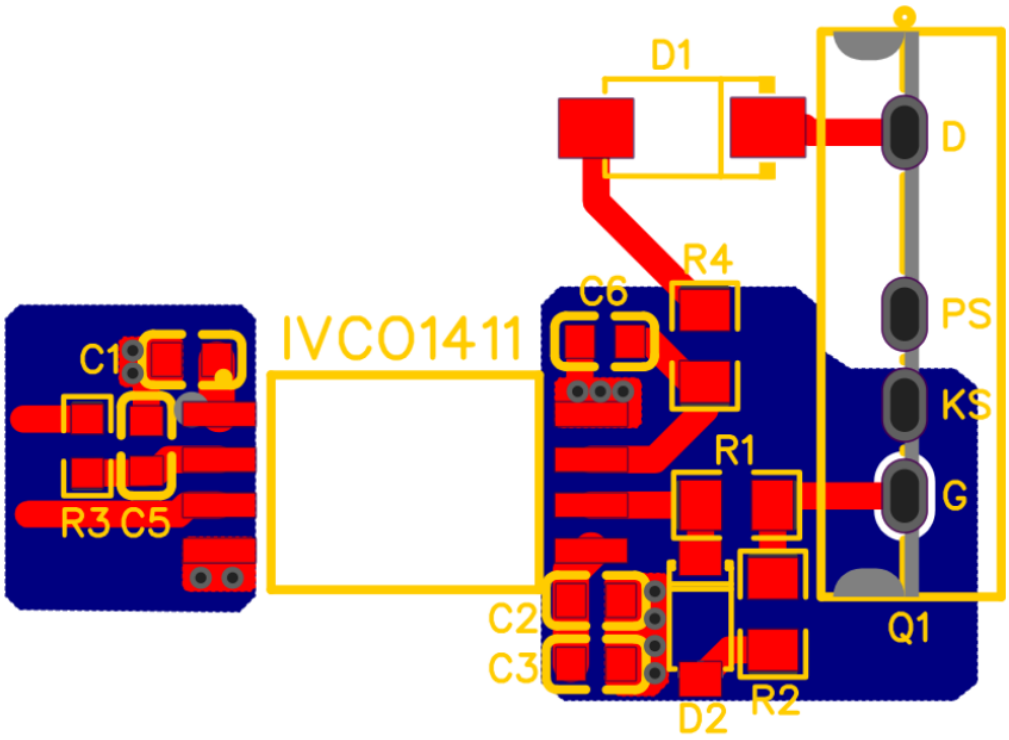


Figure 17. IVCO1411 Layout Example

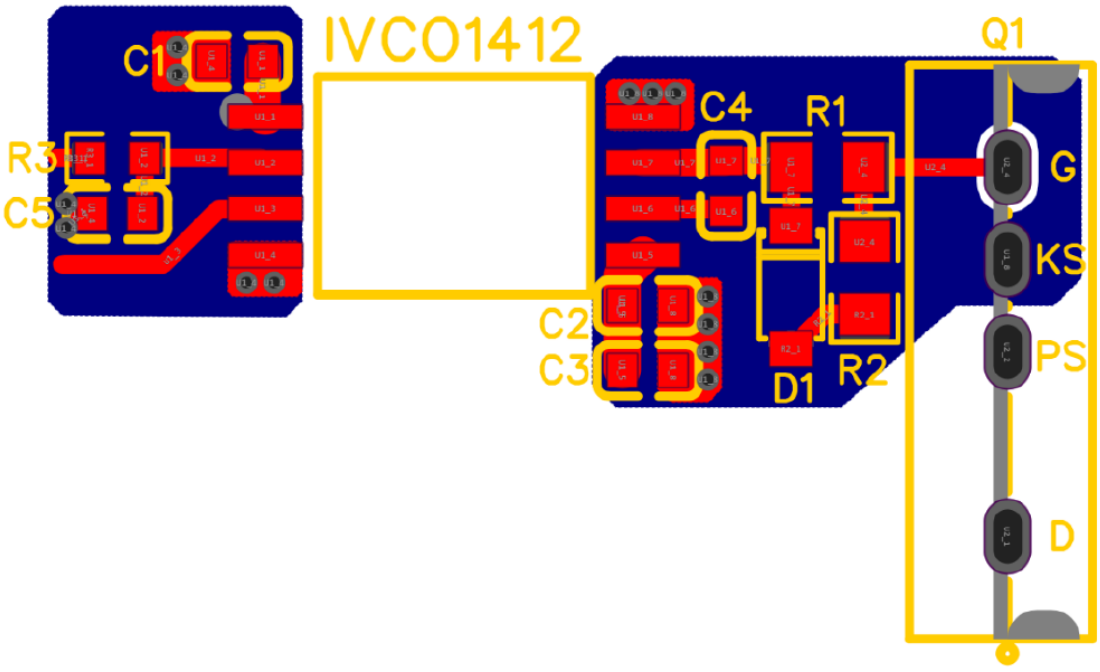
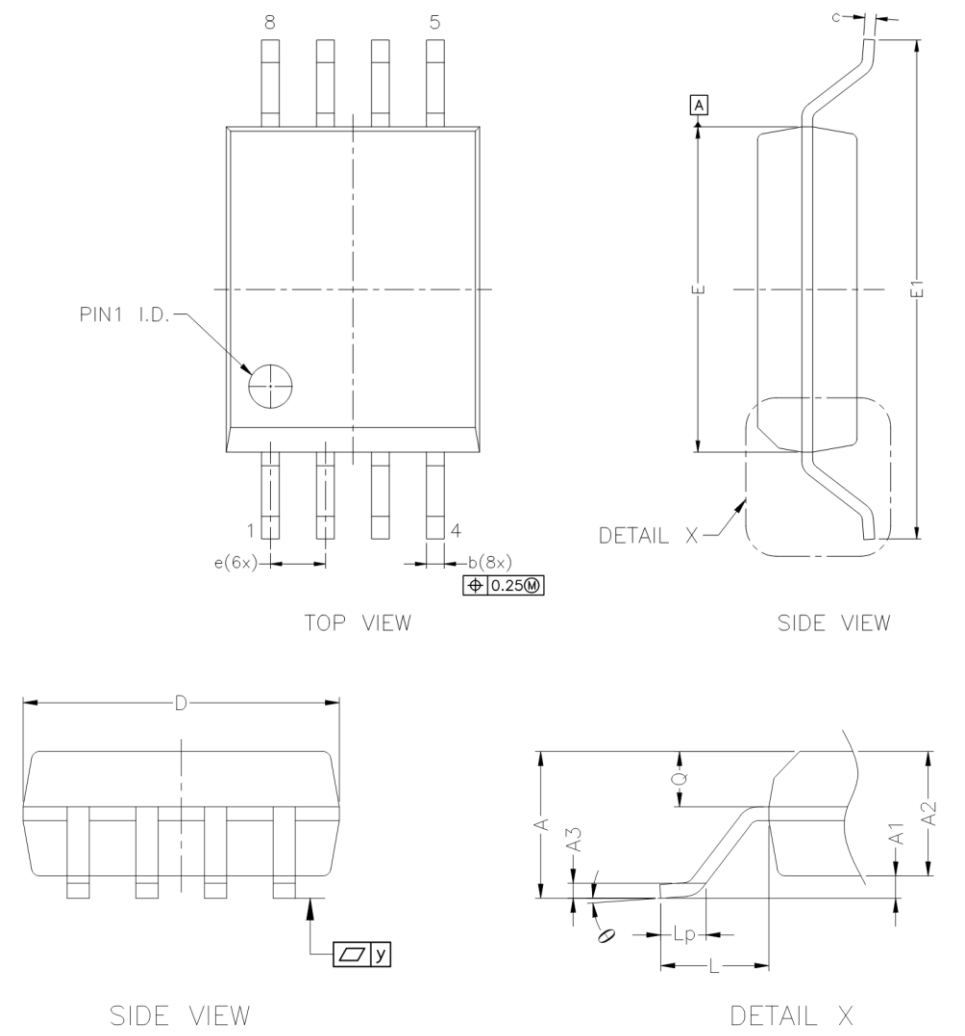


Figure 18. IVCO1412 Layout Example

10. Package information

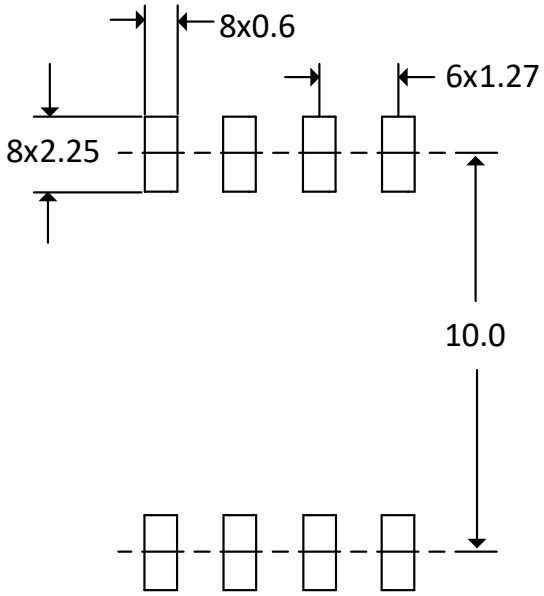
8-Lead Wide Body SOIC [DW]



* CONTROLLING DIMENSION : MM

SYMBOL	MM		
	MIN.	NOM.	MAX.
A	--	--	2.80
A1	0.36	--	0.46
A2	2.20	2.30	2.40
A3	--	0.25	--
Q	0.97	1.02	1.07
b	0.31	0.41	0.51
c	0.13	--	0.33
D	5.75	5.85	5.95
E	7.40	7.50	7.60
E1	11.25	11.50	11.75
e	1.27 bsc		
L	2.00 bsc		
Lp	0.50	--	1.00
y	--	0.10	--
θ	0°	--	8°

SOIC(W)-8 Package Dimensions (mm)



SOIC(W)-8 Recommended Soldering Dimensions (mm)

单击下面可查看定价，库存，交付和生命周期等信息

>>Inventchip(瞻芯电子)