

150V, 54A, 16mΩ N-channel Power SGT MOSFET
JMSH1516PG
Features

- Excellent $R_{DS(ON)}$ and Low Gate Charge
- 100% UIS Tested
- 100% ΔV_{ds} Tested
- Halogen-free; RoHS-compliant

Applications

- Load Switch
- PWM Application
- Power Management

Product Summary

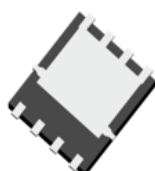
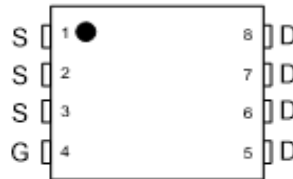
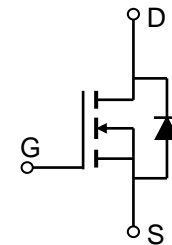
Parameters	Value	Unit
V_{DSS}	150	V
$V_{GS(th_Typ)}$	3.1	V
$I_D(@V_{GS}=10V)$	54	A
$R_{DS(ON_Typ)}(@V_{GS}=10V)$	16	mΩ



Top View



Bottom View


PDFN5X6-8L

Pin Assignment

Schematic Diagram
Ordering Information

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMSH1516PG-13	SH1516P	1	Tape&Reel	PDFN5x6-8L	5000	50000

Absolute Maximum Ratings (@ $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-to-Source Voltage	150	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Continuous Drain Current	$T_C = 25^\circ\text{C}$	54
		$T_C = 100^\circ\text{C}$	34
I_{DM}	Pulsed Drain Current ⁽¹⁾	Refer to Fig.4	A
E_{AS}	Single Pulsed Avalanche Energy ⁽²⁾	238	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	125
		$T_C = 100^\circ\text{C}$	50
T_J, T_{STG}	Junction & Storage Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	Max	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	43	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	

**Electrical Characteristics** ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	150	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120\text{V}, V_{GS} = 0\text{V}$	-	-	1.0	μA
I_{GSS}	Gate-Body Leakage Current	$V_{DS} = 0\text{V}, V_{GS} = \pm 20\text{V}$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.1	3.1	4.0	V
$R_{DS(ON)}$	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10\text{V}, I_D = 20\text{A}$	-	16	20	m Ω
Dynamic Characteristics						
R_g	Gate Resistance	$f = 1\text{MHz}$	-	0.7	-	Ω
C_{iss}	Input Capacitance	$V_{GS} = 0\text{V}, V_{DS} = 75\text{V},$ $f = 1\text{MHz}$	1635	2290	3091	pF
C_{oss}	Output Capacitance		150	210	284	pF
C_{rss}	Reverse Transfer Capacitance		13	18	24	pF
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ to } 10\text{V}$ $V_{DS} = 75\text{V}, I_D = 20\text{A}$	23	32	43	nC
Q_{gs}	Gate Source Charge		9	13	17	nC
Q_{gd}	Gate Drain("Miller") Charge		-	6	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On DelayTime	$V_{GS} = 10\text{V}, V_{DD} = 75\text{V}$ $I_D = 20\text{A}, R_{GEN} = 3\Omega$	-	15	-	ns
t_r	Turn-On Rise Time		-	19	-	ns
$t_{d(off)}$	Turn-Off DelayTime		-	22	-	ns
t_f	Turn-Off Fall Time		-	5	-	ns
Body Diode Characteristics						
I_S	Maximum Continuous Body Diode Forward Current		-	-	54	A
I_{SM}	Maximum Pulsed Body Diode Forward Current		-	-	215	A
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 20\text{A}$	-		1.2	V
t_{rr}	Body Diode Reverse Recovery Time	$I_F = 20\text{A}, di/dt = 100\text{A}/\mu\text{s}$	57	80	108	ns
Q_{rr}	Body Diode Reverse Recovery Charge		-	205	-	nC

- Notes:
1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.
 2. E_{AS} condition: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 75\text{V}$, $V_{GS} = 10\text{V}$, $R_G = 25\text{ohm}$, $L = 3\text{mH}$, $I_{AS} = 30.1\text{A}$, $V_{DD} = 0\text{V}$ during time in avalanche.
 3. $R_{\theta JA}$ is measured with the device mounted on a 1inch^2 pad of 2oz copper FR4 PCB.
 4. Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 0.5\%$.



Typical Performance Characteristics

Figure 1: Power De-rating

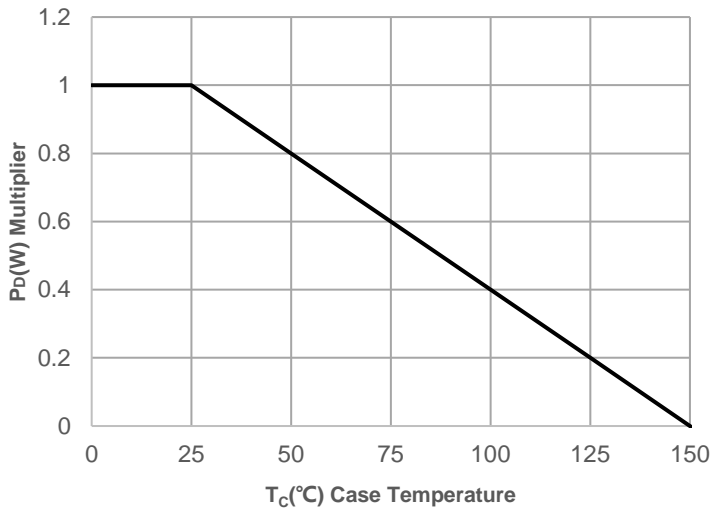


Figure 2: Current De-rating

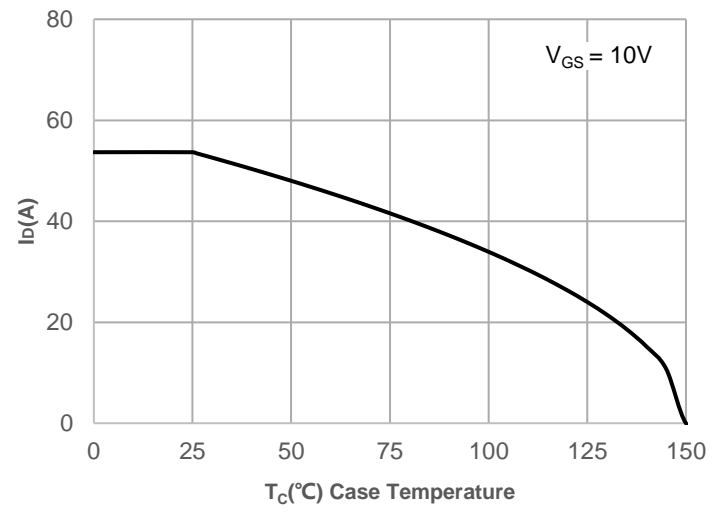


Figure 3: Normalized Maximum Transient Thermal Impedance

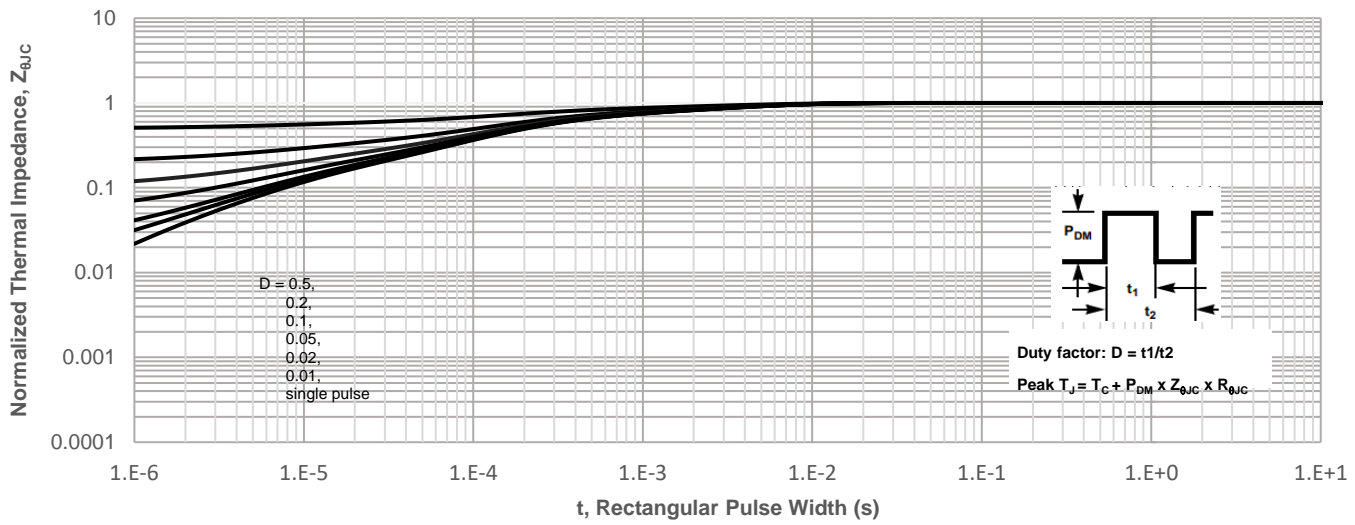
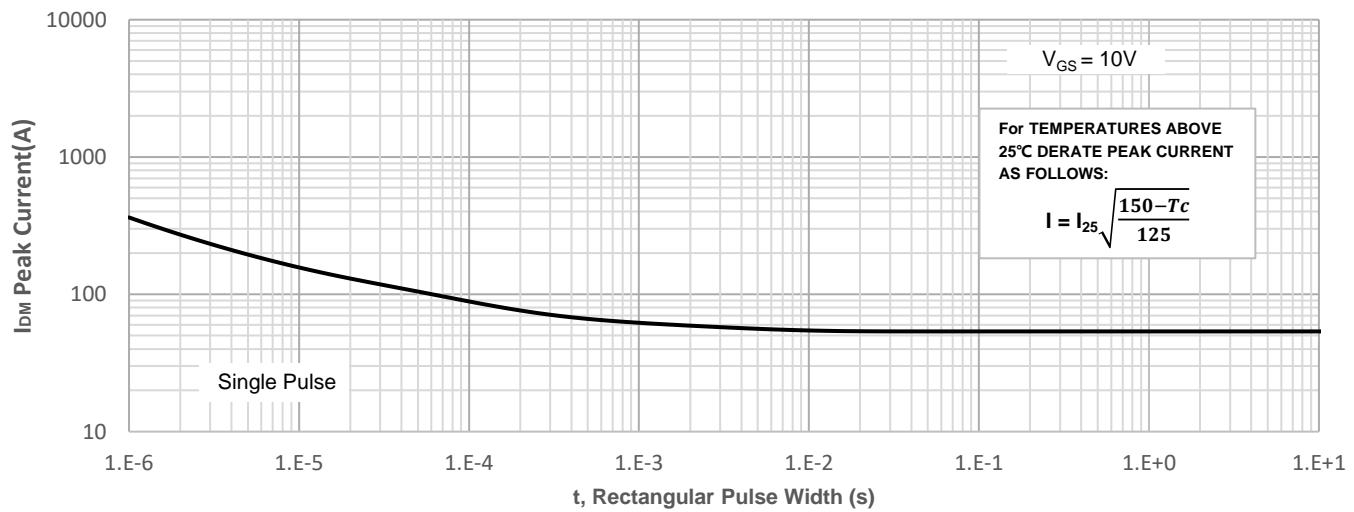
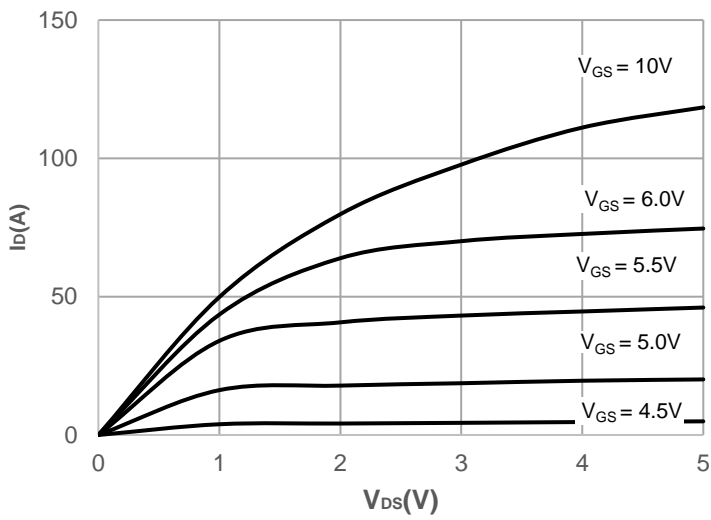
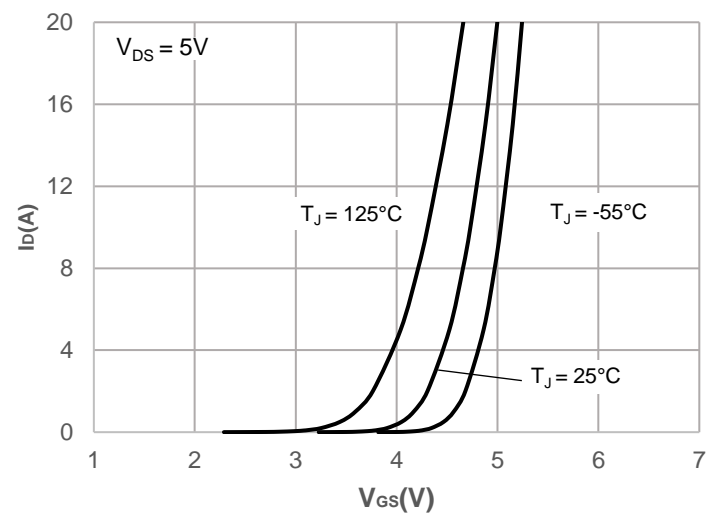
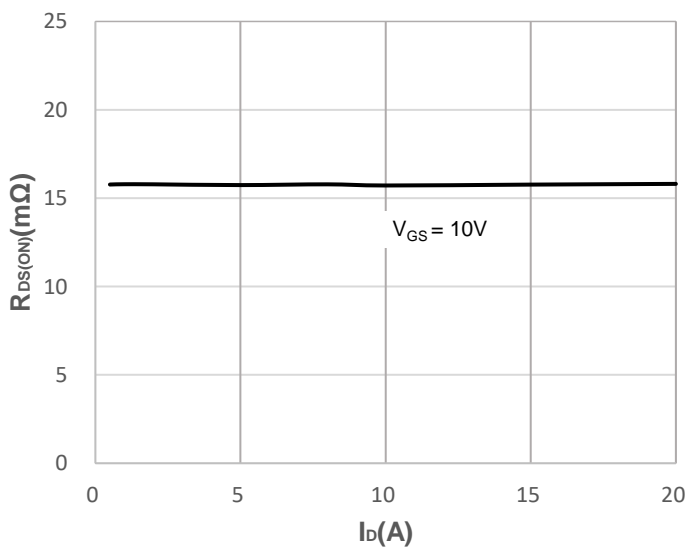
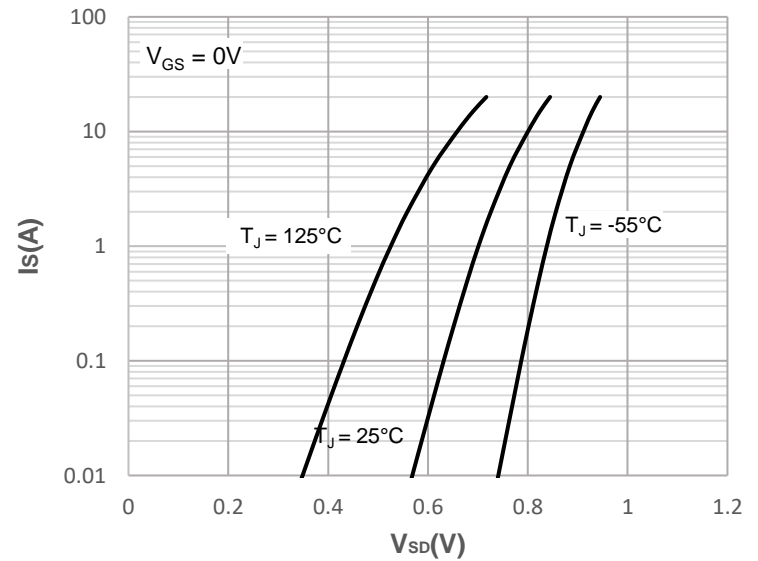
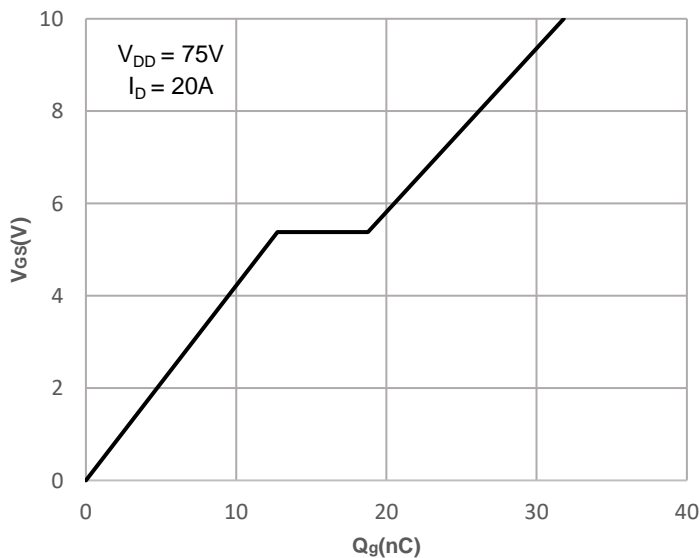
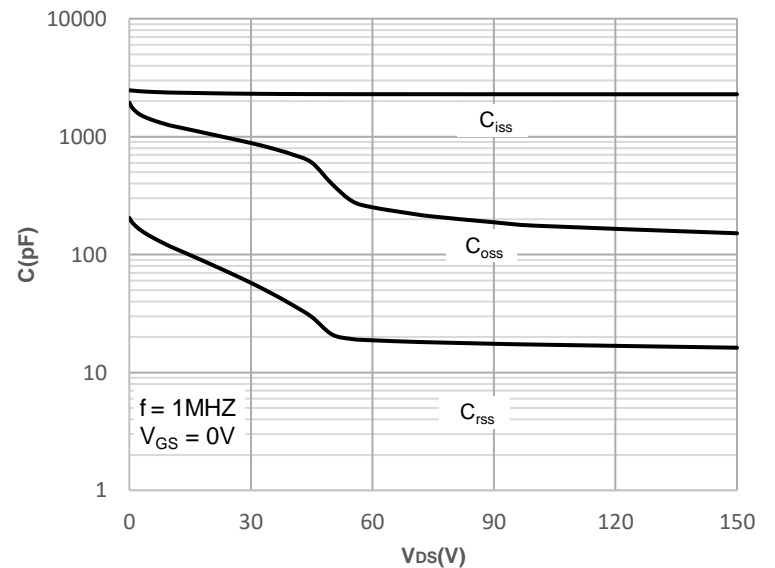


Figure 4: Peak Current Capacity



Typical Performance Characteristics

Figure 5: Output Characteristics

Figure 6: Typical Transfer Characteristics

Figure 7: On-resistance vs. Drain Current

Figure 8: Body Diode Characteristics

Figure 9: Gate Charge Characteristics

Figure 10: Capacitance Characteristics


Typical Performance Characteristics

Figure 11: Normalized Breakdown voltage vs. Junction Temperature

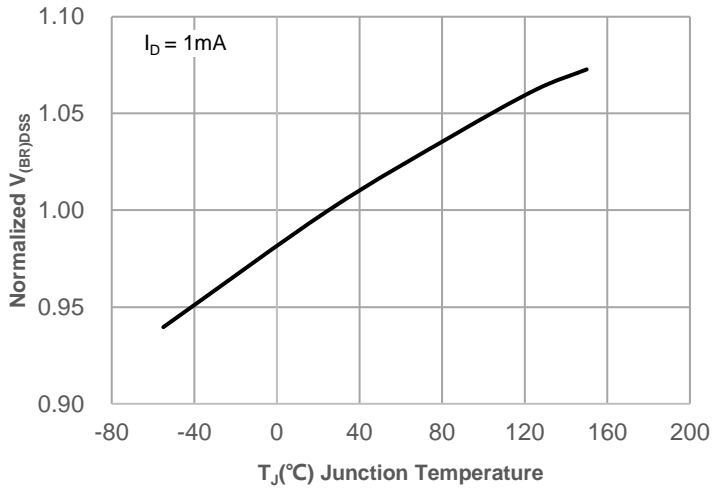


Figure 12: Normalized on Resistance vs. Junction Temperature

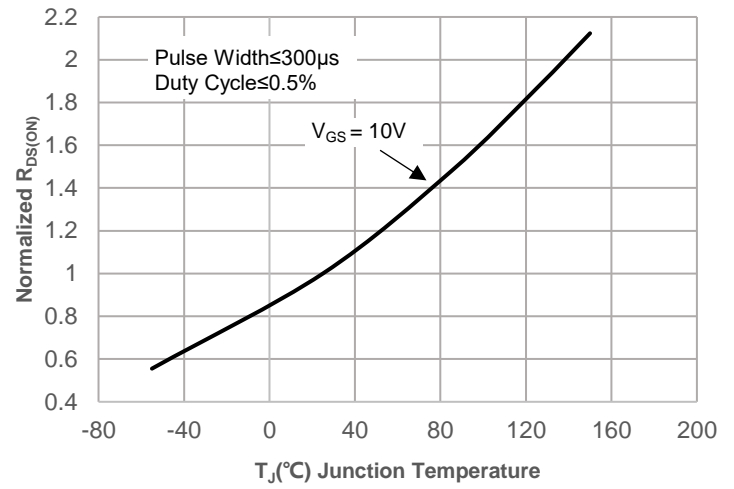


Figure 13: Normalized Threshold Voltage vs. Junction Temperature

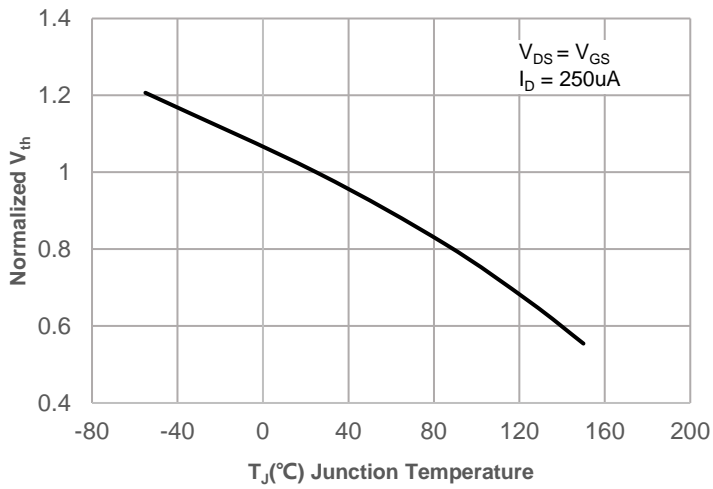


Figure 14: $R_{DS(ON)}$ vs. V_{GS}

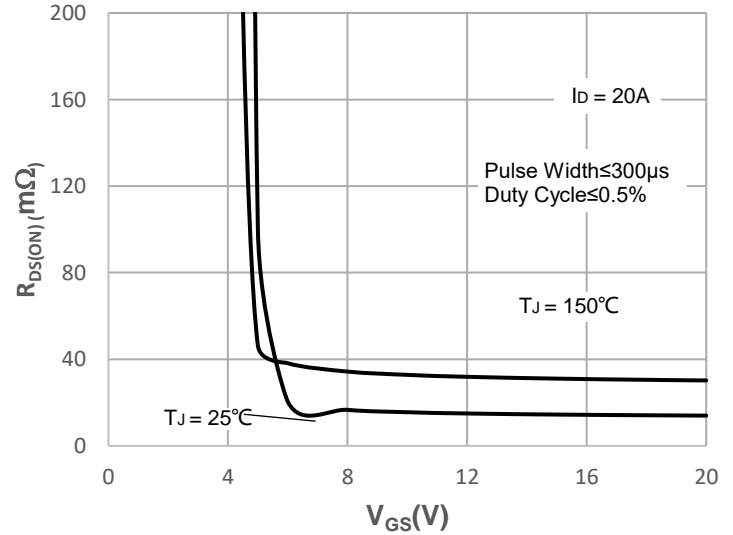
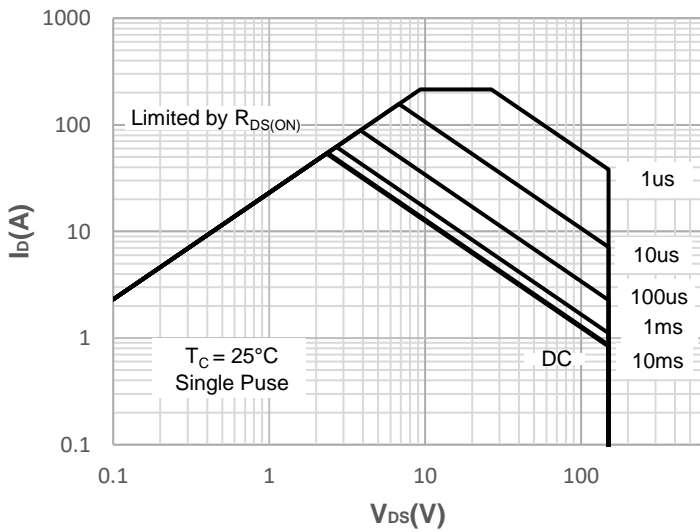


Figure 15: Maximum Safe Operating Area



Test Circuit



Figure 1: Gate Charge Test Circuit & Waveform

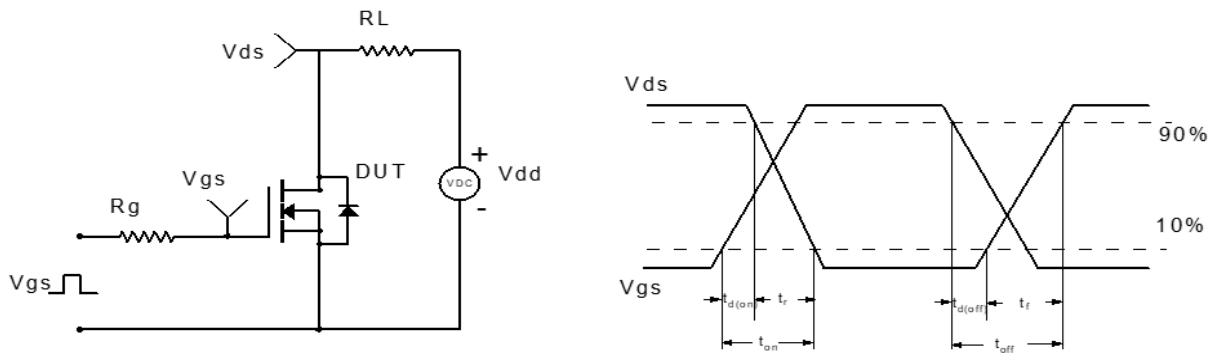


Figure 2: Resistive Switching Test Circuit & Waveform

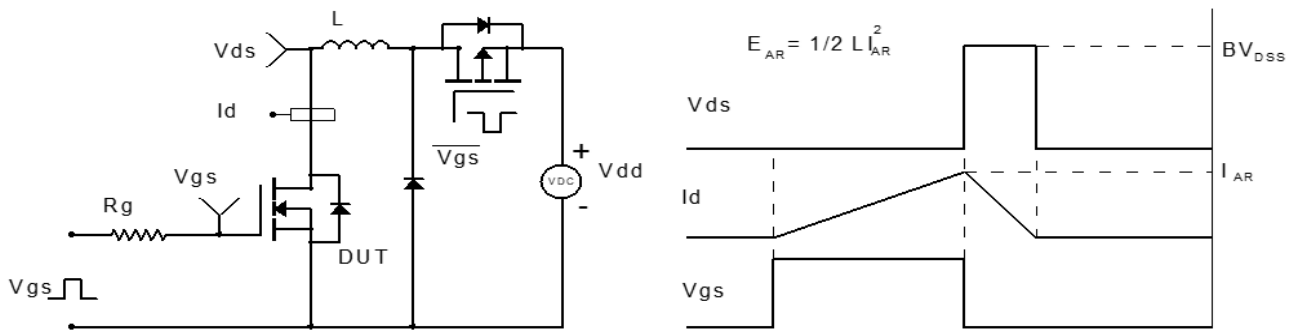


Figure 3: Unclamped Inductive Switching Test Circuit & Waveform

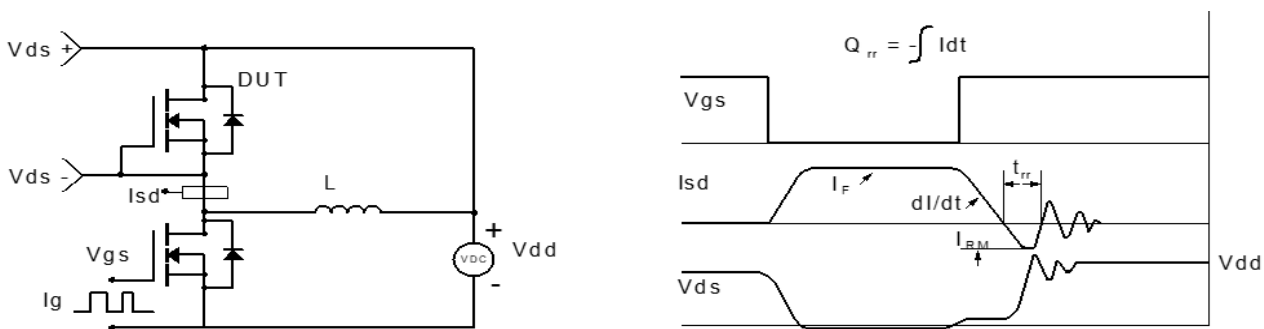
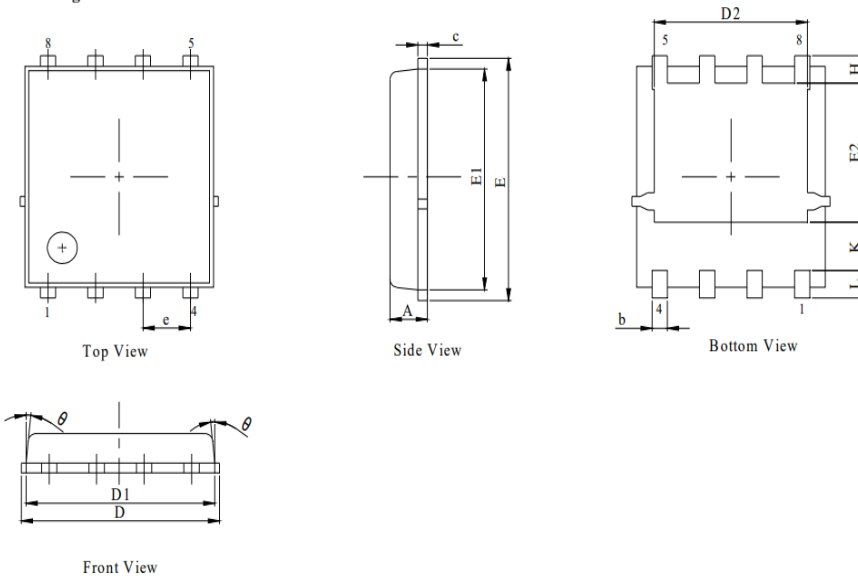


Figure 4: Diode Recovery Test Circuit & Waveform



Package Mechanical Data(PDFN5x6-8L)

Package Outline

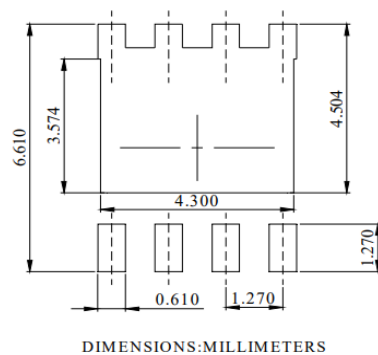


NOTES:

1. Dimension and tolerance per ASME Y14.5M, 1994.
2. All dimensions in millimeter (angle in degree).
3. Dimensions D1 and E1 do not include mold flash protrusions or gate burrs.

DIM.	MILLIMETER		
	MIN.	NOM.	MAX.
A	0.9	1	1.15
b	0.31	0.41	0.51
C	0.24	0.32	0.4
D	5	5.2	5.4
D1	4.95	5.05	5.15
D2	4	4.1	4.2
E	6.05	6.15	6.25
E1	5.5	5.6	5.7
E2	3.42	3.53	3.63
e	1.27BSC		
H	0.6	0.7	0.8
L	0.5	0.7	0.8
K	1.23 REF		
0			10

Recommended Soldering Footprint



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