

Description

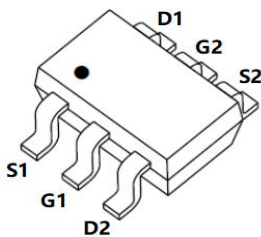
JMT N-channel Enhancement Mode Power MOSFET

Features

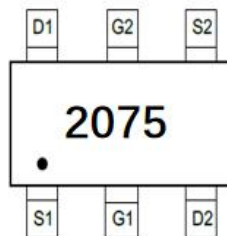
- 20V, 0.9A
 $R_{DS(ON)} < 175m\Omega @ V_{GS} = 4.5V$
 $R_{DS(ON)} < 275m\Omega @ V_{GS} = 2.5V$
- Advanced Trench Technology
- Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired
- ESD Protected: 2KV

Application

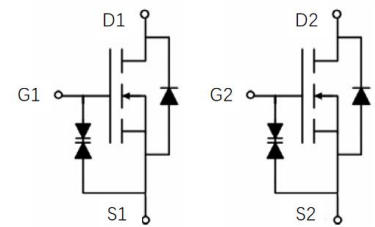
- Load Switch
- PWM Application
- Power management



SOT-363-6L (Dual) top view



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
2075	JMTLB3134K	TAPING	SOT-363-6L	7inch	3000	120000

Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 10	V
I_D	Continuous Drain Current	$T_A = 25^\circ C$	0.9
		$T_A = 100^\circ C$	0.6
I_{DM}	Pulsed Drain Current <small>note1</small>	3.6	A
P_D	Power Dissipation	$T_A = 25^\circ C$	0.23
$R_{\theta JA}$	Thermal Resistance, Junction to Case	543	$^\circ C/W$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



Electrical Characteristics (T_J=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V,	-	-	1	μA
I _{GSS}	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±10V	-	-	±10	uA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.4	0.7	1.0	V
R _{DS(on)}	Static Drain-Source on-Resistance <small>note2</small>	V _{GS} =4.5V, I _D =0.5A	-	135	240	mΩ
		V _{GS} =2.5V, I _D =0.4A	-	195	280	
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1.0MHz	-	60	-	pF
C _{oss}	Output Capacitance		-	22	-	pF
C _{rss}	Reverse Transfer Capacitance		-	12	-	pF
Q _g	Total Gate Charge	V _{DS} =10V, I _D =0.9A, V _{GS} =4.5V	-	1	-	nC
Q _{gs}	Gate-Source Charge		-	0.28	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	0.22	-	nC
Switching Characteristics						
t _{d(on)}	Turn-on Delay Time	V _{DS} =10V, I _D =0.5A, R _{GEN} =10Ω, V _{GS} =4.5V	-	2	-	ns
t _r	Turn-on Rise Time		-	19	-	ns
t _{d(off)}	Turn-off Delay Time		-	10	-	ns
t _f	Turn-off Fall Time		-	23	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	0.9	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	3.6	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =0.9A	-	-	1.2	V

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%



Typical Performance Characteristics

Figure 1: Output Characteristics

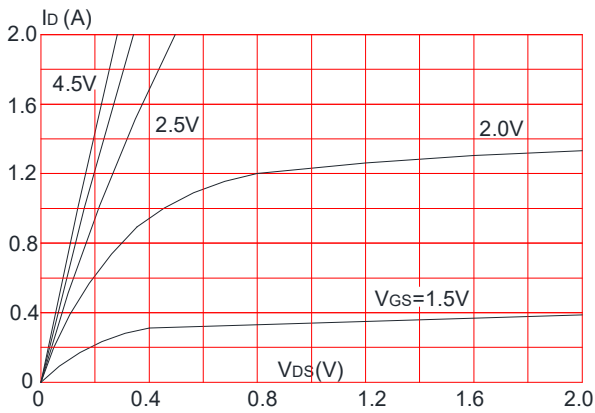


Figure 2: Typical Transfer Characteristics

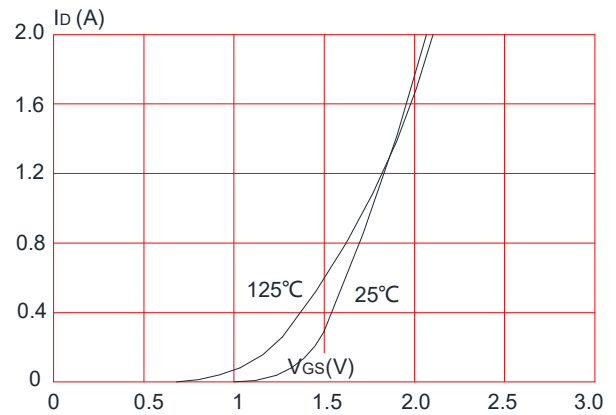


Figure 3: On-resistance vs. Drain Current

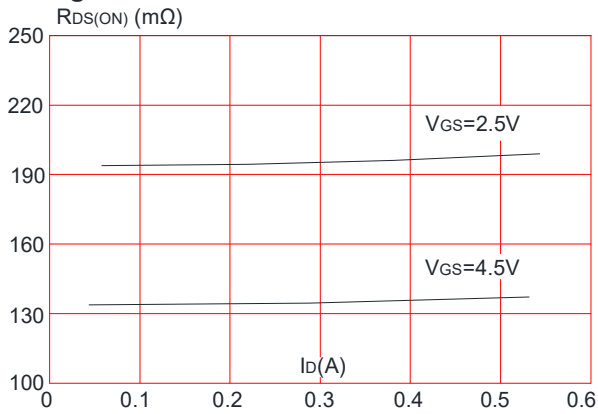


Figure 4: Body Diode Characteristics

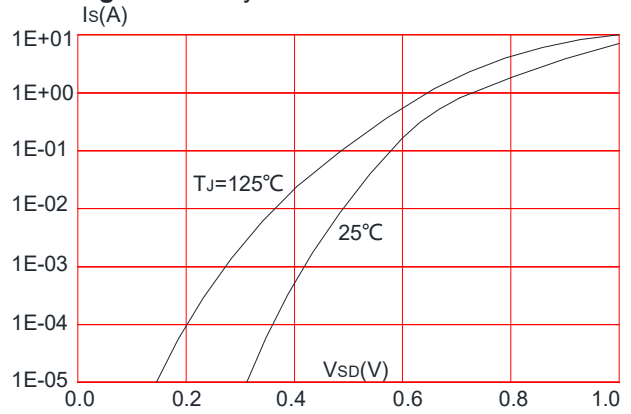


Figure 5: Gate Charge Characteristics

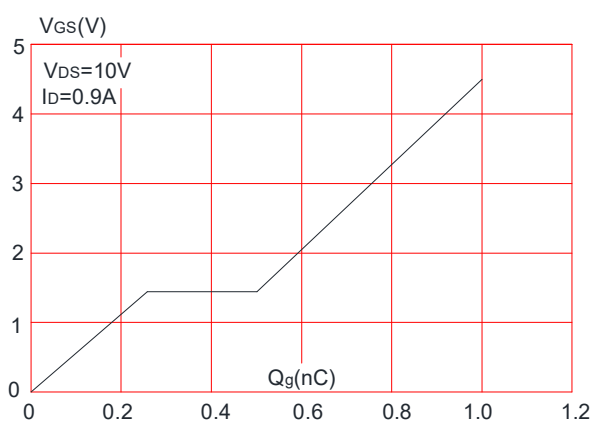


Figure 6: Capacitance Characteristics

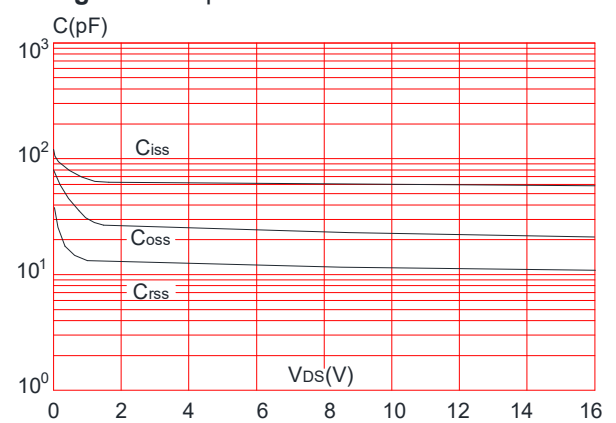




Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

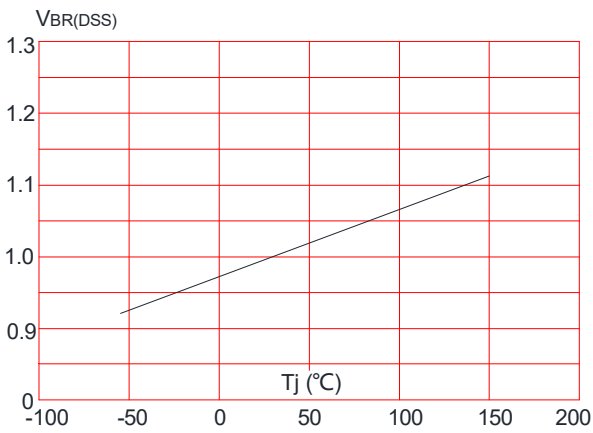


Figure 8: Normalized on Resistance vs. Junction Temperature

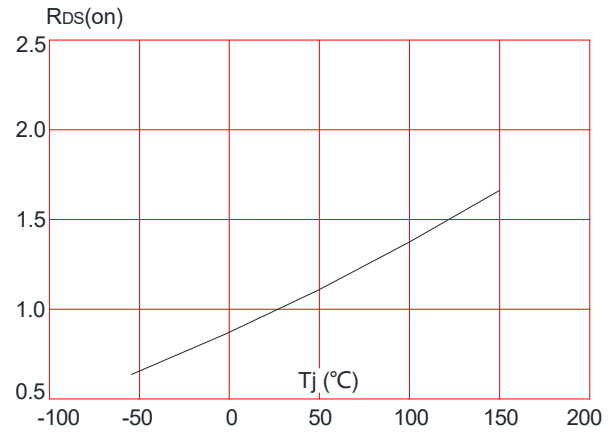


Figure 9: Maximum Safe Operating Area

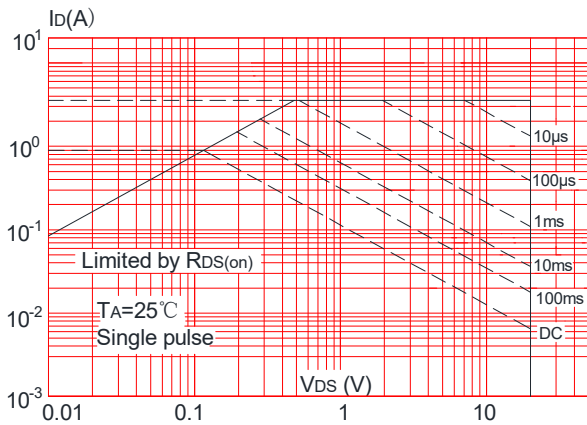


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

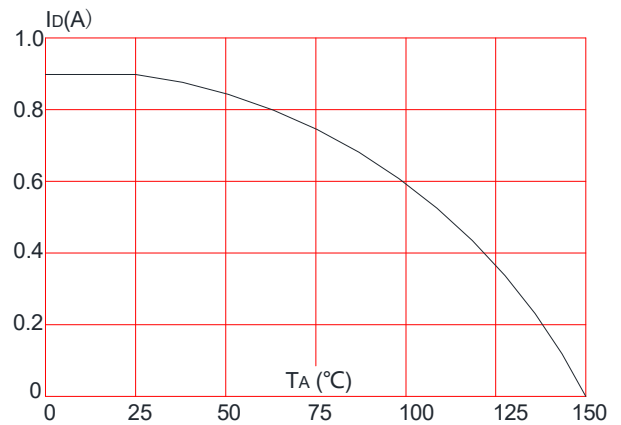
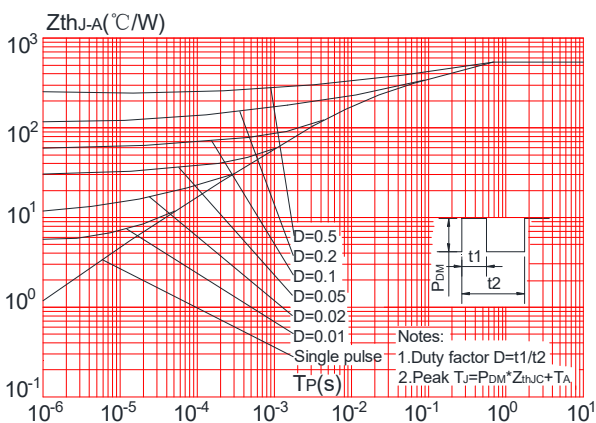


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit



Figure1:Gate Charge Test Circuit & Waveform



Figure 2: Resistive Switching Test Circuit & Waveforms

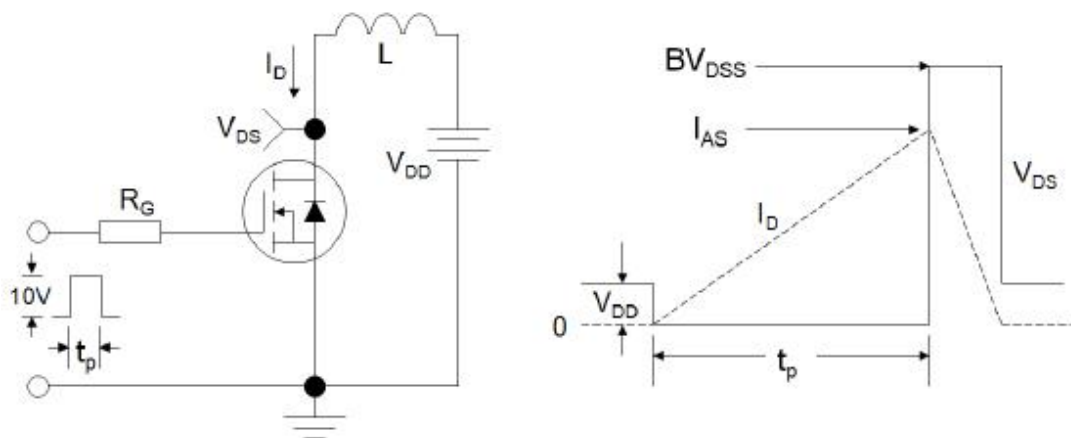
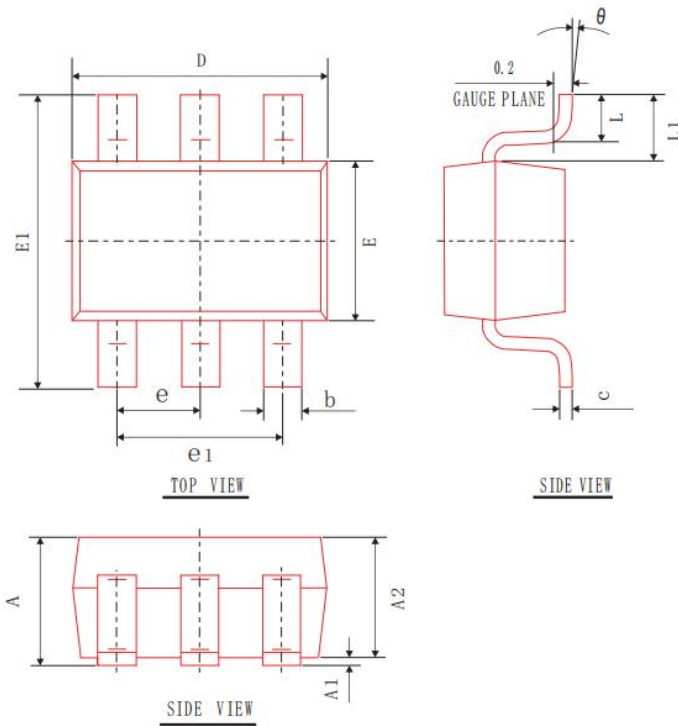


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



Package Mechanical Data-SOT-363-6L



COMMON DIMENSIONS
(UNITS OF MEASURE=mm)

SYMBOL	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.90	0.95	1.00
b	0.20	0.25	0.30
c	0.08	0.10	0.15
e1	1.20	1.30	1.40
D	2.00	2.10	2.20
E	1.15	1.25	1.35
E1	2.15	2.30	2.45
L	0.26	0.36	0.46
θ	0°	4°	8°
L1	0.525 REF		
e	0.65 TYP		

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