Anti-parallel Module

Rev.1.3 Feb.24 2023

JS151KQ

Description

1)A package consists of two inverse parallel SCR chips,
which non-repetitive peak off-state voltage is up to 2000V
2) Welding by vacuum welding technology, which provide high reliability
3) Insulated by silicone gel, provide a insulation voltage of 3000V~

V1-A-Pack

Typical Application

Soft start, solid state relay, AC/DC switch, temperature control.

Absolute Maximum Ratings (Packaged into V1-A-Pack, unless otherwise specified, T_{CASE}=25℃)

Parameter	Test Conditions	Symbol	Values			Unit
			12	16	18	
Operating junction temperature range		T_j	-40-125			℃
Storage temperature range		T_{stg}	-40-125			℃
Repetitive peak off-state voltage	T_j=25℃	V_{DRM}	1200	1600	1800	V
Repetitive peak reverse voltage	T_j=25℃	V_{RRM}	1200	1600	1800	V
Non-repetitive peak off-state voltage	T_j=25℃	V_{DSM}	1300	1700	1900	V
Non-repetitive peak reverse voltage	T_j=25℃	V_{RSM}	1300	1700	1900	V
RMS on-state current	T_C=85℃	$I_{T(RMS)}$	150			A
Peak on-state surge current	t_P=10ms V_R=0.6V_{RRM}	I_{TSM}	2200			A
I^2t value for fusing	t_P=10ms V_R=0.6V_{RRM}	I^2t	24200			A^2s
Critical rate of rise of on-state current	I_G=2×I_{GT}	di/dt	150			A/μs
Insulation voltage	A.C 50Hz(1s/1min)	V_{ISO}	3600/3000			V

Downloaded From Oneyac.com

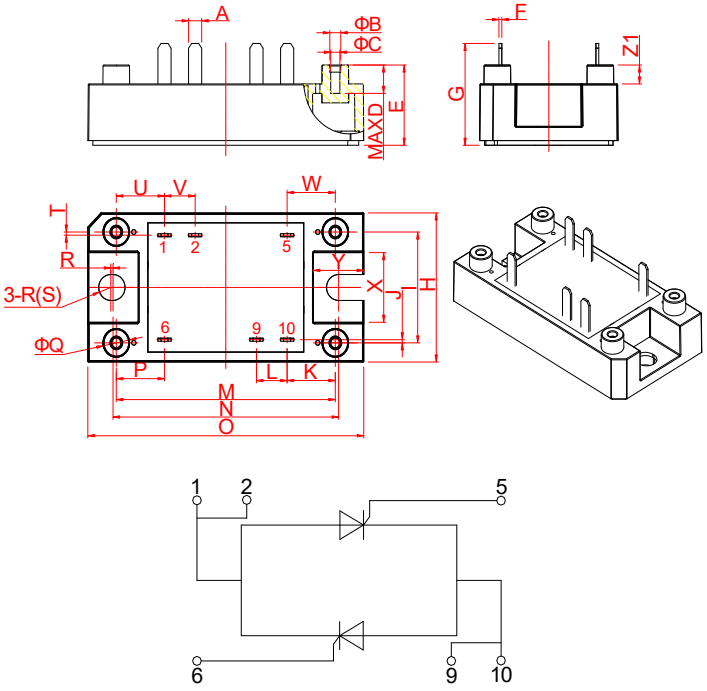
Electrical Characteristics (Packaged into V1-A-Pack, unless otherwise specified, T_{CASE}=25℃)

Parameter	Test Conditions	Symbol	Values	Unit
Peak on-state voltage	I_T=300A t_P=380μs	V_{TM}	≤1.8	V
Threshold voltage	T_j=125℃	V_{TO}	≤0.9	V
Dynamic resistance	T_j=125℃	R_d	≤2.1	mΩ
Repetitive peak off-state current	V_D=V_{RRM} T_C=25℃ T_C=125℃	 I_{DRM1} I_{DRM2}	 ≤100 ≤30	 μA mA
Repetitive peak reverse current	V_R=V_{RRM} T_C=25℃ T_C=125℃	 I_{RRM1} I_{RRM2}	 ≤100 ≤30	 μA mA
Triggering gate current	V_D=12V R_L=30Ω	I_{GT}	20-120	mA
Holding current	I_T=1A	I_H	≤250	mA
Latching current	I_G=1.2 I_{GT}	I_L	≤300	mA
Triggering gate voltage	V_D=12V R_L=30Ω	V_{GT}	≤1.8	V
Non triggering gate voltage	V_D=V_{DRM} T_j=125℃	V_{GD}	≥0.25	V
Critical rate of rise of voltage	V_D=2/3V_{DRM} T_j=125℃ Gate Open	dv/dt	≥1000	V/μs
Thermal resistance	Junction to case	$R_{th(j-c)}$	0.35	℃/W

Downloaded From Oneyac.com

Mechanical Characteristics

Module size	63x31.6mm
Module height	21.6mm
MS mounting torque to heatsink	2±15% Nm
Weight	47±2g



Symbol

Ref	Dimensions					
	Millimeters			Inches		
	Min	Typ	Max	Min	Typ	Max
A	2.85	3	3.15	0.112	0.118	0.124
B	2.3	2.5	2.7	0.091	0.098	0.106
C	1.9	2.1	2.3	0.075	0.083	0.091
D			6			0.236
E	16.25	17	17.75	0.640	0.669	0.699
F	0.55	0.65	0.75	0.022	0.026	0.030
G	20.85	21.6	22.35	0.821	0.850	0.880
H	30.85	31.6	32.35	1.215	1.244	1.274
I	23	23.5	24	0.906	0.925	0.945
J	0.17	0.67	1.17	0.007	0.026	0.046
K	10.5	11	11.5	0.413	0.433	0.453
L	6.5	7	7.5	0.256	0.276	0.295
M	49.5	50	50.5	1.949	1.989	1.988
N	51	51.5	52	2.008	2.028	2.047
O	62.25	63	63.75	2.451	2.480	2.510
P	10.5	11	11.5	0.413	0.433	0.453
Q	5.6	6.1	6.6	0.220	0.240	0.260
R	0.3	0.5	0.7	0.012	0.020	0.028
S	2.55	2.75	2.95	0.100	0.108	0.116
T	0.17	0.67	1.17	0.007	0.026	0.046
U	10.5	11	11.5	0.413	0.433	0.453
V	6.5	7	7.5	0.256	0.276	0.295
W	10.5	11	11.5	0.413	0.433	0.453
X	6.5	7	7.5	0.256	0.276	0.295
Y	10.5	11	11.5	0.413	0.433	0.453
Z1	5.6	6.1	6.6	0.220	0.240	0.260

Ordering Information

JS — JieJie Semiconductor Co., Ltd

151 — $I_{T(RMS)}$=150A

KQ — Module of anti-parallel of SCRs

-12
- 12: $V_{DSM}/V_{RSM} \geqslant 1300V$
- 16: $V_{DSM}/V_{RSM} \geqslant 1700V$
- 18: $V_{DSM}/V_{RSM} \geqslant 1900V$

Downloaded From Oneyac.com

Performance Curves

FIG.1: Forward characteristics(per thyristor)

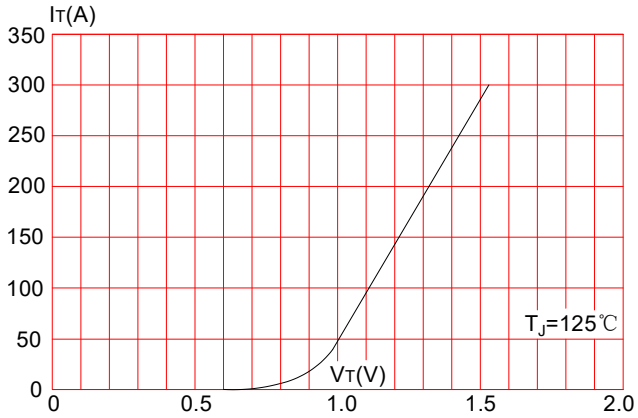


FIG.2: Surge overload current vs. time

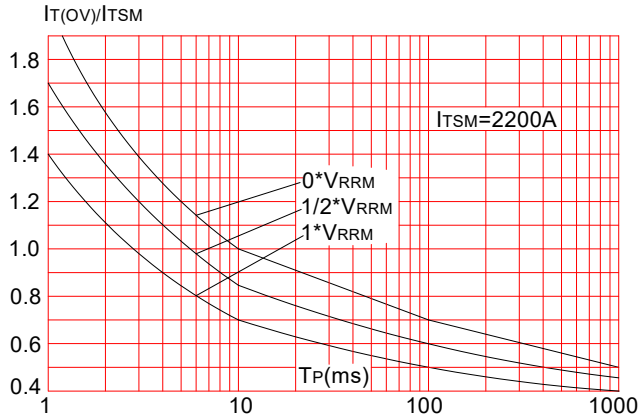


FIG.3: Power dissipation per module vs. R.M.S. current

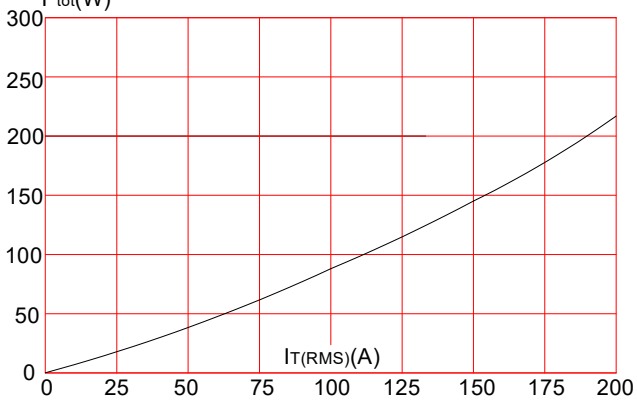
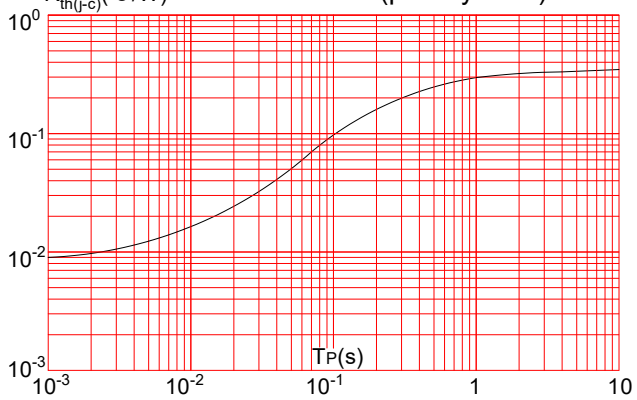


FIG.4: Maximum transient thermal impedance Junction-to-case(per thyristor)



Information furnished in this document is believed to be accurate and reliable. However, JieJie Semiconductor Co., Ltd. assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.
Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, JieJie complies with the agreement.
Products and information provided in this document have no infringement of patents. JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.
This document is the 1.3rd version which is made in 24-Feb.-2023. This document supersedes and replaces all information previously supplied.
is registered trademarks of JieJie Semiconductor Co., Ltd. Copyright©2023 Semiconductor Co., Ltd. Printed All rights reserved.

Downloaded From Oneyac.com

单击下面可查看定价，库存，交付和生命周期等信息

>>JJW(捷捷微)

Downloaded From Oneyac.com