Description

JMT Dual N-channel Enhancement Mode Power MOSFET

Features

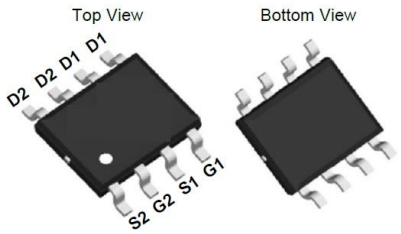
- 60V,11A
  $R_{DS(ON)}$ <14mΩ @ V_{GS} = 10V
  $R_{DS(ON)}$ <18mΩ @ V_{GS} = 4.5V
- Advanced Trench Technology
- Provide Excellent $R_{DS(ON)}$ and Low Gate Charge
- Lead free product is acquired

Application

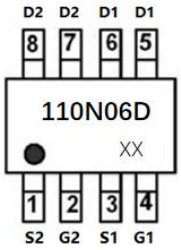
- Load Switch
- PWM Application
- Power management

100% UIS TESTED!
100% ΔVds TESTED!

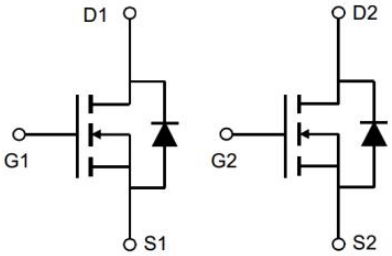
RoHS



SOP-8(Dual)



Marking and pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
110N06D	JMTP110N06D	TAPING	SOP-8	13inch	4000	48000

Absolute Maximum Ratings (T_A=25℃ unless otherwise specified)

Symbol	Parameter		Max.	Units
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Continuous Drain Current	T_A= 25℃	11	A
		T_A= 100℃	7.2	A
I_{DM}	Pulsed Drain Current note1		44	A
EAS	Single Pulsed Avalanche Energy note2		81	mJ
P_D	Power Dissipation	T_A= 25℃	3.1	W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient		40	℃/W
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	℃

Electrical Characteristics (T_J=25℃ unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V,	-	-	1.0	μA
I_{GSS}	Gate to Body Leakage Current	V_{DS}=0V, V_{GS}= ±20V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=250μA	1.0	-	2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance note3	V_{GS}=10V, I_D=11A	-	11	14	mΩ
		V_{GS}=4.5V, I_D=8A	-	13	18	
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS}=25V, V_{GS}=0V, f=1.0MHz	-	4605	-	pF
C_{oss}	Output Capacitance		-	215	-	pF
C_{rss}	Reverse Transfer Capacitance		-	191	-	pF
Q_g	Total Gate Charge	V_{DS}=30V, I_D=6A, V_{GS}=10V	-	77	-	nC
Q_{gs}	Gate-Source Charge		-	9	-	nC
Q_{gd}	Gate-Drain(“Miller”) Charge		-	23	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-on Delay Time	V_{DS}=30V, I_D=11A, R_G=1.8Ω, V_{GS}=10V	-	7.1	-	ns
t_r	Turn-on Rise Time		-	5.3	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	27.2	-	ns
t_f	Turn-off Fall Time		-	6.2	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	11	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	44	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS}=0V, I_S=11A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	I_F=11A, dI/dt=100A/μs	-	29	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	45	-	nC

Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. EAS condition : T_J=25℃, V_{DD}=30V, V_G=10V, L=0.5mH, Rg=25Ω, I_{AS}=18A

3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

Typical Performance Characteristics

Figure1: Output Characteristics

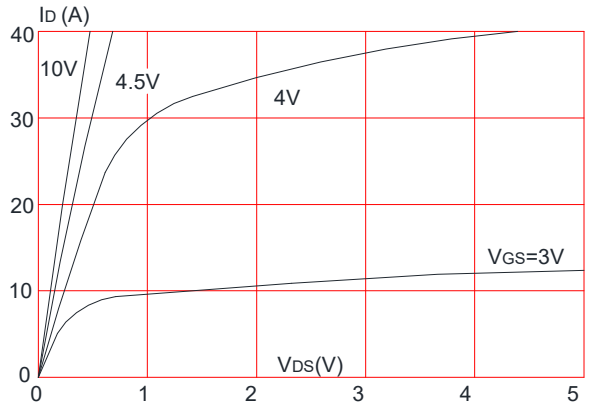


Figure 2: Typical Transfer Characteristics

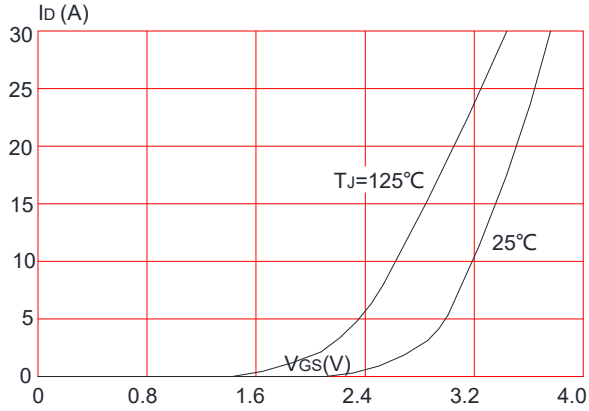


Figure 3: On-resistance vs. Drain Current

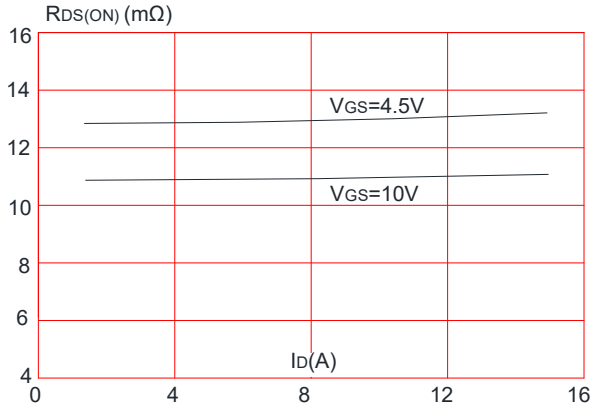


Figure 4: Body Diode Characteristics

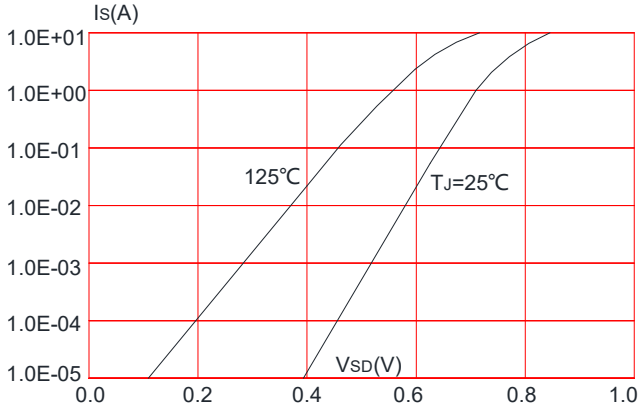


Figure 5: Gate Charge Characteristics

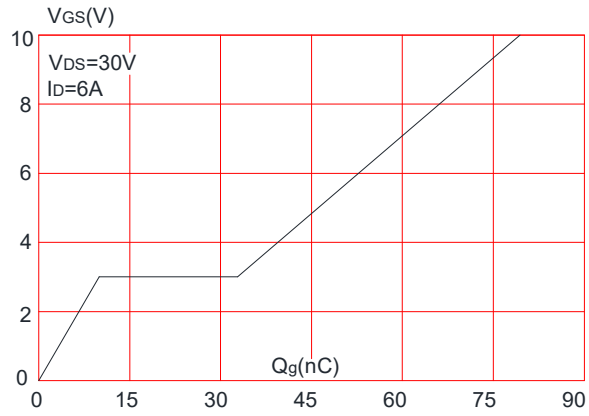


Figure 6: Capacitance Characteristics

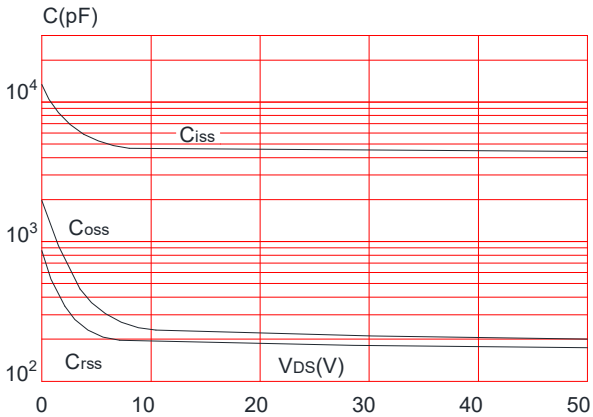


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

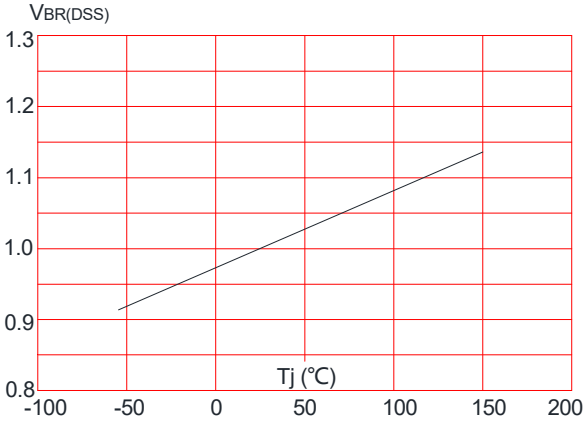


Figure 8: Normalized on Resistance vs. Junction Temperature

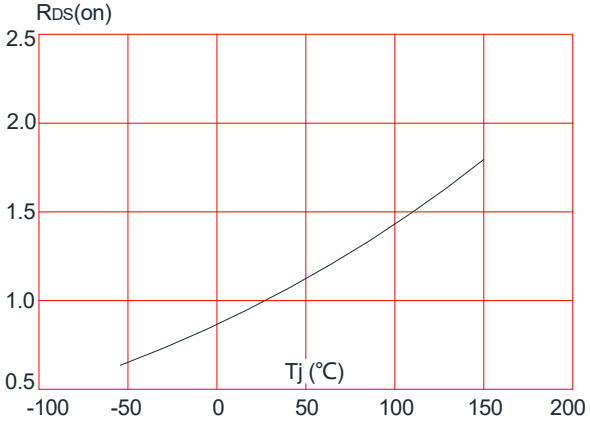


Figure 9: Maximum Safe Operating Area

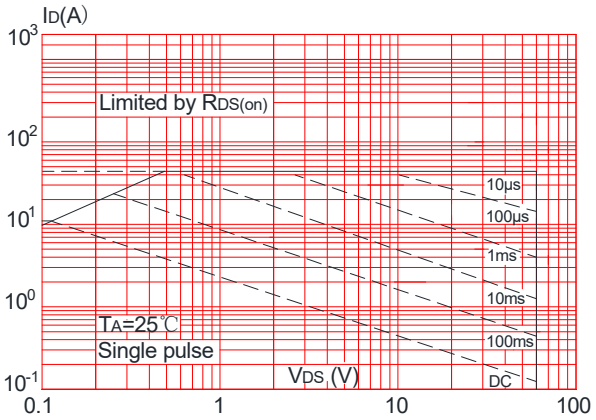


Figure 10: Maximum Continuous Drain Current vs. Ambient Temperature

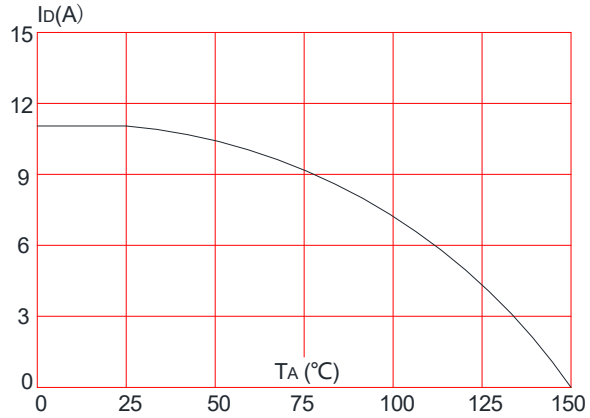
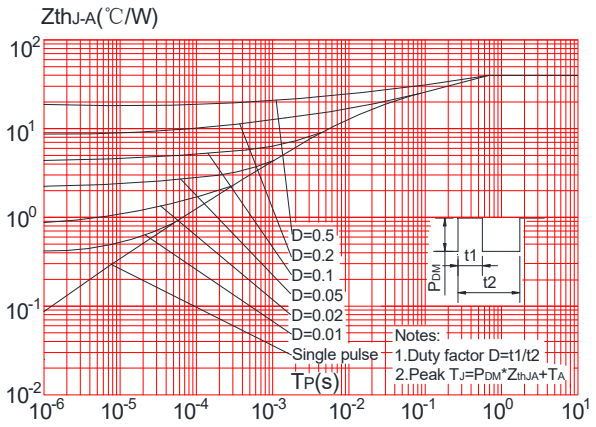


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



Test Circuit

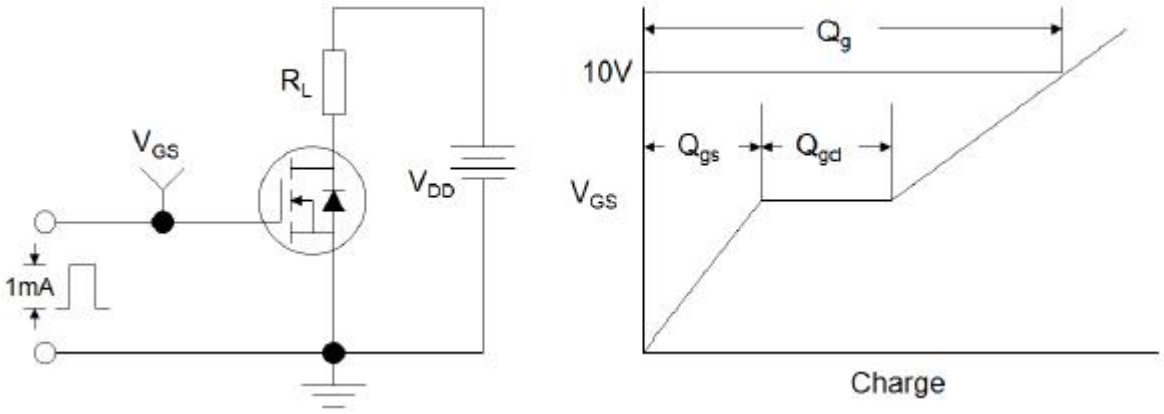


Figure1:Gate Charge Test Circuit & Waveform

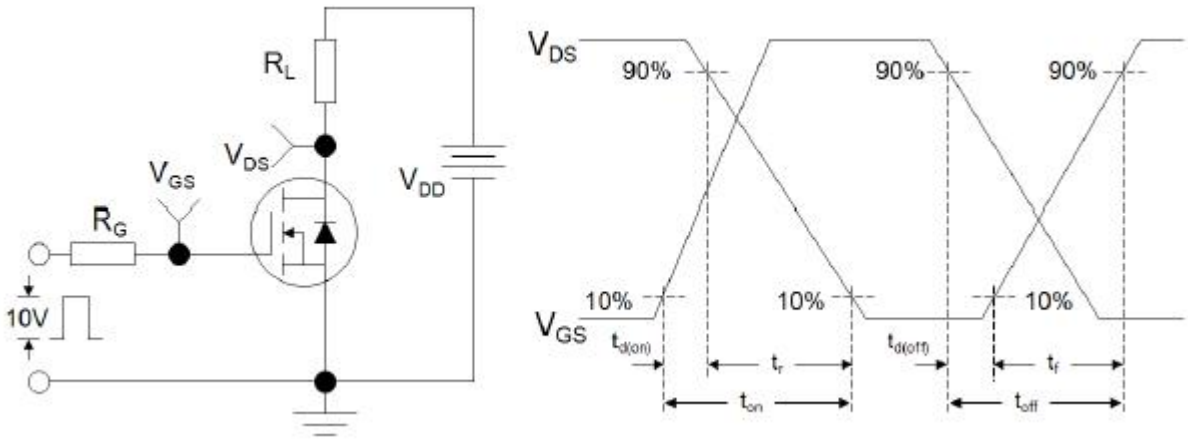


Figure 2: Resistive Switching Test Circuit & Waveforms

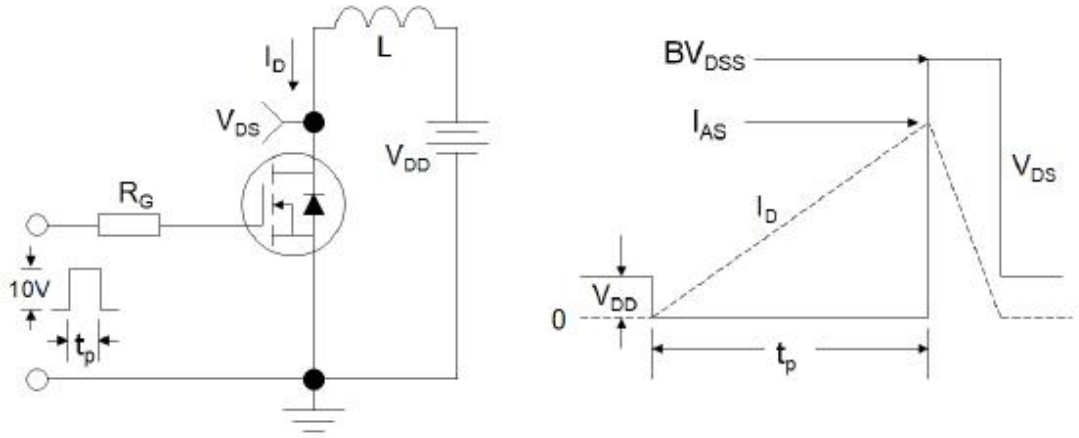


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

Package Mechanical Data- SOP-8