



# JMPK2N60G1

## Description

### JMP N-channel Enhancement Mode Power MOSFET

#### Features

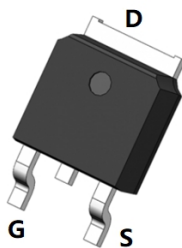
- 600V, 2A  
 $R_{DS(ON)} < 4.7\Omega @ V_{GS} = 10V$
- Fast Switching
- Improved dv/dt Capability

#### Application

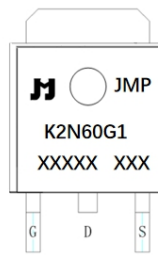
- Load Switch
- PWM Application
- Power management



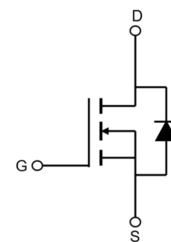
100% UIS TESTED!  
100%  $\Delta V_{ds}$  TESTED!



TO-252-4R (DPAK) top view



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
JMPK2N60G1	JMPK2N60G1	TAPING	TO-252-4R	13inch	2500	25000

## Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	600	V
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ\text{C}$	2
		$T_C = 100^\circ\text{C}$	1.3
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	8	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>	39.2	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	54
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.3	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	$^\circ\text{C/W}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

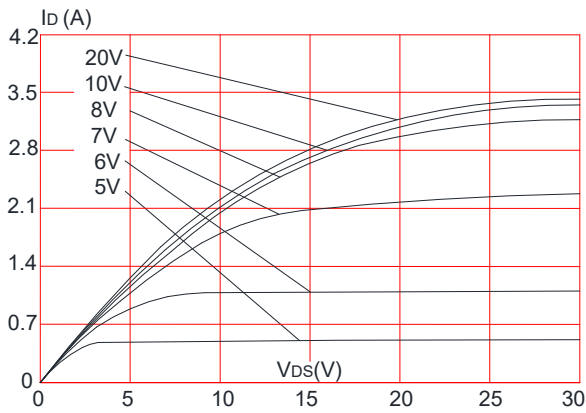
Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	600	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V, T <sub>J</sub> =25°C	-	-	1	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> = ±30V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	2	-	4	V
R <sub>DS(on)</sub> <small>note3</small>	Static Drain-Source on-Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =1A	-	3.9	4.7	Ω
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1.0MHz	-	293	-	pF
C <sub>oss</sub>	Output Capacitance		-	35	-	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	7	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DD</sub> =480V, I <sub>D</sub> =2A, V <sub>GS</sub> =10V	-	10	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	1.5	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	5	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> =300V, I <sub>D</sub> =2A, R <sub>G</sub> =25Ω	-	33.6	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	7.2	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	64	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	31.2	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	2	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	8	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>SD</sub> =2A	-	-	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> =0V, I <sub>S</sub> =2A, di/dt=100A/μs	-	180	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	0.6	-	μC

- Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature  
2. EAS condition: T<sub>J</sub> = 25°C, V<sub>DD</sub> =120V, V<sub>G</sub> = 10V, L= 10mH, I<sub>AS</sub> = 2.8A  
3. Pulse Test: Pulse Width≤300μs, Duty Cycle≤1%

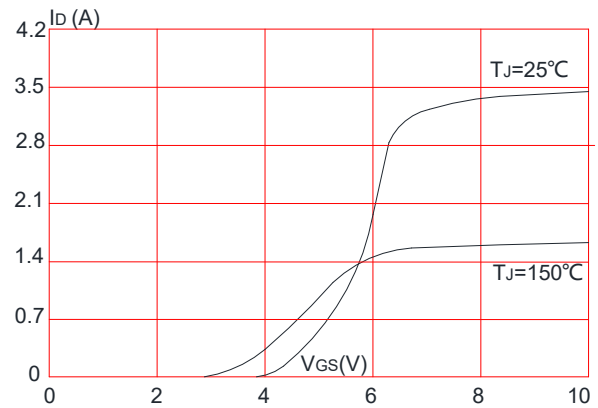


## Typical Performance Characteristics

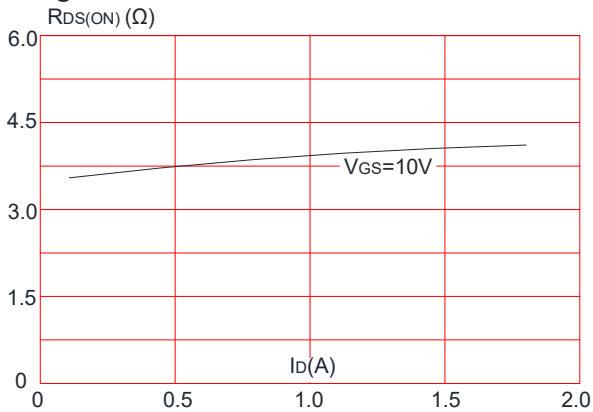
**Figure 1: Output Characteristics**



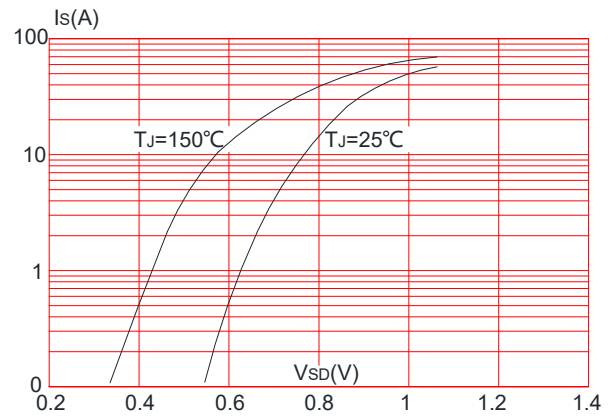
**Figure 2: Typical Transfer Characteristics**



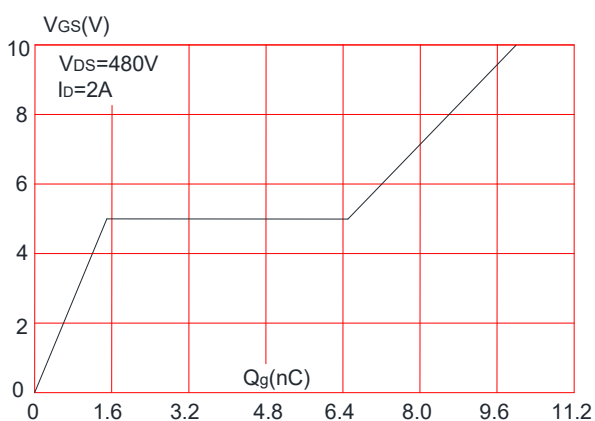
**Figure 3: On-resistance vs. Drain Current**



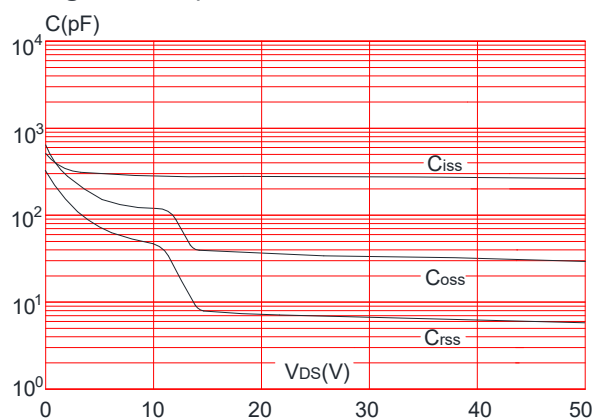
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**

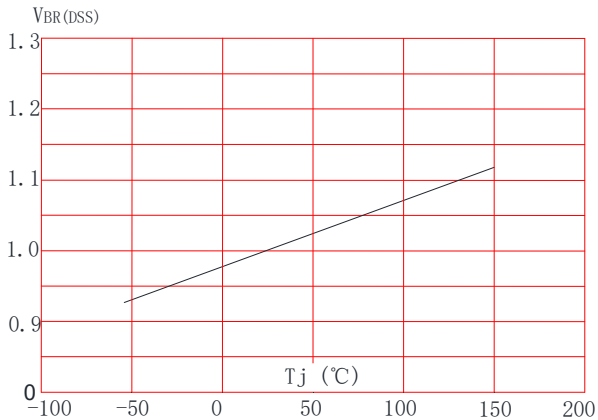


**Figure 6: Capacitance Characteristics**

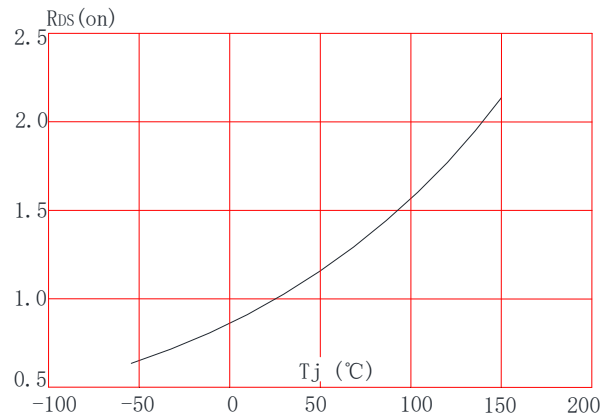




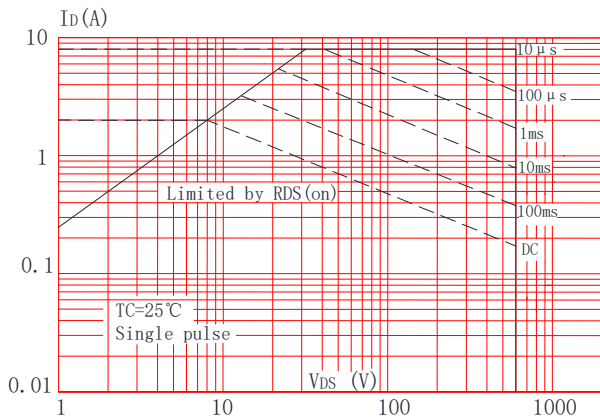
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



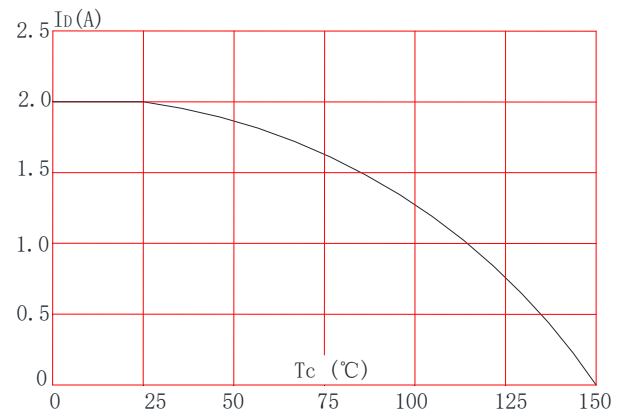
**Figure 8:** Normalized on Resistance vs. Junction Temperature



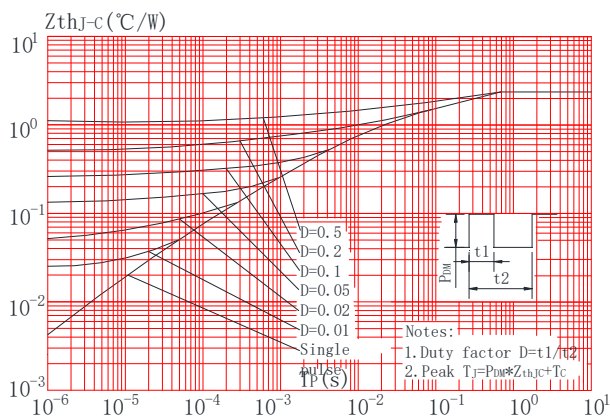
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Case Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Case



## Test Circuit

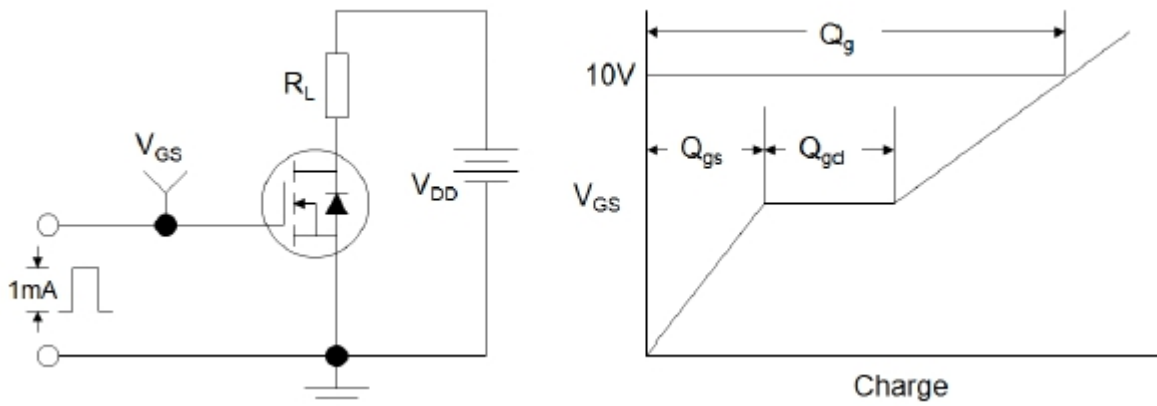


Figure1:Gate Charge Test Circuit & Waveform

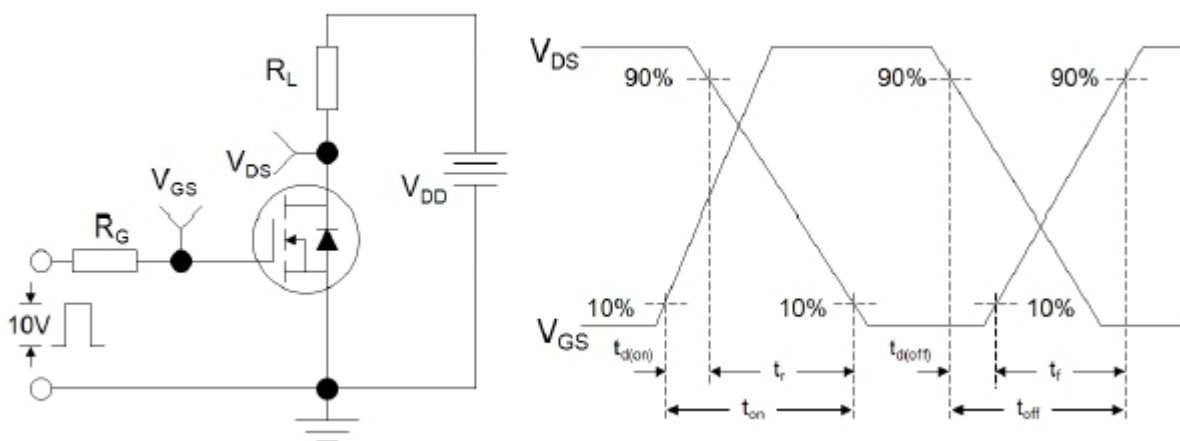


Figure 2: Resistive Switching Test Circuit & Waveforms

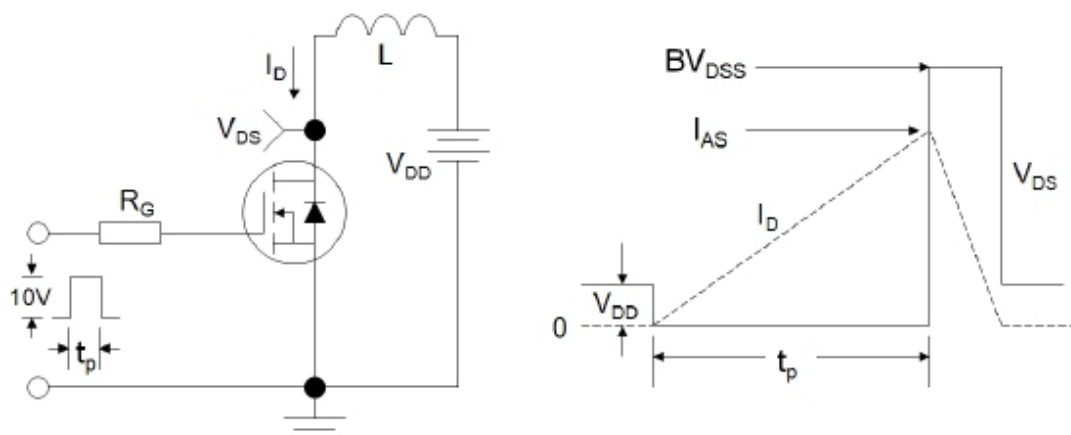
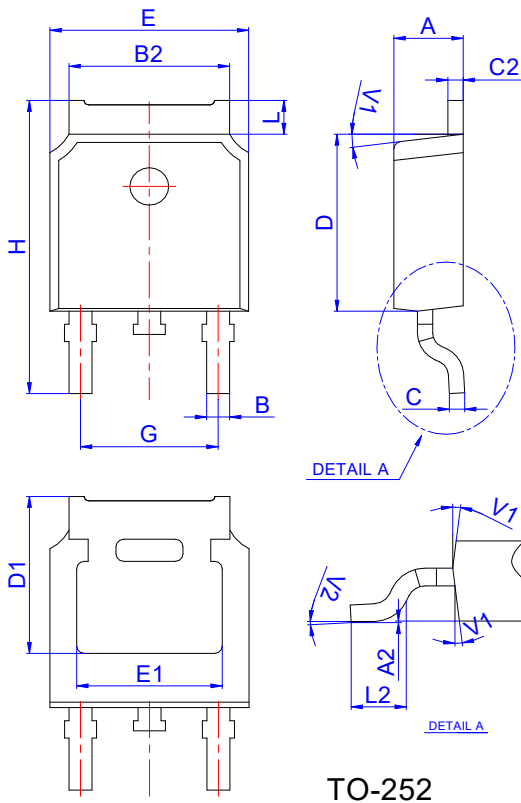


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms

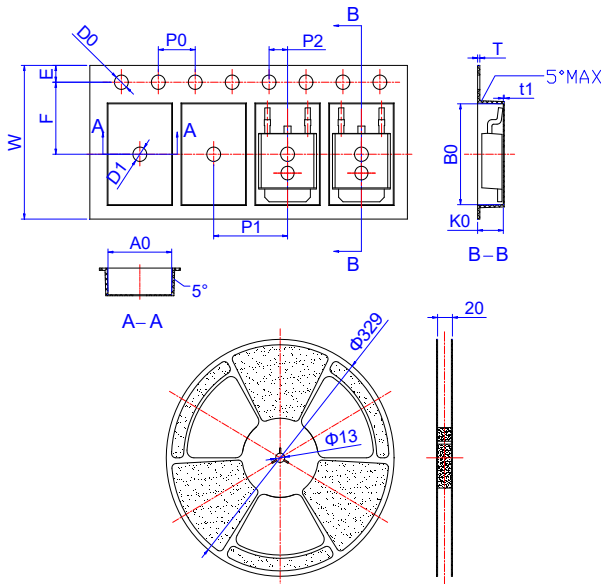


## Package Mechanical Data-TO-252-4R



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

## Reel Specification-TO-252-4R




Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583



Information furnished in this document is believed to be accurate and reliable. However, Jiangsu JieJie Microelectronics Co.,Ltd assumes no responsibility for the consequences of use without consideration for such information nor use beyond it.

Information mentioned in this document is subject to change without notice, apart from that when an agreement is signed, Jiangsu JieJie complies with the agreement.

Products and information provided in this document have no infringement of patents. Jiangsu JieJie assumes no responsibility for any infringement of other rights of third parties which may result from the use of such products and information.

 is a registered trademark of Jiangsu JieJie Microelectronics Co.,Ltd.  
Copyright ©2021 Jiangsu JieJie Microelectronics Co.,Ltd. Printed All rights reserved.

单击下面可查看定价，库存，交付和生命周期等信息

[>>JW\(捷捷微\)](#)