



## Description

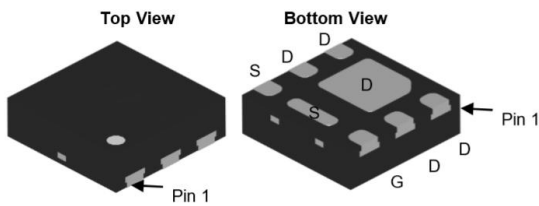
### JMT N-channel Enhancement Mode Power MOSFET

#### Features

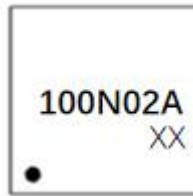
- 20V, 10A  
 $R_{DS(ON)} < 13m\Omega @ V_{GS} = 4.5V$   
 $R_{DS(ON)} < 21m\Omega @ V_{GS} = 2.5V$
- Advanced Trench Technology
- Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead free product is acquired

#### Application

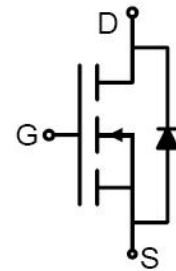
- Load Switch
- PWM Application
- Power management



DFN2X2-6L



Marking and pin Assignment



Schematic Diagram

## Package Marking and Ordering Information

Device Marking	Device	OUTLINE	Device Package	Reel Size	Reel (PCS)	Per Carton (PCS)
100N02A	JMTV100N02A	TAPING	DFN2X2-6L	7inch	3000	180000

## Absolute Maximum Ratings ( $T_A=25^\circ C$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current	$T_A = 25^\circ C$	10
		$T_A = 100^\circ C$	6.5
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	40	A
$P_D$	Power Dissipation	$T_A = 25^\circ C$	2.2
$R_{\theta JA}$	Thermal Resistance, Junction to Case	57	$^\circ C/W$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ C$



## Electrical Characteristics (T<sub>J</sub>=25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	20	-	-	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =20V, V <sub>GS</sub> =0V,	-	-	1.0	μA
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>DS</sub> =0V, V <sub>GS</sub> =±12V	-	-	±100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.5	0.8	1.1	V
R <sub>DS(on)</sub>	Static Drain-Source on-Resistance <small>note2</small>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A	-	10	13	mΩ
		V <sub>GS</sub> =2.5V, I <sub>D</sub> =5A	-	15	21	
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1.0MHz	-	946	-	pF
C <sub>oss</sub>	Output Capacitance		-	204	-	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		-	178	-	pF
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =10V, I <sub>D</sub> =4A, V <sub>GS</sub> =4.5V	-	15	-	nC
Q <sub>gs</sub>	Gate-Source Charge		-	2	-	nC
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		-	5.2	-	nC
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DS</sub> =10V, I <sub>D</sub> =4A, R <sub>GEN</sub> =3Ω, V <sub>GS</sub> =4.5V	-	9	-	ns
t <sub>r</sub>	Turn-on Rise Time		-	25	-	ns
t <sub>d(off)</sub>	Turn-off Delay Time		-	37	-	ns
t <sub>f</sub>	Turn-off Fall Time		-	14	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	10	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	40	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =10A	-	-	1.2	V

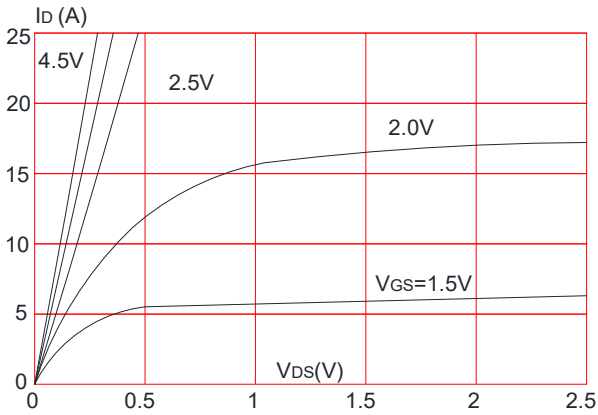
Notes:1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature

2. Pulse Test: Pulse Width≤300μs, Duty Cycle≤0.5%

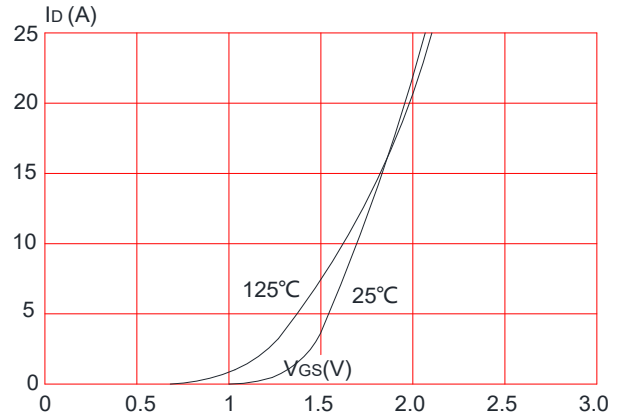


## Typical Performance Characteristics

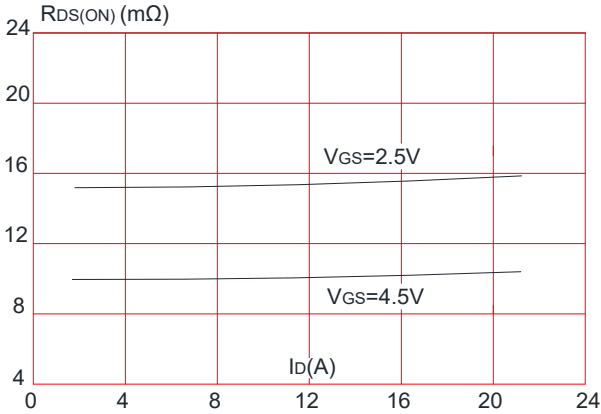
**Figure 1: Output Characteristics**



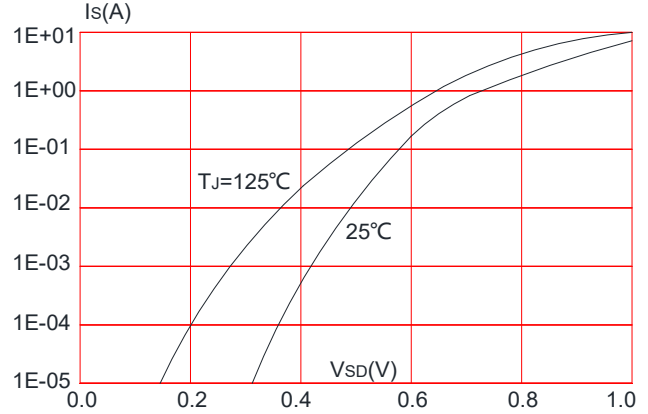
**Figure 2: Typical Transfer Characteristics**



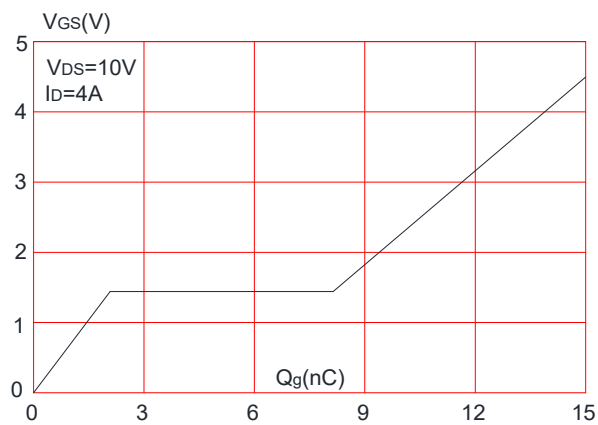
**Figure 3: On-resistance vs. Drain Current**



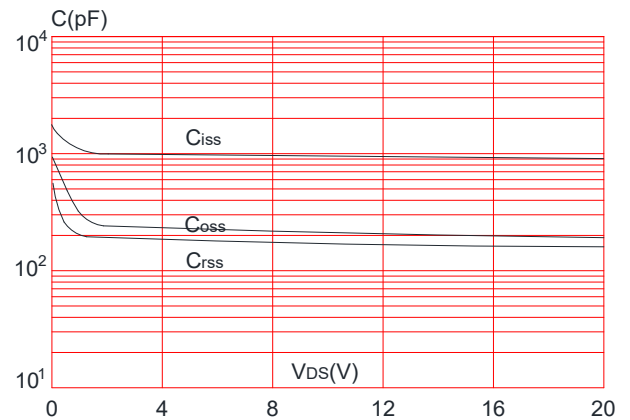
**Figure 4: Body Diode Characteristics**



**Figure 5: Gate Charge Characteristics**



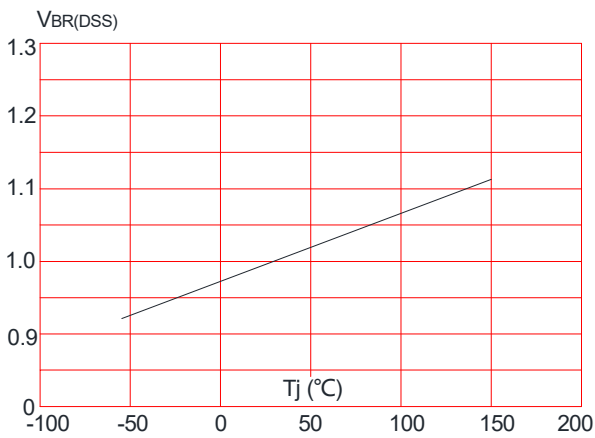
**Figure 6: Capacitance Characteristics**



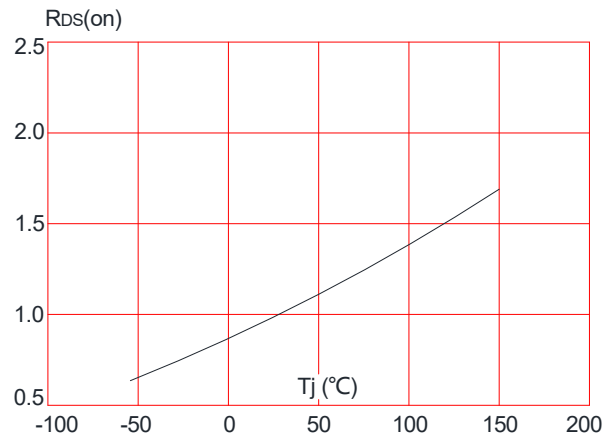


# JMTV100N02A

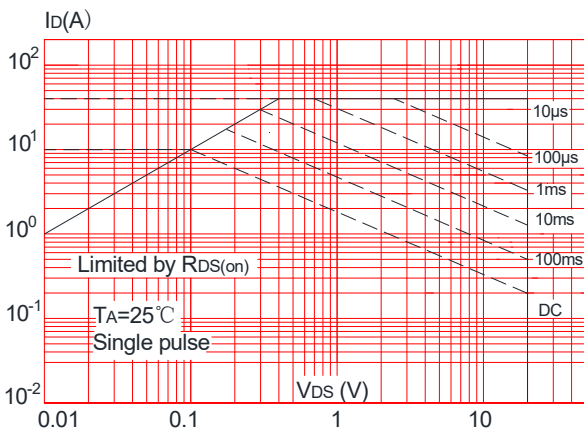
**Figure 7:** Normalized Breakdown Voltage vs. Junction Temperature



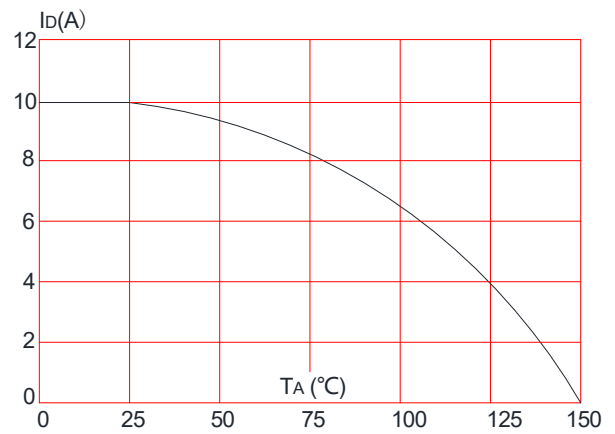
**Figure 8:** Normalized on Resistance vs. Junction Temperature



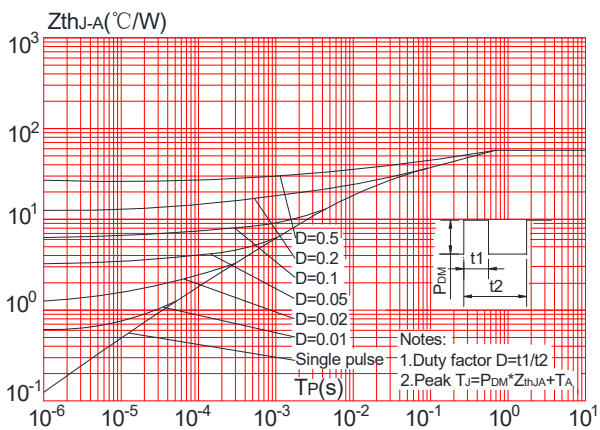
**Figure 9:** Maximum Safe Operating Area



**Figure 10:** Maximum Continuous Drain Current vs. Ambient Temperature



**Figure.11:** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



## Test Circuit

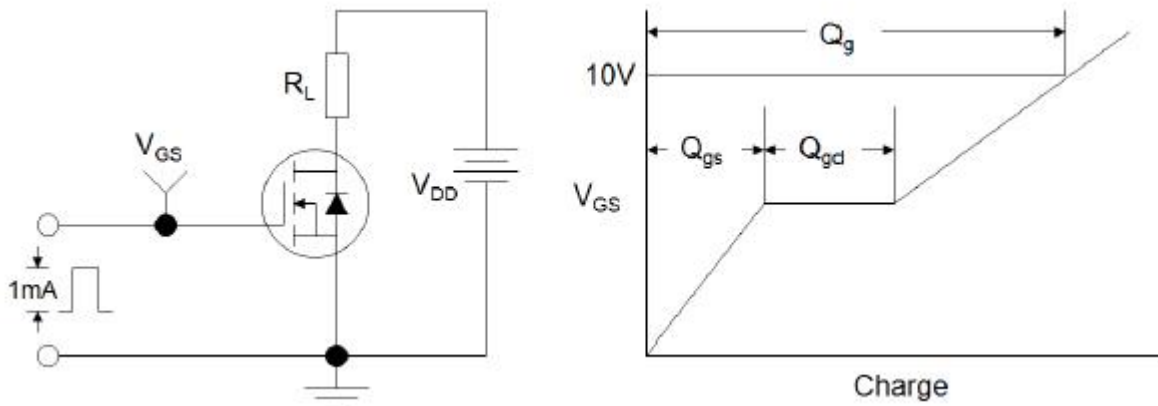


Figure1:Gate Charge Test Circuit & Waveform

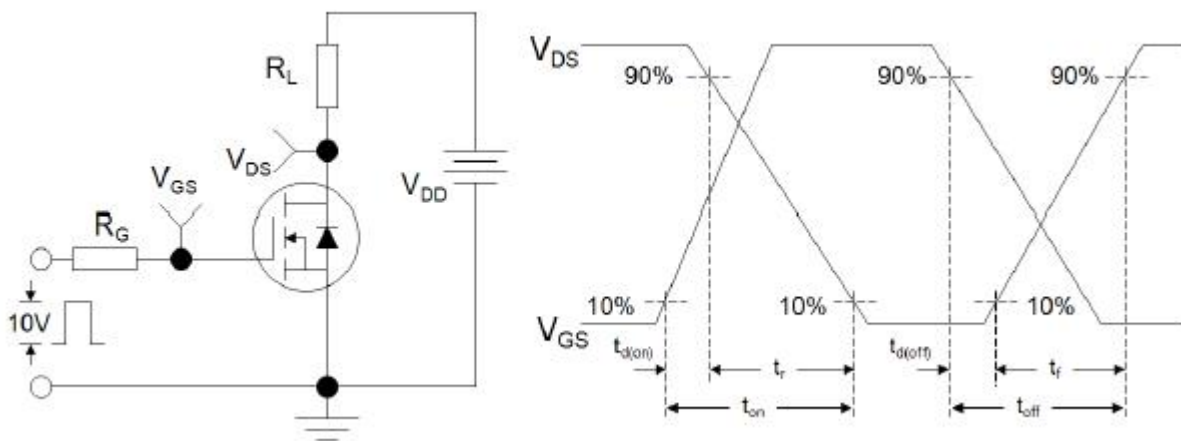


Figure 2: Resistive Switching Test Circuit & Waveforms

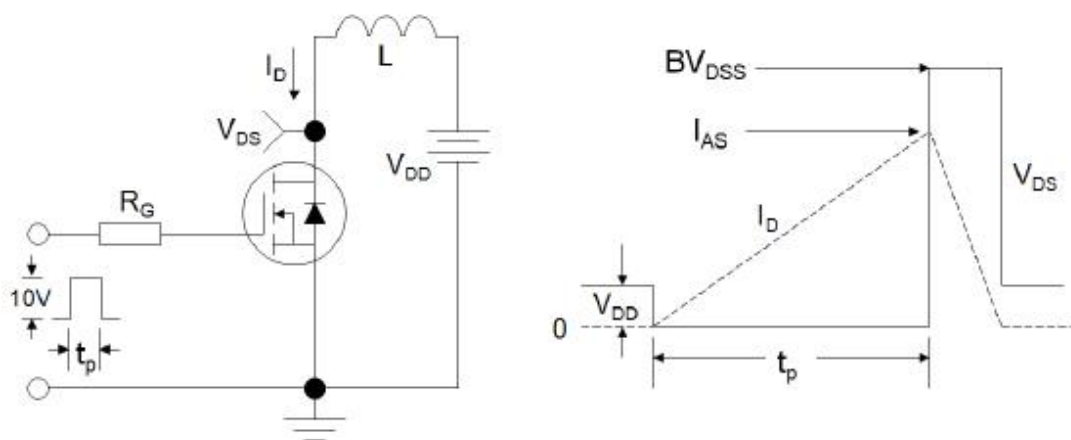
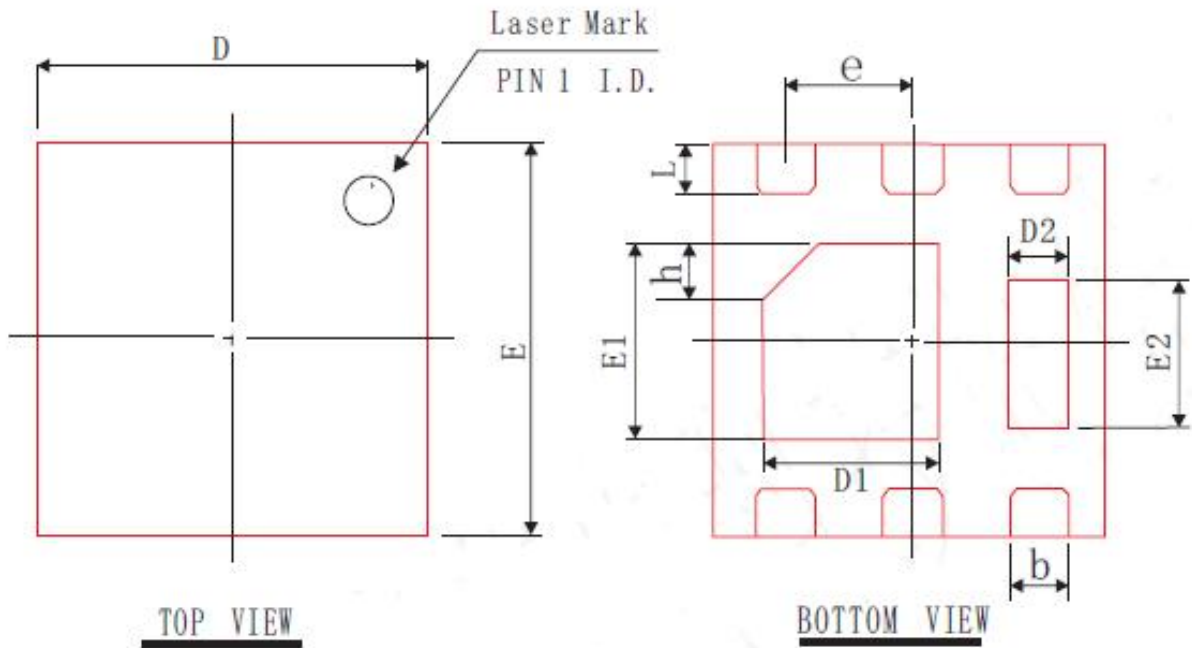


Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms



## Package Mechanical Data-DFN2X2-6L



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
D	1.95	2.00	2.07
E	1.95	2.00	2.07
D1	0.80	0.90	1.00
E1	0.90	1.00	1.10
D2	0.20	0.30	0.40
E2	0.65	0.75	0.85
L	0.20	0.25	0.35
h	0.20	0.25	0.30
c	0.203 REF		
e	0.65 BSC		




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