JOR⚫JIN a module solution provider
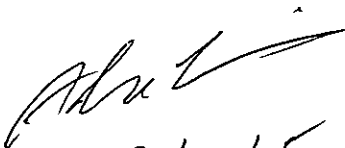
WG7831-D0 WLAN/BT

Module

**TI WiLink8 IEEE 802.11b/g/n
BT/BLE Solution**

Datasheet

Revision 0.6

Prepared By	Reviewed By	Approved By
Hsin Wei Wang 2018.11.01	Victor Lee 2018/11/65	*(signature)* 2018/11/05

a module solution provider

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1. OVERVIEW

WG7831-D0, a WiFi, BT, BLE SiP (system in package) module, is the most demanded design for mobile devices, audio, computer, PDA and embedded system applications with Wilink8 solution from TI.

1.1. Models Functional Blocks

Model	WLAN 2.4GHz	WLAN 5GHz	BT/BLE
WG7831-D0	V	-	V

1.2. General Features

- WLAN, Bluetooth, BLE with Integrated RF Front-End Module (FEM), Power Amplifier (PA), and Power Management on a Single Module.
- LGA106 pin package.
- Dimension 12.8mm(L) x 12.0mm(W) x 1.63mm(H)
- Provides efficient direct connection to battery by employing several integrated switched mode power supplies (DC2DC).
- Seamless Integration with TI Sitara™ and Other Application Processors
- WLAN and BT/BLE cores are software and hardware compatible with prior WL127x and WL128x offerings, for smooth migration to device.
- Shared HCI transport for BT/BLE over UART and SDIO for WLAN.
- Temperature detection and compensation mechanism ensures minimal variation in RF performance over the entire temperature range.
- BT, BLE and all audio processing features work in parallel and include full coexistence with WLAN
- Operating temperature: –20°C to 75°C

2. FUNCTIONAL FEATURES

2.1. Module Block Diagram
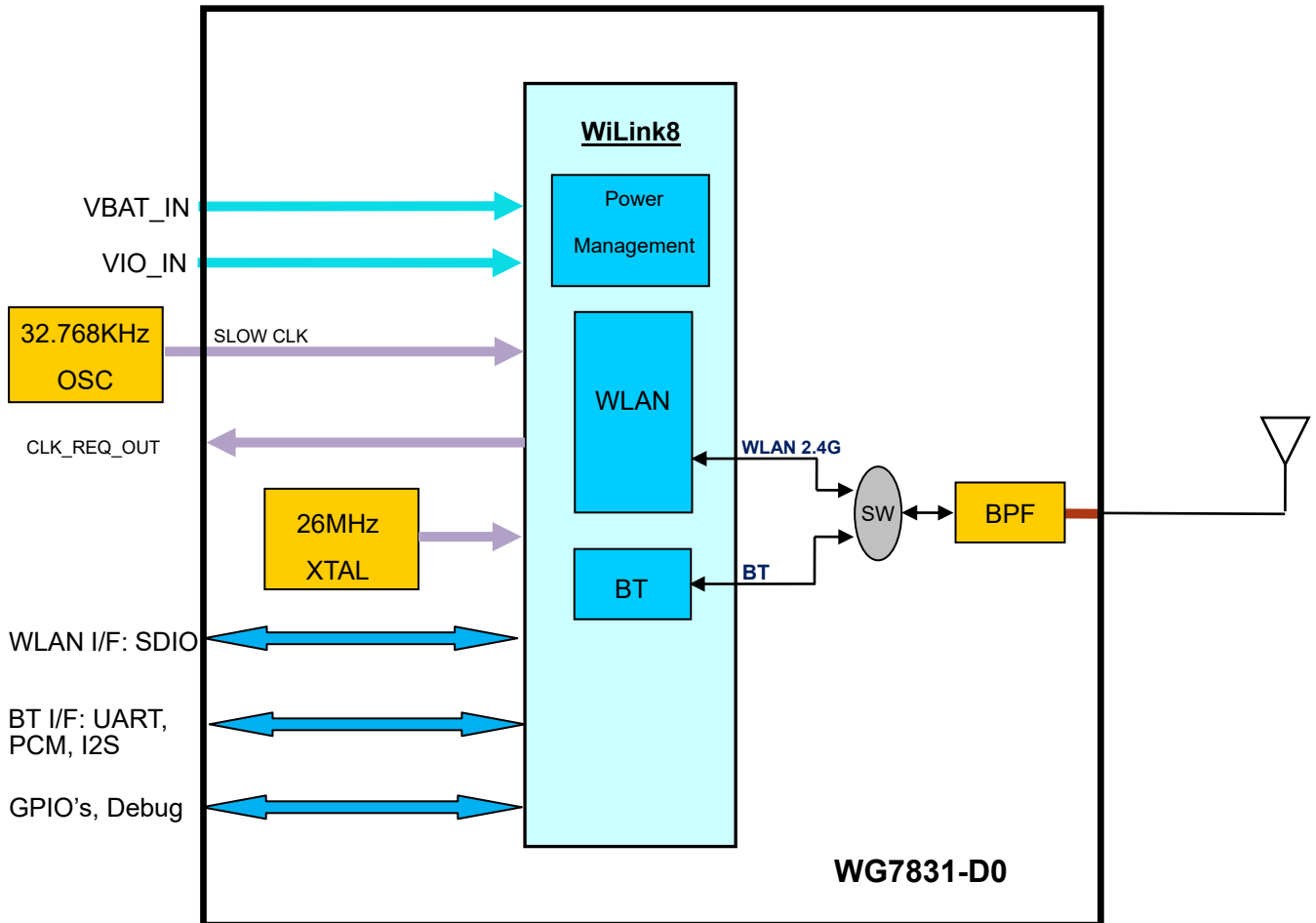
Figure 2-1. WG7831-D0 Block Diagram

2.2. Block Functional Feature

2.2.1 WLAN Features

- Integrated 2.4 GHz Power Amplifier (PA) for WLAN solution
- WLAN Baseband Processor and RF transceiver supporting IEEE 802.11b/g/n.
- WLAN 2.4GHz SISO (20/40 MHz channels)
- Baseband Processor
  - IEEE Std 802.11b/g/n data rates and IEEE Std 802.11n data rates with 20 or 40 MHz SISO.
- Fully calibrated system. Production calibration not required.
- Medium Access Controller (MAC)
  - Embedded ARM™ Central Processing Unit (CPU)
  - Hardware-Based Encryption/Decryption using 64-, 128-, and 256-Bit WEP, TKIP or AES Keys,
  - Supports requirements for Wi-Fi Protected Access (WPA and WPA2.0) and IEEE Std 802.11i [includes hardware-accelerated Advanced Encryption Standard (AES)]
  - Designed to work with IEEE Std 802.1x
- IEEE Std 802.11d,e,h,i,k,r PICS compliant.
- New advanced co-existence scheme with BT/BLE.
- Supports 4 bit SDIO host interface, including high speed (HS) and V3 modes.

2.2.2 Bluetooth and BLE Features

- Supports Bluetooth Core Specification Version 4.2.
- Includes concurrent operation and built -in coexisting and prioritization handling of Bluetooth, BLE, audio processing and WLAN
- Dedicated Audio processor supporting on chip SBC encoding + A2DP:
  - ➢ Assisted A2DP (A3DP) support - SBC encoding implemented internally
  - ➢ Assisted WB-Speech (AWBS) support - modified SBC codec implemented internally
- Fully compliant with BT and BLE dual mode standard
- Support for all roles and role-combinations, mandatory as well as optional
- Supports up to 10 BLE connections
- Independent buffering for LE allows having large number of multiple connections without affecting BR/EDR performance

3. MODULE OUTLINE

3.1. Signal Layout (Top View)
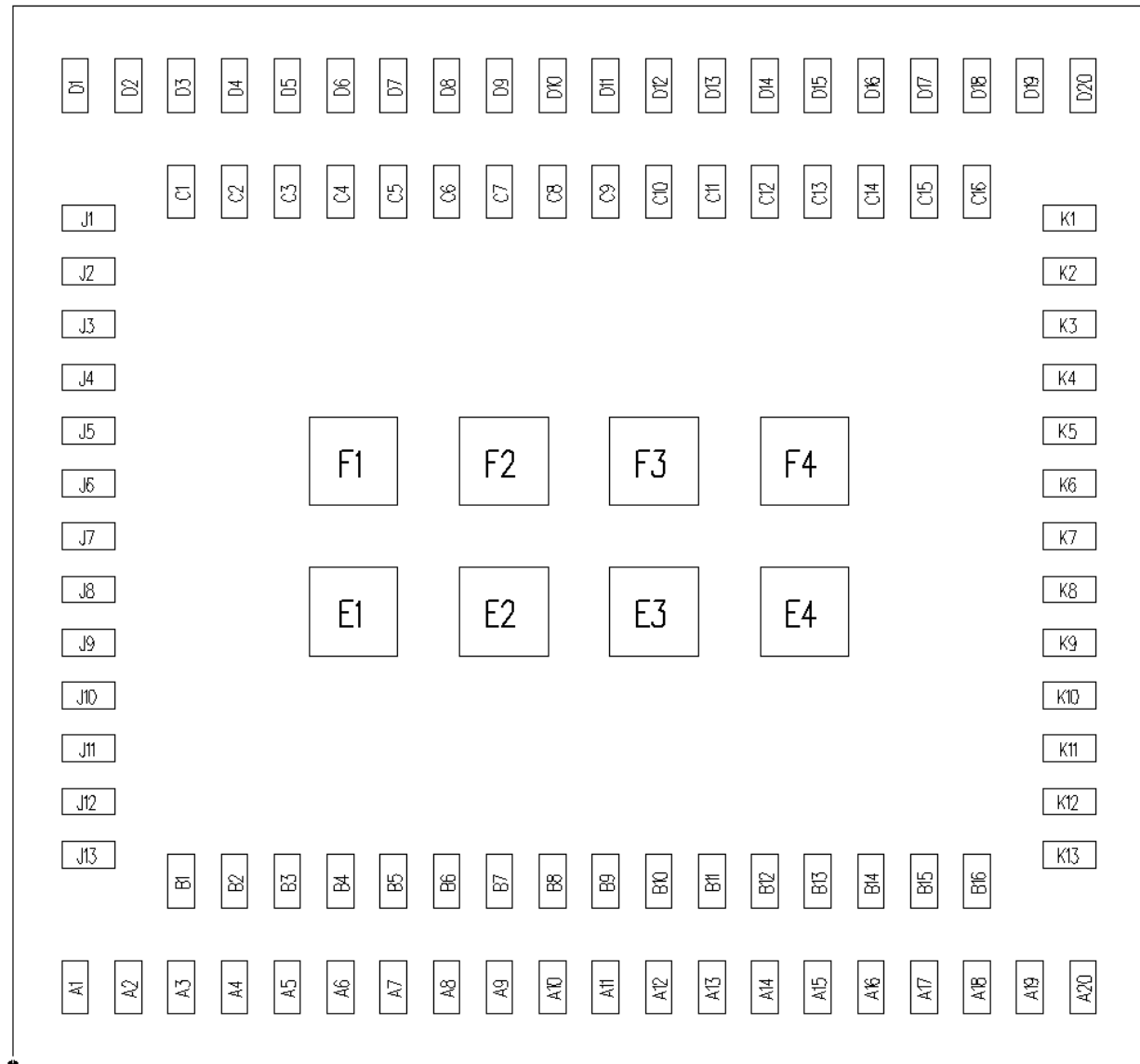
Figure 3-1 Device pins

3.2. Pin Description

Table 3-1. Pin Description

Pin No.	Signal Name	Type	Shut Down state	After Power Up[1]	Voltage Level	Description
A1	GND	GND				Ground
A2	WLAN_SDIO_D3	I/O	HiZ	PU	1.8V	WLAN SDIO Data bit 3. Changes state to PU at WL_EN or BT_EN assertion for card detects. Later disabled by software during initialization. [2]
A3	WLAN_SDIO_CMD	I/O	HiZ	HiZ	1.8V	WLAN SDIO Command [2]
A4	WLAN_SDIO_D2	I/O	HiZ	HiZ	1.8V	WLAN SDIO Data bit 2 [2]
A5	WLAN_SDIO_D0	I/O	HiZ	HiZ	1.8V	WLAN SDIO Data bit 0[2]
A6	WLAN_SDIO_D1	I/O	HiZ	HiZ	1.8V	WLAN SDIO Data bit 1 [2]
A7	WLAN_SDIO_CLK	IN	HiZ	HiZ	1.8V	WLAN SDIO Clock. Must be driven by the host.
A8	GND	GND				Ground
A9	BT_HCI_CTS	IN	PU	PU	1.8V	UART CTS from host. NC if not used.
A10	BT_HCI_RTS	OUT	PU	PU	1.8V	UART RTS to host. NC if not used.
A11	BT_HCI_TX	OUT	PU	PU	1.8V	UART TX to host. NC if not used.
A12	BT_HCI_RX	IN	PU	PU	1.8V	UART RX from host. NC if not used.
A13	NC					NC
A14	NC					NC
A15	NC					NC
A16	GND	GND				Ground
A17	NC					NC
A18	GND	GND				Ground
A19	VIO_IN	POW	PD	PD	1.8V	Connect to 1.8V external VIO
A20	GND	GND				Ground

B1	NC					NC
B2	NC					NC
B3	GPIO11	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B4	GPIO9	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B5	GPIO10	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B6	GPIO12	I/O	PU	PU	1.8V	Reserved for future use. NC if not used.
B7	NC					NC
B8	NC					NC
B9	NC					NC
B10	NC					NC
B11	NC					NC
B12	NC					NC
B13	NC					NC
B14	NC					NC
B15	NC					NC
B16	NC					NC
C1	GND	GND				Ground
C2	NC					NC
C3	NC					NC
C4	BT_UART_DEBUG	OUT	PU	PU	1.8V	Option: Bluetooth logger
C5	NC					NC
C6	WLAN_UART_DBG	OUT	PU	PU	1.8V	Option: WLAN logger
C7	GPIO1	I/O	PD	PD	1.8V	WL_RS232_TX (when IRQ_WL = 1 at power up)
C8	NC					NC
C9	NC					NC
C10	WLAN_EN	IN	PD	PD	1.8V	Mode setting: High = enable
C11	WLAN_IRQ	OUT	PD	0	1.8V	SDIO available, interrupt out. Active high. To use WL_RS232_TX and RX lines, need to pull up with 10K resistor.
C12	GND	GND				Ground
C13	GND	GND				Ground
C14	GND	GND				Ground

C15	GND	GND				Ground
C16	GND	GND				Ground
D1	GND	GND				Ground
D2	VBAT	POW			VBAT	Power supply input, 2.9 to 4.8 V
D3	NC					NC
D4	NC					NC
D5	NC					NC
D6	GND	GND				Ground
D7	NC					NC
D8	GND	GND				Ground
D9	PA_DC2DC_OUT	POW				Internal DC2DC output
D10	GPIO4	I/O	PD	PD	1.8V	Reserved for future use. NC if not used.
D11	GPIO2	I/O	PD	PD	1.8V	WL_RS232_RX (when IRQ_WL = 1 at power up)
D12	BT_EN	In	PD	PD	1.8V	Mode setting: High = enable
D13	NC					NC
D14	NC					NC
D15	GND	GND				Ground
D16	GND	GND				Ground
D17	GND	GND				Ground
D18	GND	GND				Ground
D19	NC					NC
D20	GND	GND				Ground
E1	GND	GND				Ground
E2	GND	GND				Ground
E3	GND	GND				Ground
E4	GND	GND				Ground
F1	GND	GND				Ground
F2	GND	GND				Ground
F3	GND	GND				Ground
F4	GND	GND				Ground
J1	GND	GND				Ground
J2	GND	GND				Ground
J3	GND	GND				Ground

J4	NC					NC
J5	NC					NC
J6	NC					NC
J7	NC					NC
J8	NC					NC
J9	NC					NC
J10	CLK_REQ_OUT	OUT	PD	PD	1.8V	Clock request out, Not used. Leave NC.
J11	GND	GND				Ground
J12	GND	GND				Ground
J13	NC					NC
K1	GND	GND				Ground
K2	RF_ANT_BG	RF				WLAN/BT 2.4G RF Port
K3	GND	GND				Ground
K4	GND	GND				Ground
K5	GND	GND				Ground
K6	GND	GND				Ground
K7	BT_AUD_OUT	OUT	PD	PD	1.8V	Bluetooth PCM/I2S Bus. Data out. NC if not used.
K8	GND	GND				Ground
K9	SLOW_CLK	ANA				Input Sleep clock: 32.768 KHz
K10	GND	GND				Ground
K11	BT_AUD_IN	IN	PD	PD	1.8V	Bluetooth PCM/I2S Bus. Data in. NC if not used.
K12	BT_AUD_CLK	OUT	PD	PD	1.8V	Bluetooth PCM/I2S Bus. Clock. NC if not used.
K13	BT_AUD_FSYNC	OUT	PD	PD	1.8V	Bluetooth PCM/I2S Bus. Frame sync. NC if not used.

(1) PU=pull up; PD=pull down.

(2) Host must provide PU for all non-CLK SDIO signals

4. MODULE SPECIFICATION

4.1. General Module Requirements and Operation

4.1.1 Absolute Maximum Ratings [1]

Parameter		Value	Units
VBAT		4.8 [2]	V
VIO		-0.5 to 2.1	V
Input voltage to Analog pins		-0.5 to 2.1	V
Input voltage to all other pins		-0.5 to (VIO + 0.5V)	V
Operating ambient temperature range		-20 to +75	°C
Storage temperature range		-55 to +125	°C
ESD Stress Voltage [3]	Human Body Model [4]	>1000	V
	Charged Device Model [5]	>250	V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) 4.8 V cumulative to 2.33 years, including charging dips and peaks

(3) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into device.

(4) Level listed is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Pins listed as 1000V may actually have higher performance.

(5) Level listed is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 250V CDM is possible if necessary precautions are taken. Pins listed as 250V may actually have higher performance.

4.1.2 Recommended Operating Conditions

Parameter	Condition	Sym	Min	Max	Units
VBAT [1]	DC supply range for all modes		2.9	4.8	V
1.8 V IO ring power supply voltage			1.62	1.95	
IO high-level input voltage		VIH	0.65 x VIO	VIO	
IO low-level input voltage		VIL	0	0.35 x VIO	
Enable inputs high-level input voltage		VIH_EN	1.365	VIO	
Enable inputs low-level input voltage		VIL_EN	0	0.4	
High-level output voltage	@ 4 mA	VOH	VIO -0.45	VIO	
Low-level output voltage	@ 4 mA	VOL	0	0.45	
Input transitions time Tr/Tf from 10% to 90% (Digital IO) [2]		Tr/Tf	1	10	ns
Output rise time from 10% to 90% (Digital pins) [2]	CL < 25 pF	Tr		5.3	ns
Output fall time from 10% to 90% (Digital pins) [2]	CL < 25 pF	Tf		4.9	
Ambient operating temperature			-20	75	ºC
Maximum power dissipation	WLAN operation			2.8	W
	BT operation			0.2	

(1) 4.8V is applicable only for 2.3 years (30% of the time). Otherwise, the maximum VBAT should not exceed 4.3V.
(2) Applies to all Digital lines except SDIO, UART, I2C, PCM and slow clock lines

4.1.3 External Slow Clock Input (SLOW_CLK)

The supported digital slow clock is 32.768 kHz digital (square wave).

Parameter	Condition	Sym	Min.	Typ.	Max.	Units
Input slow clock Frequency				32.768		KHz
Input slow clock accuracy (Initial + temp + aging)	WLAN, BT				+/-250	ppm
Input Transition time Tr/Tf - 10% to 90%		Tr/Tf			100	ns
Frequency input duty Cycle			15	50	85	%
Input Voltage Limits	Square Wave, DC-coupled	Vih	0.65x VIO		VIO	Vpeak
		Vil	0		0.35x VIO	
Input Impedance			1			MΩ
Input Capacitance					5	pF

4.2. WLAN RF Performance

4.2.1 WLAN 2.4-GHz Receiver

Parameter	Condition	Min	Typ	Max	Units
Operation frequency range		2412		2484	MHz
Sensitivity - 20MHz Bandwidth - At < 10% PER limit	1 Mbps DSSS		-96.3	-93.4	dBm
	2 Mbps DSSS		-93.2	-90.5	
	5.5 Mbps CCK		-90.6	-87.9	
	11 Mbps CCK		-87.9	-85.7	
	6 Mbps OFDM		-92	-89.2	
	9 Mbps OFDM		-90.4	-87.7	
	12 Mbps OFDM		-89.5	-86.8	
	18 Mbps OFDM		-87.2	-84.5	
	24 Mbps OFDM		-84.1	-81.4	
	36 Mbps OFDM		-80.7	-78	
	48 Mbps OFDM		-76.5	-73.8	
	54 Mbps OFDM		-74.9	-72.4	
	MCS0 MM 4K		-90.4	-87.4	
	MCS1 MM 4K		-87.6	-84.9	
	MCS2 MM 4K		-85.9	-83.2	
	MCS3 MM 4K		-82.8	-80.1	
	MCS4 MM 4K		-79.4	-76.7	
	MCS5 MM 4K		-75.2	-72.5	
	MCS6 MM 4K		-73.5	-70.8	
	MCS7 MM 4K		-72.4	-69.7	
	MCS0 MM 4K 40MHz		-87.4	-82.7	
	MCS7 MM 4K 40MHz		-69	-65.5	
Max Input Level At < 10% PER limit	OFDM(11g/n)	-20	-10		dBm
	CCK	-4	-1		
Adjacent channel rejection Sensitivity level +3dB for OFDM, Sensitivity level +6dB for 11b	2Mbps DSSS	42.0			dBm
	11Mbps CCK	38.0			
	54Mbps OFDM	2.0			

4.2.2 WLAN 2.4-GHz Transmitter

Parameter	Condition	Min	Typ	Max	Units
Operation frequency range		2412		2484	MHz

Output Power
 	
- Maximum RMS output power
 	
  measured at 1dB from IEEE
 	
  spectral mask or EVM
	1 Mbps DSSS	15	17		dBm

	2 Mbps DSSS	15	17		
	5.5 Mbps CCK	15	17		
	11 Mbps CCK	15	17		
	6 Mbps OFDM	15	17		
	9 Mbps OFDM	15	17		
	12 Mbps OFDM	15	17		
	18 Mbps OFDM	15	17		
	24 Mbps OFDM	14	16.2		
	36 Mbps OFDM	13.1	15.3		
	48 Mbps OFDM	12.4	14.6		
	54 Mbps OFDM	11.8	13.8		
	MCS0 MM	13.9	16.1		
	MCS1 MM	13.9	16.1		
	MCS2 MM	13.9	16.1		
	MCS3 MM	13.9	16.1		
	MCS4 MM	13.3	15.3		
	MCS5 MM	12.4	14.6		
	MCS6 MM	11.8	13.8		
	MCS7 MM [1]	10.6	12.6		
	MCS0 MM 40MHz	12.3	14.8		
	MCS7 MM 40MHz	10.2	12.2		
Return loss			-10		dB
Reference input impedance			50		Ω

(1) To ensure compliance with the EVM conditions specified in the PHY chapter of IEEE Std 802.11™ – 2012:
- MCS7 20 MHz channel 12 output power is 2 dB lower than the typical value.
- MCS7 20 MHz channel 8 output power is 1 dB lower than the typical value.

4.3. Bluetooth RF Performance

4.3.1 BT Receiver Characteristics, In-Band Signals

Parameter	Condition		Min	Typ	Max	Units
BT BR, EDR operation frequency range			2402		2480	MHz
BT BR, EDR channel spacing				1		MHz
BT BR, EDR input impedance				50		Ω
BT BR, EDR sensitivity [1] Dirty TX on	BR, BER = 0.1%			-92.2	-88.7	dBm
	EDR2, BER = 0.01%			-91.7	-87.7	
	EDR3, BER = 0.01%			-84.7	-80.2	
BT EDR BER floor at sensitivity + 10 dB, dirty TX off (for 1,600,000 bits)	EDR2		1e-6			
	EDR3		1e-6			
BT BR, EDR maximum useable input power	BR, BER = 0.1%		-5.0			dBm
	EDR2, BER = 0.1%		-15.0			
	EDR3, BER = 0.1%		-15.0			
BT BR intermodulation	Level of interferers For n = 3, 4, and 5		-36.0	-30.0		dBm
BT BR, EDR C/I performance Numbers show wanted-signal to interfering-signal ratio. Smaller numbers indicate better C/I performances (Image frequency = -1MHz)	BR, Co-channel			8.0	10.0	dB
	EDR, Co-channel	EDR2		9.5	12.0	
		EDR3		16.5	20.0	
	BR, adjacent ±1 MHz			-10.0	-3.0	
	EDR, adjacent ±1 MHz, (image)	EDR2		-10.0	-3.0	
		EDR3		-5.0	2.0	
	BR, adjacent +2 MHz			-38.0	-33.0	
	EDR, adjacent +2 MHz,	EDR2		-38.0	-33.0	
		EDR3		-38.0	-28.0	
	BR, adjacent -2 MHz			-28.0	-20.0	
	EDR, adjacent -2 MHz	EDR2		-28.0	-20.0	
		EDR3		-22.0	-13.0	
	BR, adjacent ≥I±3I MHz			-45.0	-42.0	
	EDR, adjacent ≥I±3I MHz	EDR2		-45.0	-42.0	
		EDR3		-44.0	-36.0	
BT BR, EDR RF return loss				-10.0		dB

(1) Sensitivity degradation up to -3dB may occur due to fast clock harmonics with dirty TX on.

4.3.2 BT Transmitter, BR

Parameter		Min	Typ	Max	Units
BR RF output power [1]	VBAT >= 3V		11.7		dBm
	VBAT < 3V		7.2		
BR Gain Control Range			30		dB
BR Power Control Step			5		
BR Adjacent Channel Power |M-N| = 2			-43		dBm
BR Adjacent Channel Power |M-N| > 2			-48		

(1) Values reflect maximum power. Reduced power is available using a vendor-specific (VS) command.

4.3.3 BT Transmitter, EDR

Parameter		Min	Typ	Max	Units
EDR output power [1]	VBAT >= 3V		7.2		dBm
	VBAT < 3V		5.2		
EDR relative power		-2		1	dB
EDR Gain Control Range			30		dB
EDR Power Control Step		2	5	8	dB
EDR Adjacent Channel Power |M-N| = 1			-36		dBc
EDR Adjacent Channel Power |M-N| = 2			-30		dBm
EDR Adjacent Channel Power |M-N| > 2			-42		

(1) Values reflect maximum power. Reduced power is available using a vendor-specific (VS) command.

4.3.4 BT Modulation, BR

Parameter	Condition[1]		Min	Typ	Max	Units
BR -20dB Bandwidth				925	995	kHz
BR modulation characteristics	Δf1avg	Mod data = 4-ones, 4-zeros: 111100001111...		160		kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...		130		kHz
	Δf2avg / Δf1avg			88		%
BR carrier frequency drift	One slot packet		-25		+25	kHz
	Three and five slot packet		-35		35	kHz

| BR drift rate | lfk+5 – fkl , k = 0 …. max | | | 15 | kHz/ 50µs |
| BR initial carrier frequency tolerance (2) | f0 – fTX | -75 | | 75 | kHz |

(1) Performance figures at maximum power
(2) This number is added on top of the reference clock frequency accuracy

4.3.5 BT Modulation, EDR

Parameter [1]	Condition	Min	Typ.	Max	Units
EDR Carrier frequency stability		-5		5	kHz
EDR Initial Carrier Frequency Tolerance [2]		-75		75	kHz
EDR RMS DEVM	EDR2		4		%
	EDR3		4		%
EDR 99% DEVM	EDR2			30	%
	EDR3			20	%
EDR Peak DEVM	EDR2		9		%
	EDR3		9		%

(1) Performance figures at maximum power
(2) This number is added on top of the reference clock frequency accuracy

4.4. BT LE RF Performance

4.4.1 BT LE Receiver Characteristics, In-Band Signals

Parameter	Condition [2]	Min	Typ	Max	Units
BT LE Operation frequency range		2402		2480	MHz
BT LE Channel spacing			2		MHz
BT LE Input impedance			50		Ω
BT LE Sensitivity [1], Dirty Tx on			-92.2		dBm
BT LE Maximum useable input power		-5			dBm
BT LE Intermodulation characteristics	Level of interferers. For n = 3, 4, 5	-36	-30		dBm
BT LE C/I performance Note: Numbers show wanted signal-to-interfering signal ratio. Smaller numbers indicate better C/I performance. Image = -1MHz	LE, co-channel		8	12	dB
	LE, adjacent ±1MHz		-5	0	
	LE, adjacent +2MHz		-45	-38	
	LE, adjacent –2MHz		-22	-15	
	LE, adjacent ≥ |±3|MHz		-47	-40	

(1) BER of 0.1% corresponds to PER of 30.8% for a minimum of 1500 transmitted packets, according to Bluetooth LE test specification.

(2) Sensitivity degradation up to -3dB may occur due to fast clock harmonics.

4.4.2 BT LE Transmitter Characteristics

Parameter		Min	Typ	Max	Unit
BT LE RF output power [1]	Vbat >= 3V [2]		7.0		dBm
	Vbat < 3V		7.0		dBm
BT LE Adjacent Channel Power |M-N| = 2			-51		dBm
BT LE Adjacent Channel Power |M-N| > 2			-54		

(1) Bluetooth low energy power is restricted to comply with the ETSI 10-dBm EIRP limit requirement.

(2) VBAT is measured with an on-chip ADC that has an accuracy error of up to 5%.

4.4.3 BT LE Modulation Characteristics

Parameter	Condition [1]		Performances			Units
			Min	Typ	Max	
BT LE modulation characteristics	Δf1avg	Mod data = 4-ones, 4-zeros: 111100001111...	240	250	260	kHz
	Δf2max ≥ limit for at least 99.9% of all Δf2max	Mod data = 1010101...	195	215		kHz
	Δf2avg / Δf1avg			90		%
BT LE carrier frequency drift	lf0 – fnl , n = 2,3 …. K		-25		25	kHz
BT LE drift rate	lf1 – f0l and lfn – fn-5l ,n = 6,7…. K				15	kHz/ 50µs
LE initial carrier frequency tolerance [2]	fn – fTX		-75		75	kHz

(1) Performance figures at maximum power.
(2) Numbers include XTAL frequency drift over temperature and aging.

4.5. POWER CONSUMPTION

All measurements are performed with Vbat = 3.7V, VIO = 1.8V, temperature at 25°C.

4.5.1 Shutdown and Sleep Currents

Parameter	Power Supply Current	Typ	Max.	Unit
Shutdown mode	VBAT	10	15	
All functions shut down.	VIO	2	3	
WLAN sleep mode	VBAT	160	340	uA
BT sleep mode	VBAT	110	285	

4.5.2 Operating Conditions

Parameter	Power Supply Current	Typ	Max.	Unit
Connected IDEL	VBAT	750	960	uA
VBAT[1]	VBAT	420	850	mA
VIO[2]	VIO	40	450	uA

(1) VBAT quoted to max operational TX consumption and periodic calibration current.
(2) VIO quoted for operational IO's (WLAN + BT IF) without debug IO.

4.5.3 WLAN Power Currents

Parameter	Conditions	Typ (avg)	Max.	Units
LPM	2.4GHz RX LPM	49	61	mA
Receiver	2.4GHz RX search SISO20	54	66	mA
	2.4GHz RX search SISO40	59	72	mA
	2.4GHz RX 20M SISO 11CCK	56	72	mA
	2.4GHz RX 20M SISO 6OFDM	61	72	mA
	2.4GHz RX 20M SISO MCS7	65	77	mA
	2.4GHz RX 40MHz MCS7	77	90	mA
Transmitter	2.4GHz TX 20M SISO 6OFDM 17dBm	285	374	mA
	2.4GHz TX 20M SISO 11CCK 17dBm	273	357	mA
	2.4GHz TX 20M SISO 54OFDM 13.8dBm	247	328	mA
	2.4GHz TX 20M SISO MCS7 12.6dBm	238	321	mA
	2.4GHz TX 40M SISO MCS7 12.2dBm	243	329	mA

4.5.4 Bluetooth Currents

Current measurements are done at the following output power:

BR at 11.7dBm,   EDR at 7.2dBm.

Use Case [1]	Typ	Units
BR Voice HV3 + sniff	11.6	mA
EDR Voice 2-EV3 no retrans. + sniff	5.9	mA
Sniff 1 attempt 1.28s	178	uA
EDR A2DP EDR2 (master). SBC high quality – 345Kbs	10.4	mA
EDR A2DP EDR2 (master). MP3 high quality – 192Kbs	7.5	mA
Full throughput ACL RX: RX-2DH5 [2] [3]	18	mA
Full throughput BR ACL TX: TX-DH5 [3]	50	mA
Full throughput EDR ACL TX: TX-2DH5 [3]	33	mA
Page or inquiry 1.28s/11.25ms	253	uA
P&I Scan (P=1.28/I=2.56)	332	uA

(1)   The role of Bluetooth in all scenarios except A2DP is slave.
(2)   CL1P5 PA is connected to VBAT, 3.7V.
(3)   Full throughput assumes data transfer in one direction.

4.5.5 Bluetooth LE Currents

All current measurements are done at output power of 7dBm

Use Case	Typ	Units
Advertising, non-connectable [1]	131	uA
Advertising, discoverable [1]	143	uA
Scanning [2]	266	uA
Connected, master role, 1.28sec conn. Interval [3]	124	uA
Connected, slave role, 1.28sec conn. Interval [3]	132	uA

(1)   Advertising in all 3 channels, 1.28sec advertising interval, 15 Bytes advertise data.
(2)   Listening to a single frequency per window, 1.28sec scan interval, 11.25msec scan window.
(3)   Zero Slave connection latency Empty Tx/Rx LL packets.

5. HOST INTERFACE TIMING CHARACTERISTICS

The following table summarizes the Host Controller interface options. All interfaces operate independently.

WLAN	Shared HCI for all functional blocks except WLAN	BT Voice/Audio
WLAN HS SDIO	Over UART	BT PCM

The device incorporates UART module dedicated to the BT shared-transport Host Controller Interface (HCI) transport layer. The HCI interface is used to transport commands, events and ACL between the Bluetooth device and its host using HCI data packets. This acts as a shared transport for all functional blocks except WLAN.

5.1. WLAN SDIO Transport Layer

The SDIO is the host interface for WLAN. The interface between the host and the device uses an SDIO interface and supports a maximum clock rate of 50MHz.

The Device SDIO also supports the following features of the SDIO V3 specification:
● 4 bit data bus
● Synchronous and Asynchronous In-Band-Interrupt
● Default and High-Speed (50MHz) timing
● Sleep/wake commands

5.2. SDIO Timing Specifications

5.2.1 SDIO Switching Characteristics – Default Rate
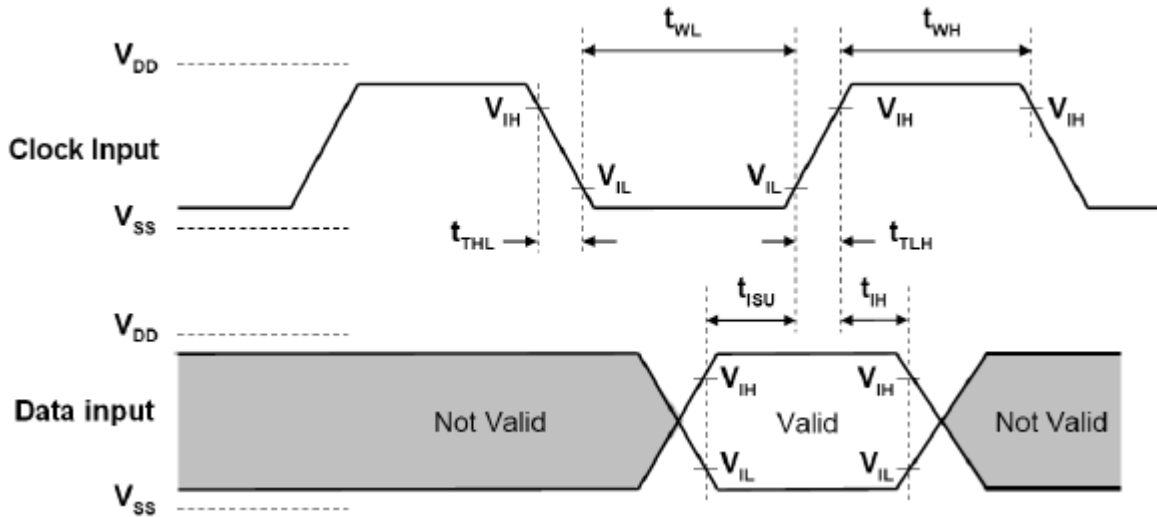
Figure 5-1. SDIO default input timing
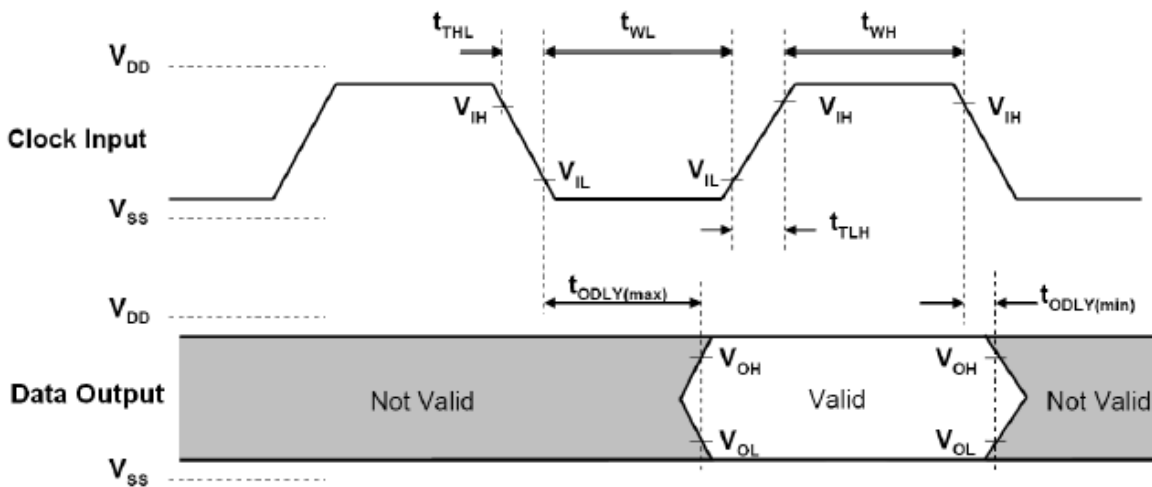
Figure 5-2. SDIO default output timing

Table 5-1. SDIO Default Timing Characteristics[1]

PARAMETER[2]		MIN	MAX	UNIT
Fclock	Clock frequency, CLK	0	26	MHz
DC	Low/high duty cycle	40	60	%
tTLH	Rise time, CLK		10	ns
tTHL	Fall time, CLK		10	ns
tISU	Setup time, input valid before CLK↑	3		ns

tIH	Hold time, input valid after CLK↑	2		ns
tODLY	Delay time, CLK↓ to output valid	2.5	14.8	ns
CI	Capacitive load on outputs		15	pF

(1) To change the data out clock edge from the falling edge (default) to the rising edge, set the configuration bit.
(2) Parameter values reflect maximum clock frequency.

5.2.2 SDIO Switching Characteristics – High Rate
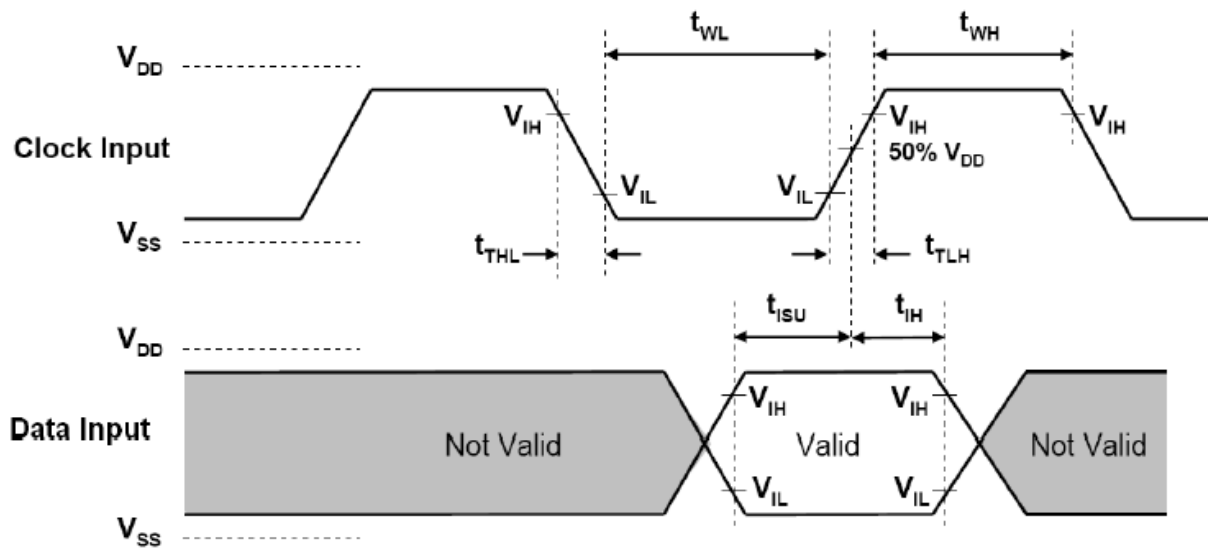
Figure 5-3. SDIO HS input timing
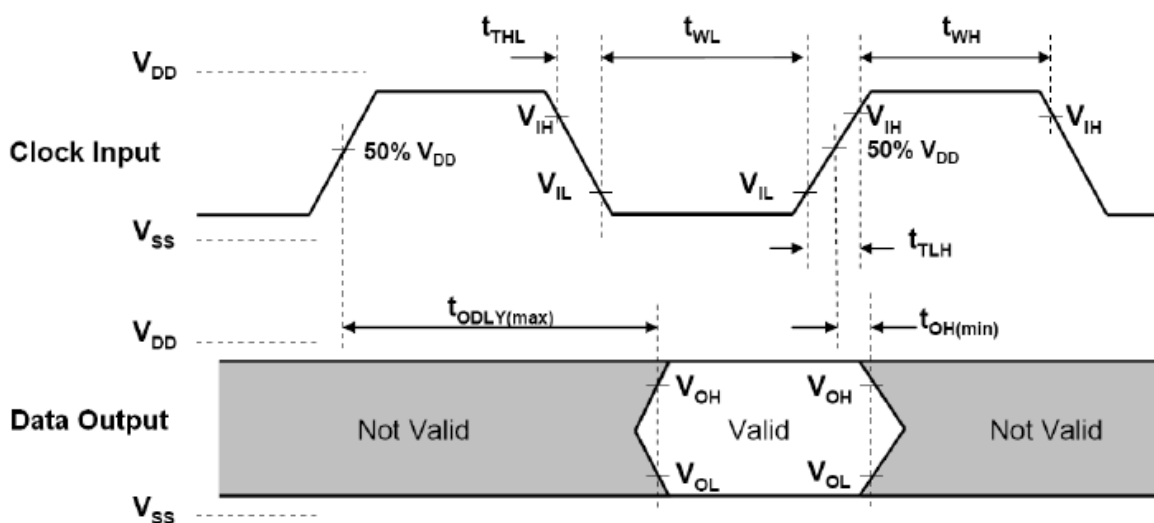
Figure 5-4. SDIO HS output timing

Table 5-2. SDIO HS Timing Characteristics

PARAMETER		MIN	MAX	UNIT
Fclock	Clock frequency, CLK	0	50	MHz
DC	Low/high duty cycle	40	60	%
tTLH	Rise time, CLK		3	ns
tTHL	Fall time, CLK		3	ns
tISU	Setup time, input valid before CLK↑	3		ns
tIH	Hold time, input valid after CLK↑	2		ns
tODLY	Delay time, CLK↓ to output valid	2.5	14	ns
CI	Capacitive load on outputs		10	pF

5.3. HCI UART Shared Transport Layers for All Functional Blocks

The HCI UART supports most baud rates (including all PC rates) for all fast clock frequencies up to a maximum of 4 Mbps. After power up the baud rate is set for 115.2 kbps, regardless of fast clock frequency. The baud rate can then be changed by using a VS command. The Device responds with a Command Complete Event (still at 115.2 kbps), after which the baud rate change occurs.

HCI hardware includes the following features:
- Receiver detection of break, idle, framing, FIFO overflow and parity error conditions.
- Receiver Transmitter underflow detection.
- CTS/RTS hardware flow control.
- 4 wires (H4)

The below table lists the UART default settings

Table 5-3. UART Default Setting

Parameter	Value
Bit Rate	115.2 kbps
Data Length	8 bits
Stop Bit	1
Parity	None

5.3.1 UART 4-Wires Interface – H4

The interface includes four signals: TXD, RXD, CTS and RTS. Flow control between the host and the Device is byte-wise by hardware. (See Figure 5-5)
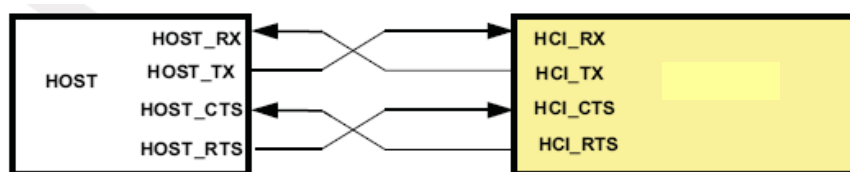
Figure 5-5. HCI UART Connection

When the UART RX buffer of the device passes the flow-control threshold, the buffer sets the UART_RTS signal high to stop transmission from the host. When the UART_CTS signal is set high, the device stops transmitting on the interface. If HCI_CTS is set high in the middle of transmitting a byte, the device finishes transmitting the byte and stops the transmission.

5.4. UART Timing Specifications
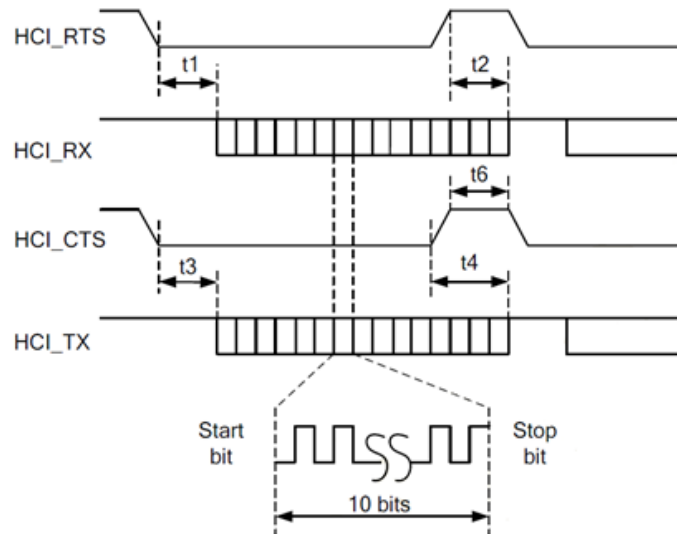
Figure 5-6. UART Timing Diagram

Table 5-4. UART Timing Characteristics

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Baud rate			37.5		4364	Kbps
Baud rate accuracy per byte	RX/TX		-2.5		+1.5	%
Baud rate accuracy per bit	RX/TX		-12.5		+12.5	%
CTS low to TX_DATA on		t3	0	2		us
CTS low to TX_DATA off	Hardware flow control	t4			1	Byte
CTS High Pulse Width		t6	1			bit
RTS low to RX_DATA on		t1	0	2		us
RTS high to RX_DATA off	Interrupt set to 1/4 FIFO	t2			16	Bytes
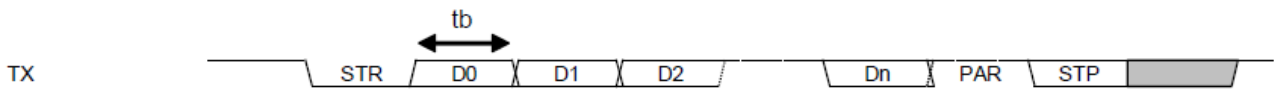
STR-Start bit;   D0..Dn - Data bits (LSB first); PAR - Parity bit (if used);   STP - Stop bit

Figure 5-7. UART Data Frame

5.5. Bluetooth Codec-PCM(Audio) Timing Specifications

Figure 5-8 shows the Bluetooth codec-PCM (audio) timing diagram.

Table 5-5 lists the Bluetooth codec-PCM master timing characteristics.

Table 5-6 lists the Bluetooth codec-PCM slave timing characteristics.
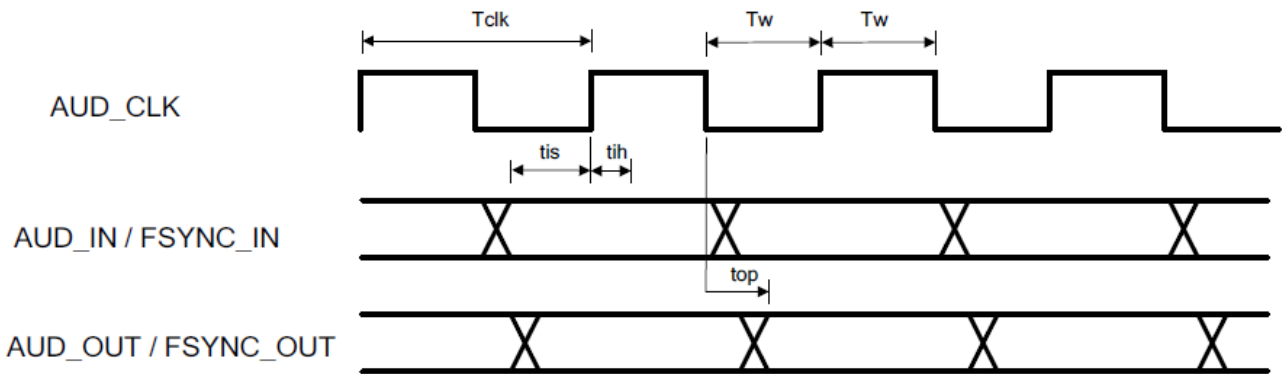
Figure 5-8. PCM Interface Timing

Table 5-5. Bluetooth Codec-PCM Master Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Cycle time	Tclk	166.67 (6.144MHz)	15625 (64 kHz)	ns
High or low pulse width	Tw	35% of Tclk min		
AUD_IN setup time	tis	10.6		
AUD_IN hold time	tih	0		
AUD_OUT propagation time	top	0	15	
AUD_FSYNC_OUT propagation time	top	0	15	
Capacitive loading on outputs	Cl		40	pF

Table 5-6. Bluetooth Codec-PCM Slave Timing Characteristics

Parameter	Symbol	Min	Max	Unit
Cycle time	Tclk	81 (12.288MHz)		ns
High or low pulse width	Tw	35% of Tclk min		
AUD_IN setup time	tis	5		
AUD_IN hold time	tih	0		
AUD_OUT propagation time	top	5		
AUD_FSYNC_OUT propagation time	top	0	19	
Capacitive loading on outputs	Cl		40	pF

6. CLOCK AND POWER MANAGEMENT

The slow clock is a free-running, 32.768 kHz clock supplied from an external clock source. The clock is connected to the SLOW_CLK pin and is a digital square-wave signal in the range of 0 to 1.8V nominal

6.1. Reset-Power-Up System

After VBAT and VIO are fed to the device and while BT_EN and WL_EN are deasserted (low), the device is in SHUTDOWN state, during which functional blocks, internal DC-DCs, and LDOs are disabled. The power supplied to the functional blocks is cut off. When one of the signals (BT_EN or WL_EN) are asserted (high), a power-on reset (POR) is performed. Stable slow clock, VIO, and VBAT are prerequisites for a successful POR.

6.2. Reset-Power-Up System

Figure 6-1 shows the WLAN power-up sequence.
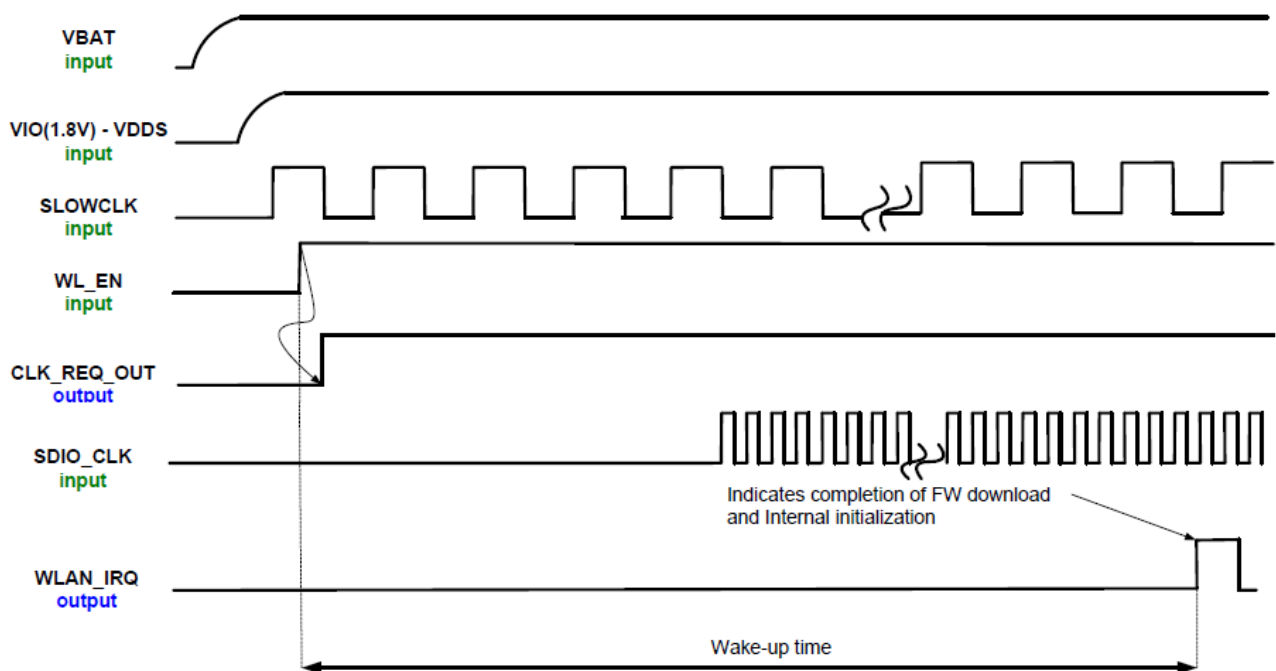
Figure 6-1. WLAN Power-Up Sequence

6.3. Bluetooth/BLE Power-Up Sequence

Figure 6-2 shows the Bluetooth/BLE power-up sequence.
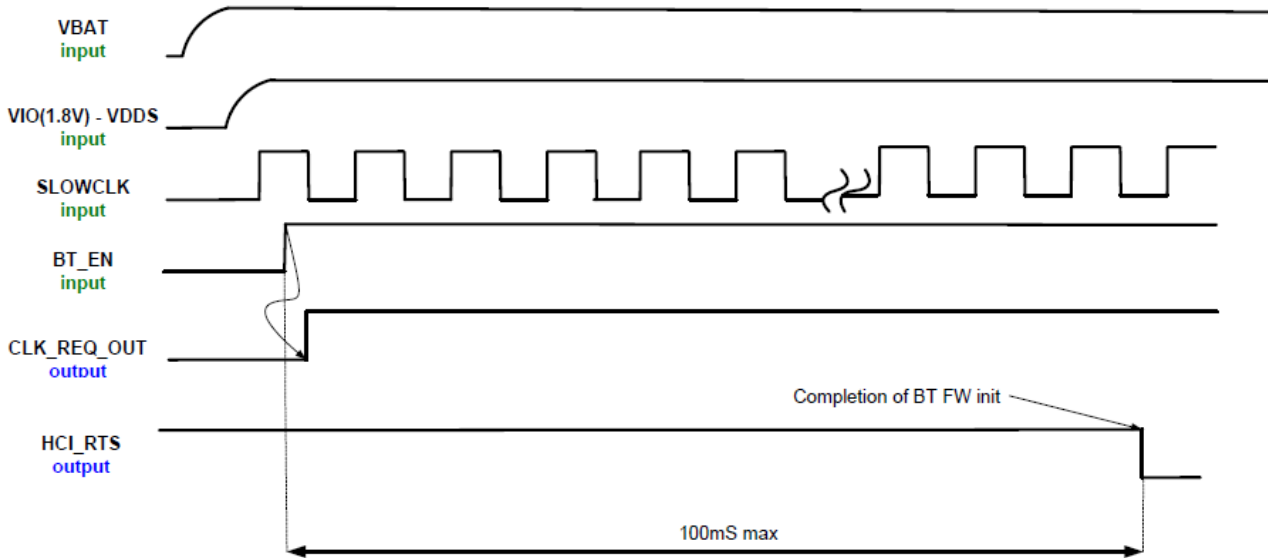
Figure 6-2 Bluetooth/BLE power-up sequence

7. REFERENCE SCHEMATICS
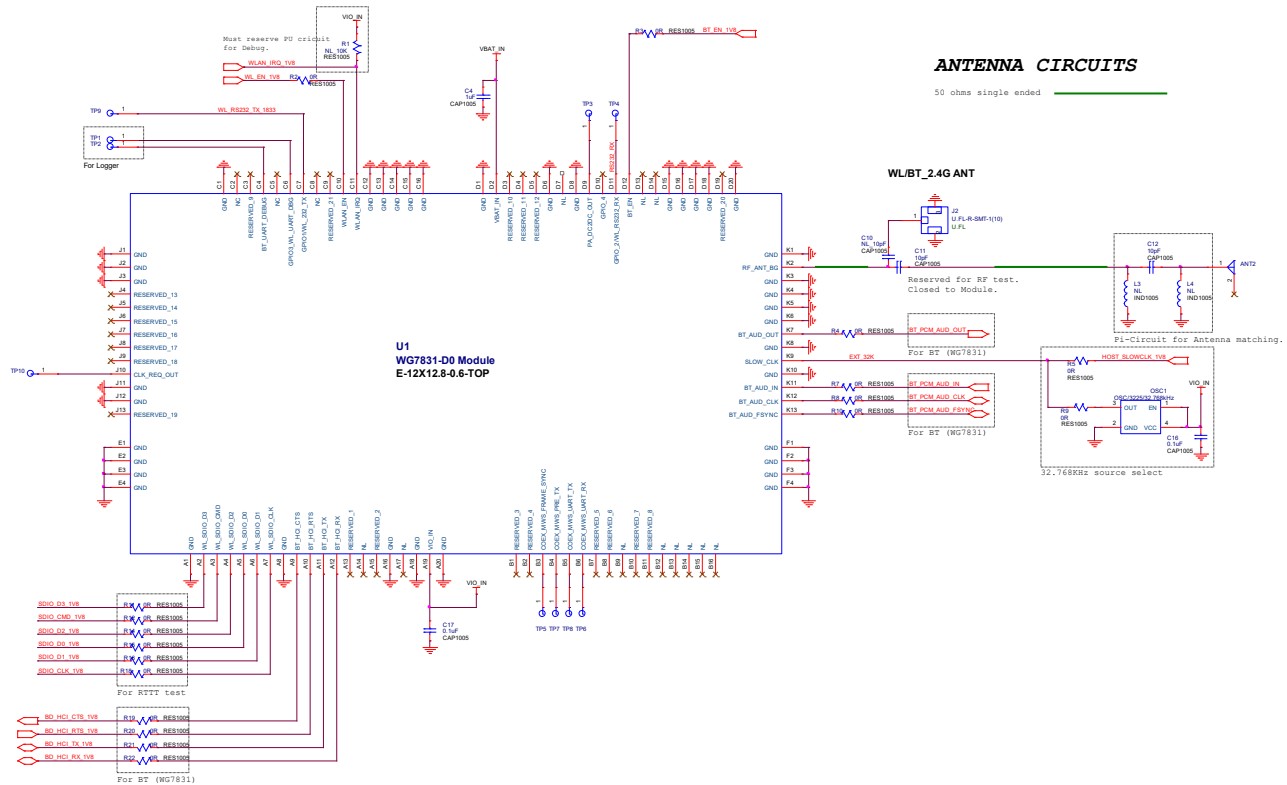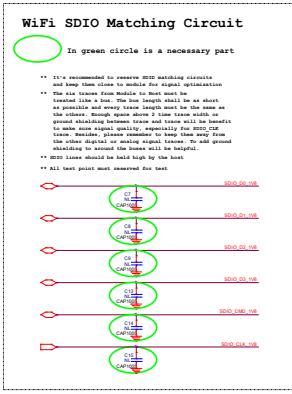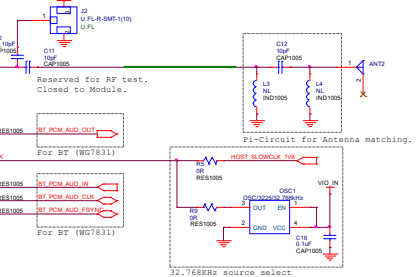
8. DESIGN RECOMMENDATIONS

8.1. Design Note on Debug Port

- Pin# C6, C4 serve as WLAN and BT debug port, respectively. So test points for these two signals should be reserved for debugging purpose.
- Pin# C11 (WLAN_IRQ) needs to be pulled high via 10Kohm and use Pin# D11, C7 (WL_RS232_RX, WL_RS232_TX) as hardware interface to communicate with system platform and TI RTTT test utility for WLAN RF performance test, debug and manufacturing application.

8.2. Module Layout Recommendations

Follow these module layout recommendations:

- **Digital Signals Layout**
  - ➢ SDIO signals traces (CMD, D0, D1, D2 and D3) should be routed in parallel to each other and as short as possible. **(Less than 12cm) Besides, every trace length must be the same as the others.**
  - ➢ Enough space above 1.5 time trace width or ground shielding between trace and trace will be benefit to make sure signal quality, especially for SDIO_CLK trace. Remember to keep them away from the other digital or analog signal traces. Adding ground shielding around these bus is recommended.
  - ➢ Route trace of SDIO_CLK at Top layer without vias.
  - ➢ SDIO Clock, Audio Clock (PCM_AUD_CLK), these digital clock signals are a source of noise. Keep the traces of these signals as short as possible. Whenever possible, maintain a clearance around them.
  - ➢ BT_AUD signals should be rounted in the same group and it's better to rout them at the same layer or confirm them referring to the same reference plane.

- **RF Trace & Antenna**
  - ➢ Keep 50ohm trace impedance.
  - ➢ Move all the high-speed traces and components far away from the antenna.
 - ➢ Check antenna vendor for the layout guideline and clearance.

● **Power Trace**
  ➢ Power trace for VBAT should be 20mil wide. 1.8V trace should be 15mil wide, at least.
 ➢ Isolate different power traces with Ground plane

● **Ground**
  ➢ Having a complete Ground and more GND vias under module in layer1 for system stable and thermal dissipation.
  ➢ Have a complete Ground pour in layer 2 for thermal dissipation.
  ➢ Increase the GND pour in the 1st layer, move all the traces from the 1st layer to the inner layers if possible.
  ➢ Move GND vias close to the pad.

9. PACKAGE INFORMATION

9.1. Module Mechanical Outline

12.8±0.1 mm   1.63±0.1 mm

12.0±0.1 mm

Top View   Side View
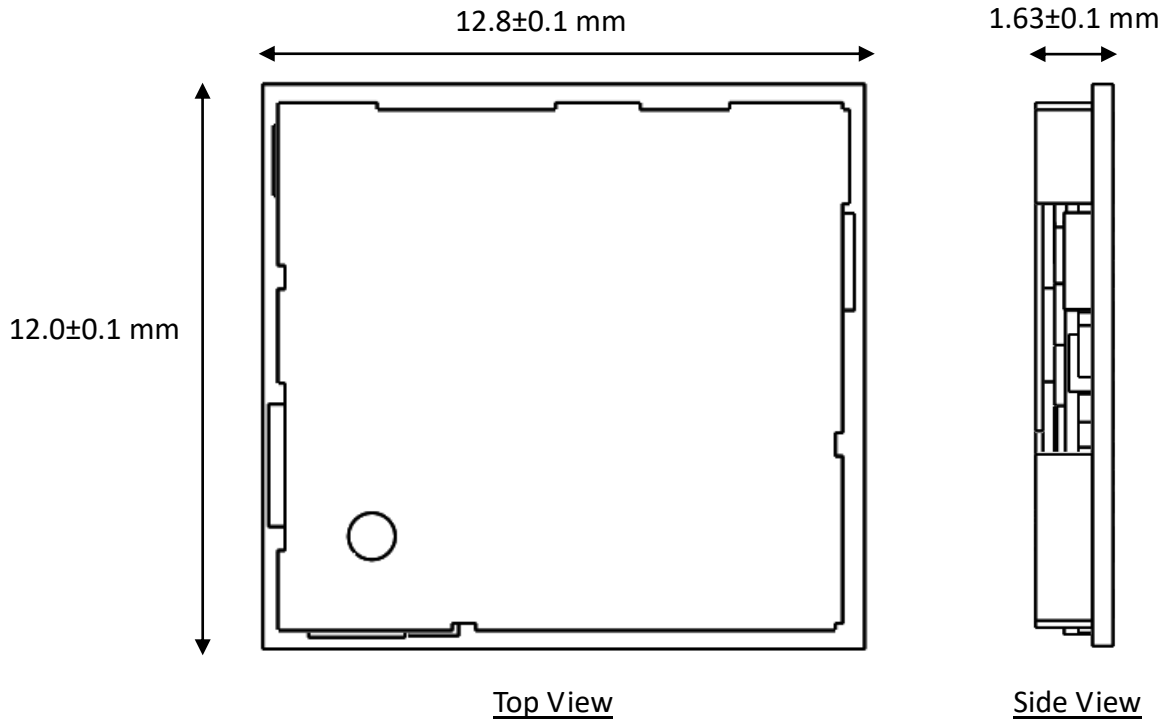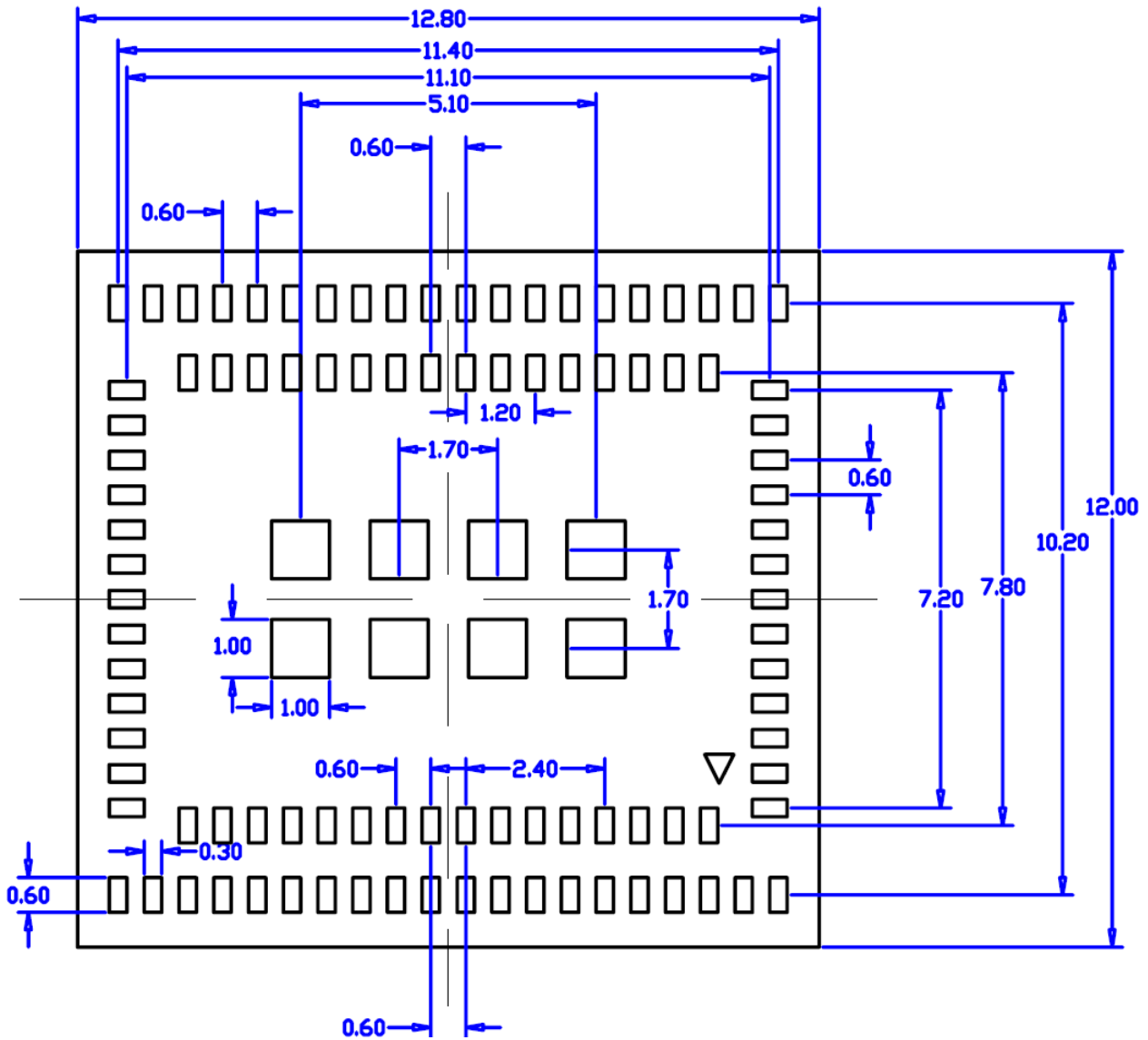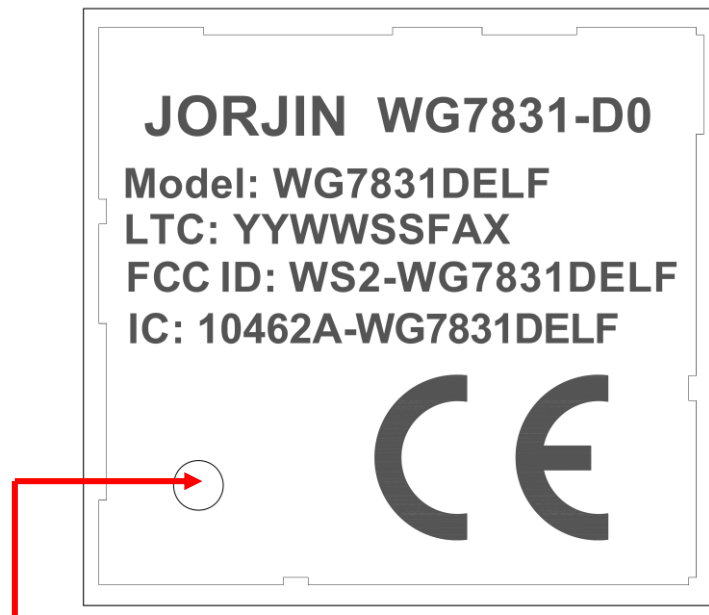
Bottom View

*We recommend adopting the same dimensions listed above for building PCB footprint.

** Pad tolerance as +/- 30um

9.2. Ordering Information

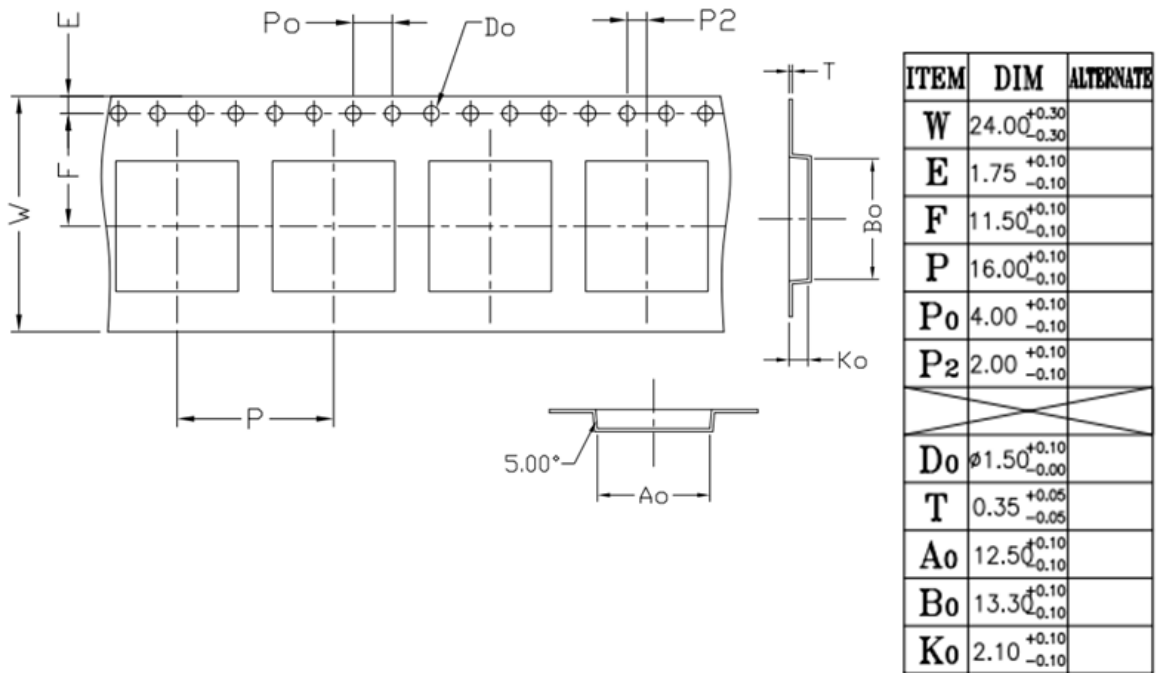| Part number:	WG7831-D0A

9.3. Package Marking

PIN-1 Marking

9.4. Certification Information

- **FCC ID :** WS2-WG7831DELF, single modular FCC grant ID
- **IC ID :** 10462A-WG7831DELF, single modular IC grant ID
- **CE :** CE compliance mark
- LTC : Date Code , **YYWWSSFAX**

    YY = Digit of the year, ex: 2011=11

    WW = Week (01~52)

    SS = Serial number from 01 ~99 match to manufacture's lot number

    F = Reserve for internal use

    A = Module version from A to Z
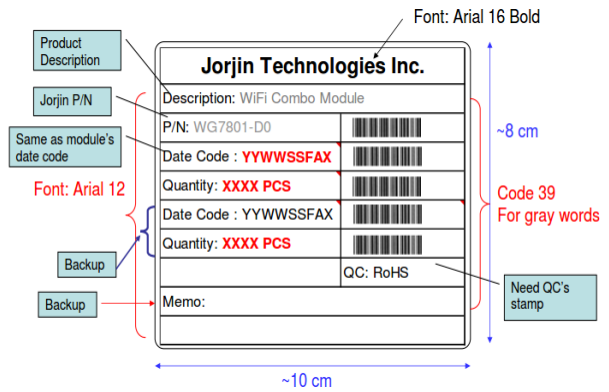
    X = Chip version

9.5. Packaging Specification

ITEM	DIM	ALTERNATE
W	$24.00^{+0.30}_{-0.30}$	
E	$1.75^{+0.10}_{-0.10}$	
F	$11.50^{+0.10}_{-0.10}$	
P	$16.00^{+0.10}_{-0.10}$	
Po	$4.00^{+0.10}_{-0.10}$	
P2	$2.00^{+0.10}_{-0.10}$	
Do	$\phi1.50^{+0.10}_{-0.00}$	
T	$0.35^{+0.05}_{-0.05}$	
Ao	$12.50^{+0.10}_{-0.10}$	
Bo	$13.30^{+0.10}_{-0.10}$	
Ko	$2.10^{+0.10}_{-0.10}$	

<Reel : 1.8K pcs per reel>

<Pizza box : 1 reel per pizza box>

<Carton : 5 pizza boxes per carton>
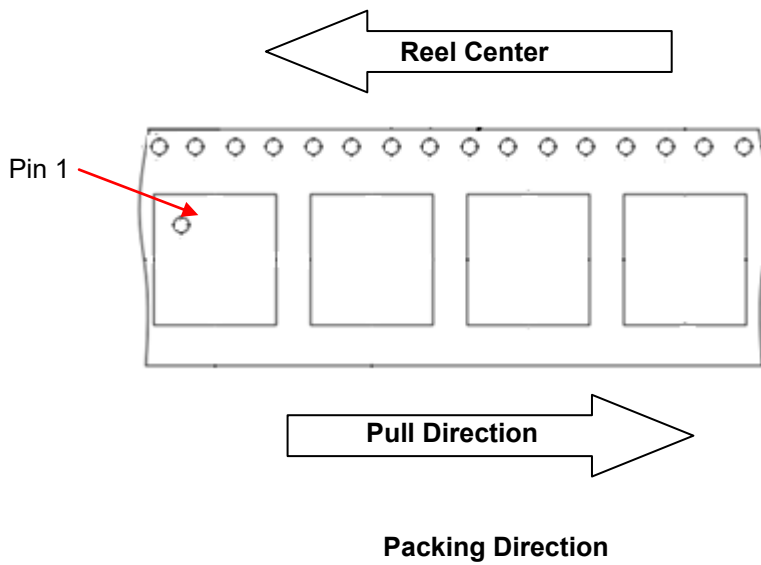

**Product label**

Packing Direction

10. SMT AND BAKING RECOMMENDATION

10.1. Baking Recommendation

➢ Baking condition：
- Follow MSL Level 4 to do baking process.
- After bag is opened, devices that will be subjected to reflow solder or other high temperature process must be
  a) Mounted within 72 hours of factory conditions <30°C/60% RH, or
  b) Stored at <10% RH.
- Devices require bake, before mounting, if Humidity Indicator Card reads >10%
  If baking is required, Devices may be baked for 8 hrs. at 125 °C.

10.2. SMT Recommendation

➢ Recommended Reflow profile：
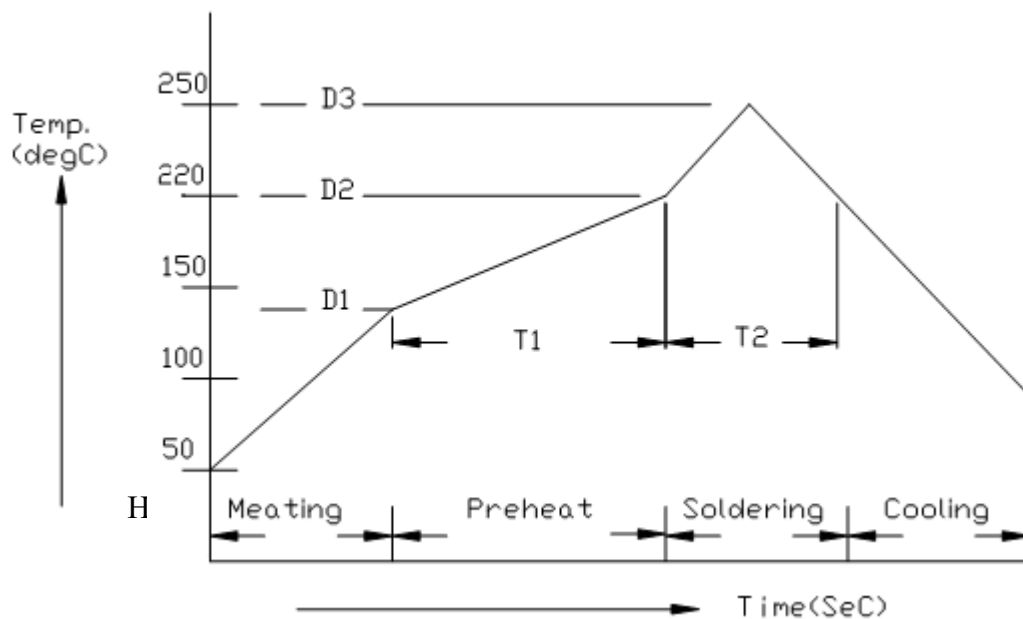
No.	Item	Temperature (°C)	Time (sec)
1	Pre-heat	D1: 140 ~ D2: 200	T1: 80 ~ 120
2	Soldering	D2: = 220	T2: 60 +/- 10
3	Peak-Temp.	D3: 250 °C max	

Note: (1) Reflow soldering is recommended two times maximum.

(2) Add Nitrogen while Reflow process： SMT solder ability will be better.

➤ **Stencil thickness**： 0.1~ 0.13 mm (Recommended)

➤ **Soldering paste (without Pb)**： Recommended SENJU N705-GRN3360-K2-V can get better soldering effects.

11. REGULATORY INFORMATION

This section outlines the regulatory information for the following countries:
- United States
- Canada
- Europe

11.1. United States

Federal Communications Commission Statement

15.21. You are cautioned that changes or modifications not expressly approved by the part responsible for compliance could void the user's authority to operate the equipment.
This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

    (1) This device may not cause harmful interference and

    (2) This device must accept any interference received, including interference that may cause undesired operation of the device.

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure limits. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

End Product Labeling:

This module is designed to comply with the FCC statement, FCC ID: WS2-WG7831DELF. The host system using this module must display a visible label indicating the following text:
"Contains FCC ID: WS2-WG7831DELF"

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as shown in this manual.

11.2. Canada

This device complies with Industry Canada's licence-exempt RSSs.

Operation is subject to the following two conditions:

  (1) this device may not cause interference, and

  (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence

L'exploitation est autorisée aux deux conditions suivantes:

  (1) l'appareil ne doit pas produire de brouillage, et

  (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

IC RF Radiation Exposure Statement:

To comply with IC RF exposure requirements, this device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.

Pour se conformer aux exigences de conformité RF canadienne l'exposition, cet appareil et son antenne ne doivent pas être co-localisés ou fonctionnant en conjonction avec une autre antenne ou transmetteur.

End Product Labeling:

This module is designed to comply with the IC statement, IC: 10462A-ZB7. The host system using this module must display a visible label indicating the following text:

"Contains IC: 10462A-WG7831DELF"

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual shall include all required regulatory information/warning as shown in this manual.

11.3. Europe

Jorjin Technologies Inc. declares that the radio equipment type RF module is in compliance with Directive 2014/53/EU

The full text of the EU declaration of conformity is available at the following internet address:
http://www.jorjin.com/upload/1507274387.pdf

The compliance has been verified in the operating frequency band of 2400 MHz to 2483.5 MHz. Developers and integrators that incorporate the WG7831-D0 Module in any end products are responsible for obtaining applicable regulatory approvals for such end product.

The WG7831-D0 has been tested in the 2400 MHz to 2483.5 MHz ISM frequency band at 3.3 V with a maximum peak power of 15.31 dBm EIRP across the temperature range –40°C to +85°C and tolerance.

Labeling and User Information Requirements

As a result of the conformity assessment procedure described in Annex III of the Directive 2014/53/EU, the end-customer equipment should be labeled as follows:

$$C \, \epsilon$$

12. HISTORY CHANGE

Revision	Date	Description
R 0.1	2014 / 10 / 16	Initial Released
R 0.2	2015 / 11 / 17	1. Support to Bluetooth 4.1 2. Remove ANT function of module.
R 0.3	2016 / 05 / 23	1. Separated from WG7831_01-D0-DTS-R02. 2. Add Certification Information
R 0.4	2017 / 01 / 25	1. Modified 5.1 description. 2. Support Bluetooth 4.2.
R 0.5	2017 / 10 / 13	1. Add CE RED Certification Information. 2. Updated Module package marking information.
R 0.6	2018 / 10 / 29	1. Updated absolute maximum ratings and recommended operating 2. Updated WLAN 2.4G RF Performance 3. Updated Bluetooth RF Performance 4. Updated Bluetooth LE Transmitter 5. Updated Power consumption information

单击下面可查看定价，库存，交付和生命周期等信息

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单击下面可查看定价，库存，交付和生命周期等信息